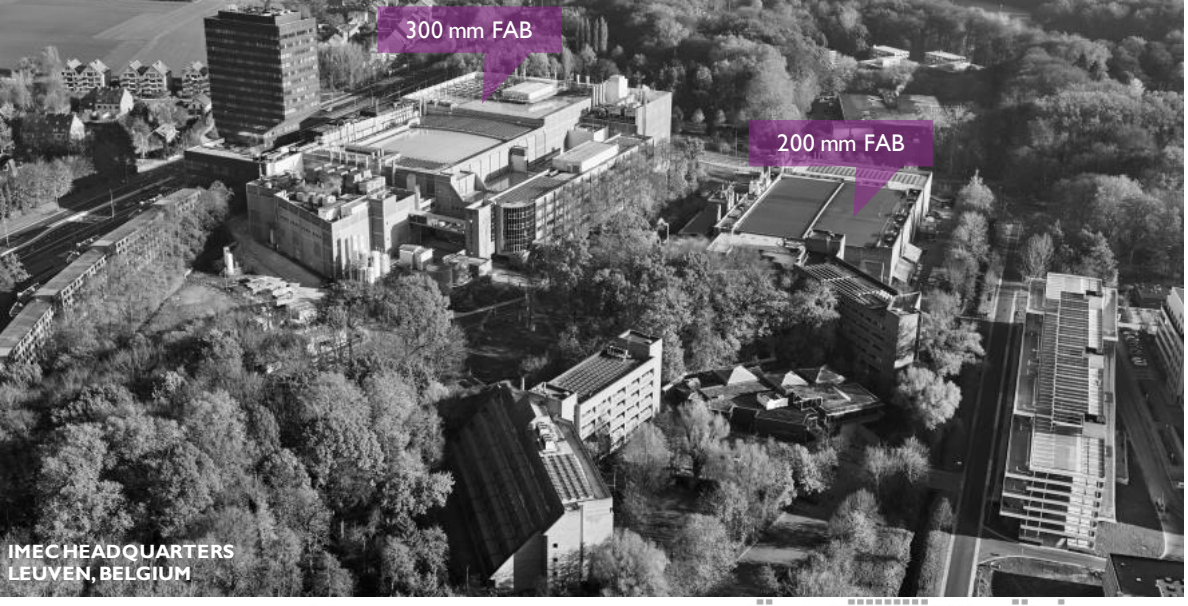
Extending the CMOS technology roadmap with system technology co-optimization

James Myers

STCO Program Director & UK Site Manager

Outline

- An introduction to imec and imec UK
- The CMOS technology landscape through system eyes
- System Technology Co-optimization (STCO): what system, what technology?
- How does STCO work and what does it get us?



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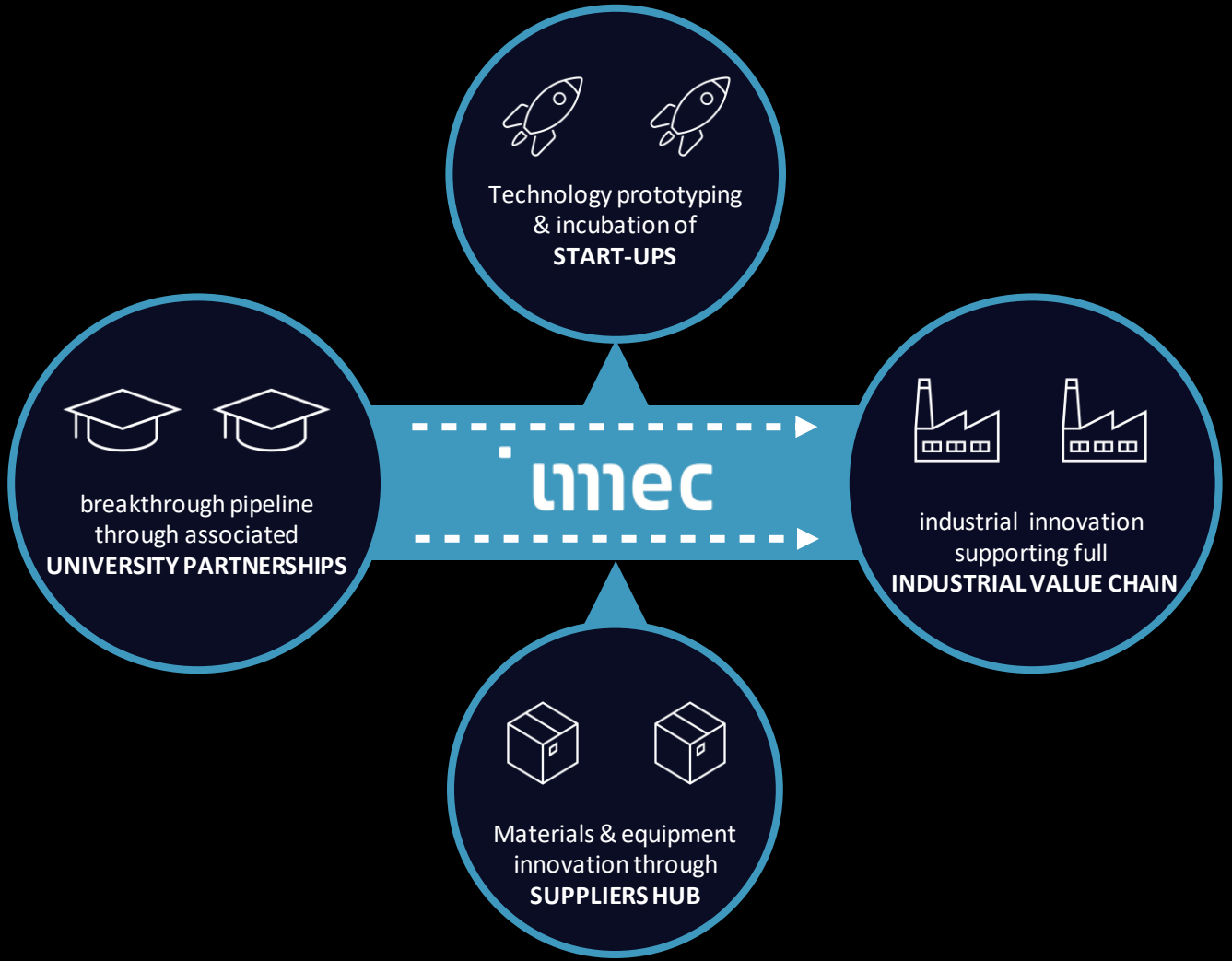
- World-leading R&D in **nano-electronics & digital technology**
- Delivering **industry relevant technology** R&D solutions for ICT, Healthcare and Energy markets **5-10 years ahead** of market introduction
- **5500** international R&D top talents from 95 nationalities
- Unique **€ 3.5B leading edge semiconductor R&D fabs**
- **€ 845M revenues: 75%** industry, **16%** regional gov't, **9 %** EU & regional programs
- **Not-for-profit** R&D center
- Created **120+ spin-off** companies since 1984


Technology prototyping
& incubation of
START-UPS
breakthrough pipeline
through associated
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imec
industrial innovation
supporting full
INDUSTRIAL VALUE CHAIN
Materials & equipment
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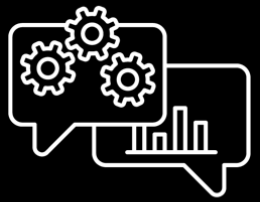
BUSINESS MODELS TO CREATE IMPACT

R&D
COLLABORATION



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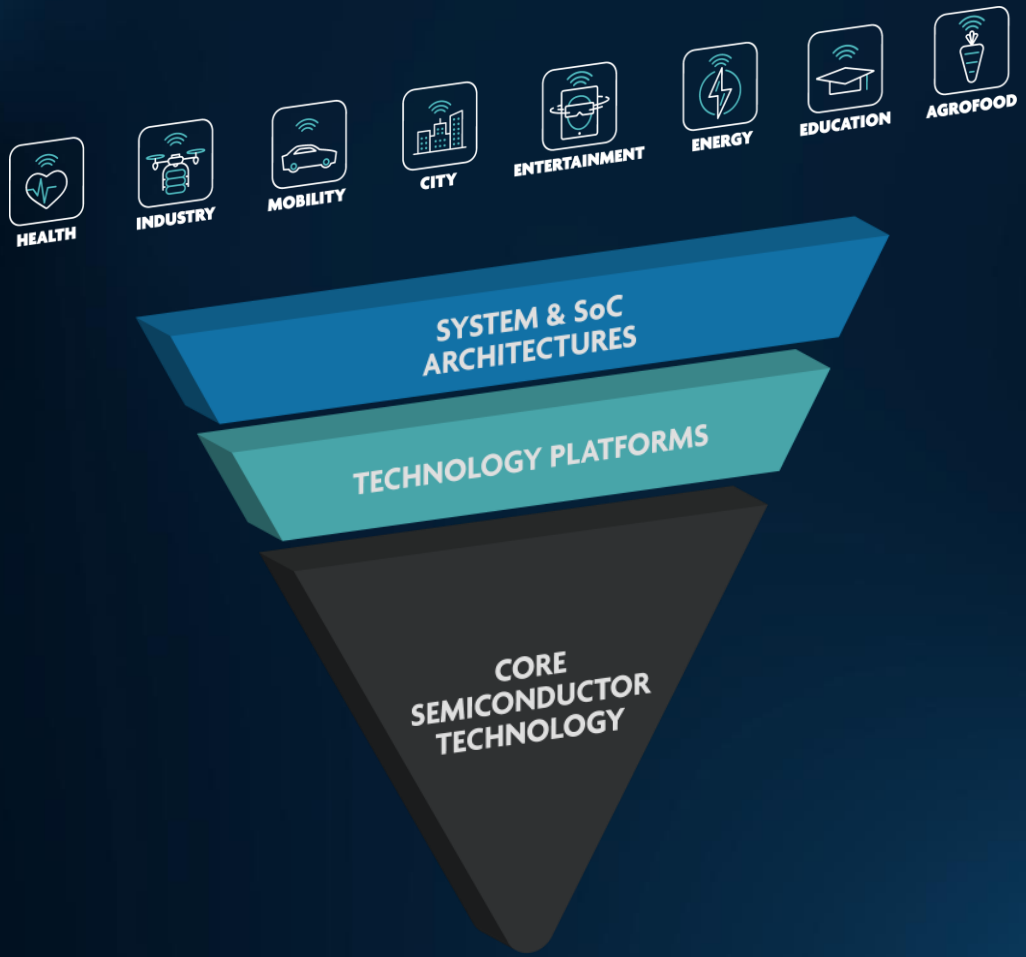
HEALTH
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SYSTEM & SoC ARCHITECTURES
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CORE SEMICONDUCTOR TECHNOLOGY

Imec UK

- Founded August 2022 to access UK design expertise
- Currently a team of 9 circuit and system researchers with experience of cross stack projects from device through circuits and system to algorithms
- Active projects in optical & wireless comms, novel memory, computer architecture
- Now collaborating with UK academia through co-funded & co-supervised PhDs
- Keen to discuss other UK collaboration models

- We're hiring!
  - https://www.imec-int.com/en/work-at-imec/job-opportunities

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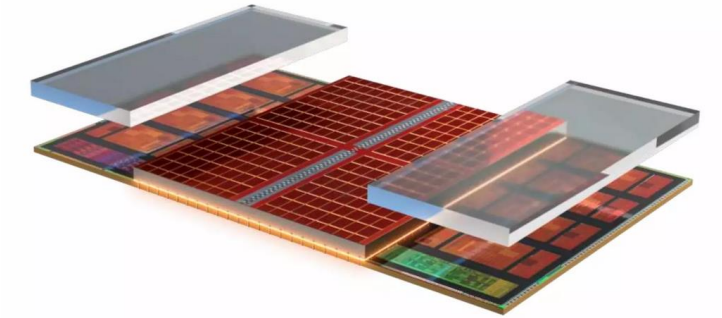
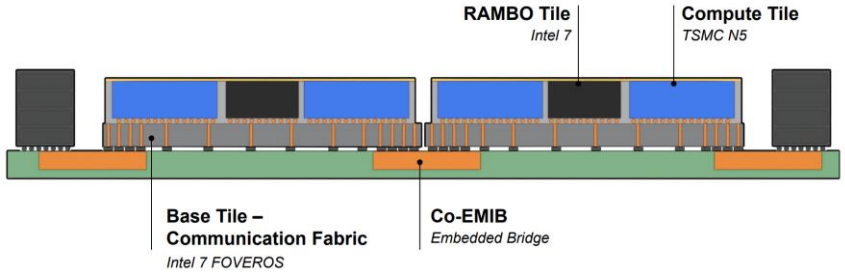
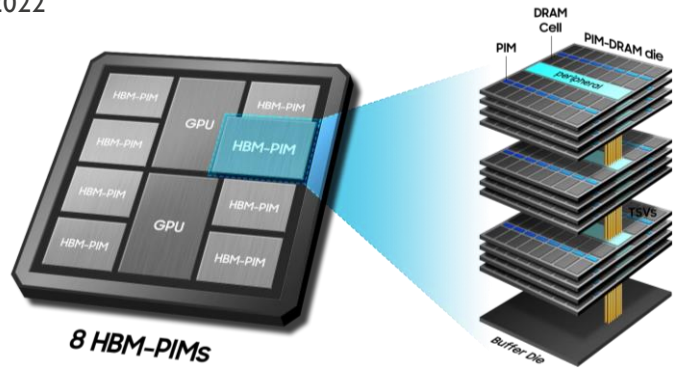
Many innovations hitting today's SoC products



Source: AMD ISSCC 2022



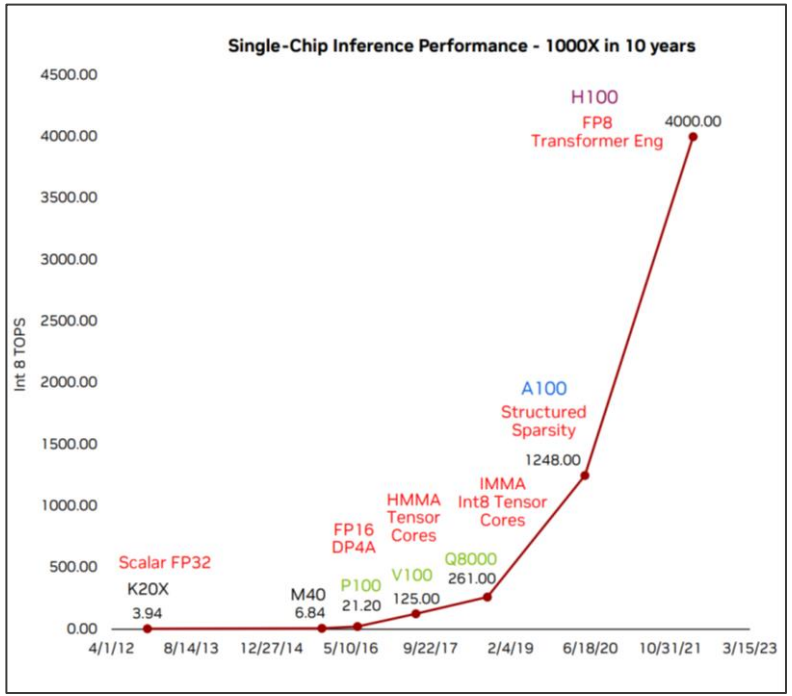
Source: Intel ISSCC 2022



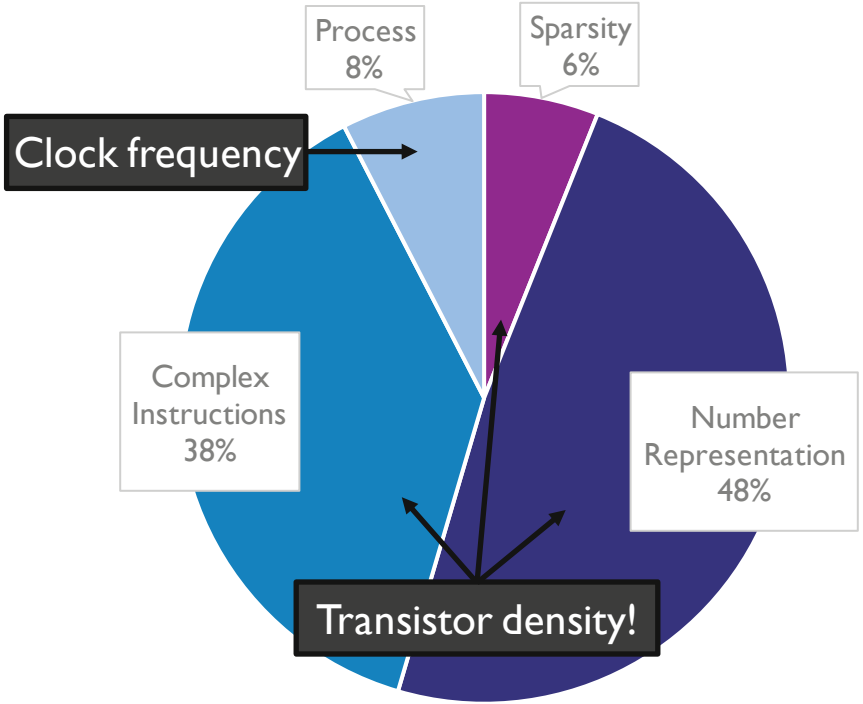
Source: Samsung ISSCC 2021

Transistor density = specialism = performance

Density scaling enables architects to boost performance at iso-frequency

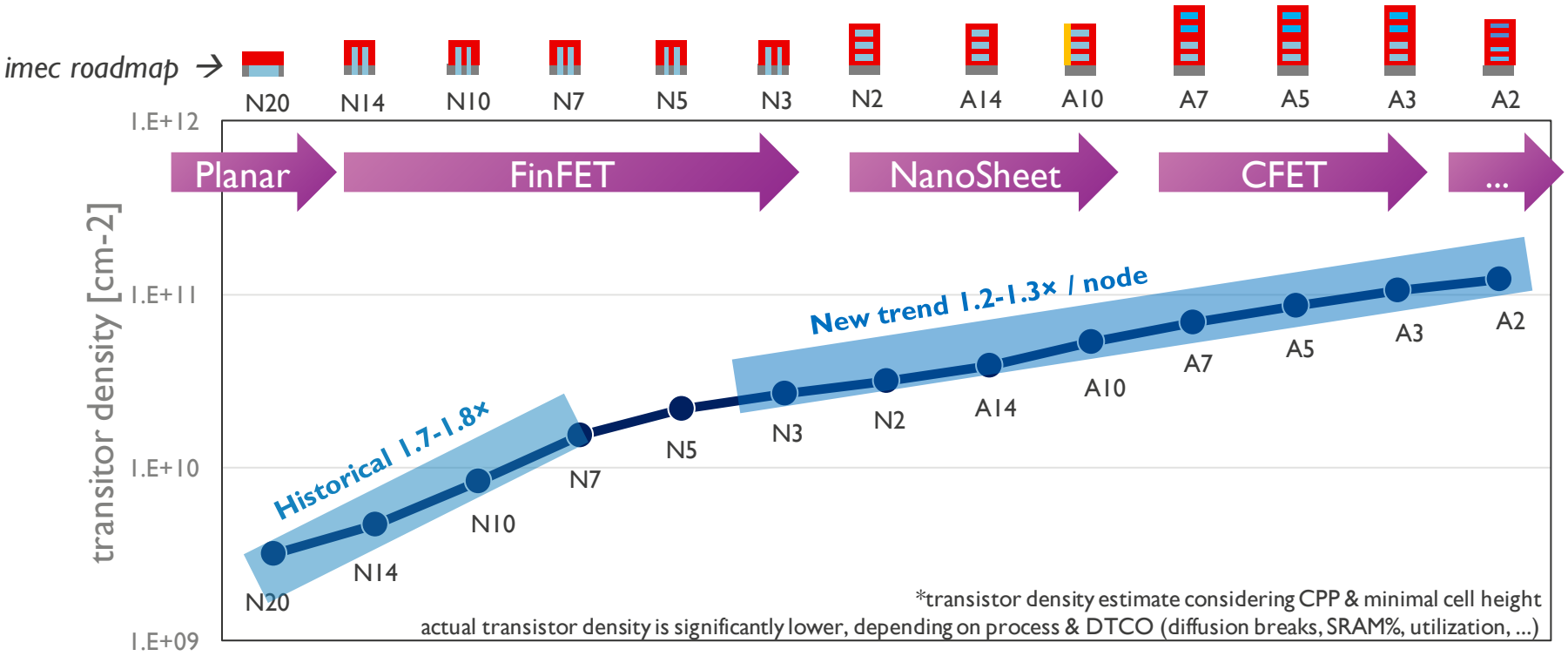


[Bill Dally, Nvidia, Hot Chips 2023]



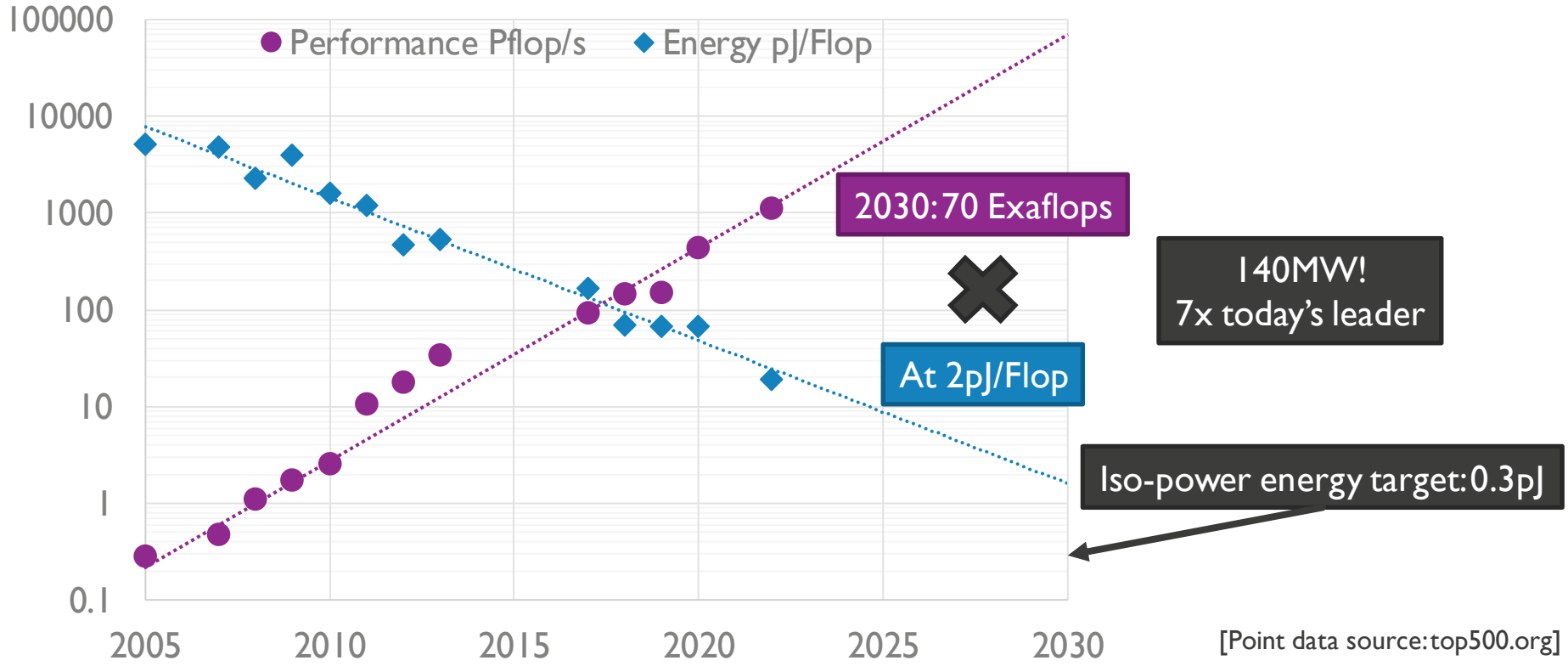
But transistor density scaling projected to slow down

CPP x cell height scaling stalling



The world's fastest supercomputers 2005-2030

Efficiency falling behind continued performance improvements



[Point data source: top500.org]

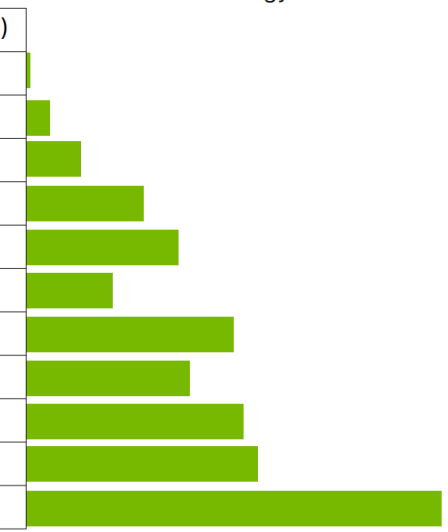
FLOP = floating point operation (64b in this case)

We have an open benchmarking issue

Imec can fill this gap – N2 P-PDK and beyond

Relative Energy Cost

Operation:	Energy (pJ)
8b Add	0.03
16b Add	0.05
32b Add	0.1
16b FP Add	0.4
32b FP Add	0.9
8b Mult	0.2
32b Mult	3.1
16b FP Mult	1.1
32b FP Mult	3.7
32b SRAM Read (8KB)	5
32b DRAM Read	640



**Energy numbers from 45nm process

[Bill Dally, Nvidia, Hot Chips 2023]

		Picojoules per Operation			Ratio
Operation		N45	N7	N2 (imec)	N2/N7
Add	IEEE FP32	0.9	0.38	0.346	91%
	IEEE FP16	0.4	0.16	0.187	117%
	BFloat16		0.11	0.146	133%
	Int32	0.1	0.03	0.019	63%
	Int8	0.03	0.007	0.003	45%
Multiply	IEEE FP32	3.7	1.31	0.734	56%
	IEEE FP16	1.1	0.34	0.215	63%
	BFloat16		0.21	0.096	46%
	Int32	3.1	1.48	0.562	38%
	Int8	0.2	0.07	0.023	33%

30x

100x

20x

30x

[imec paper under review]

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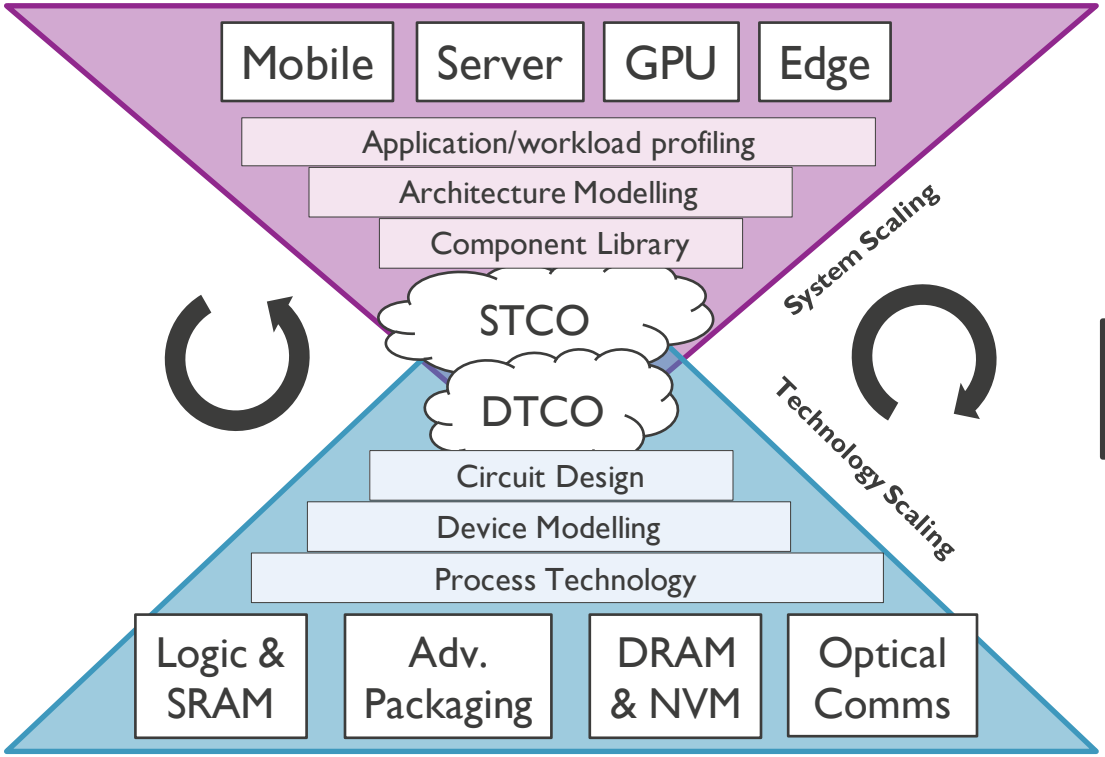
Imec's STCO vision

The future of compute depends upon cross-stack codesign with technology innovations

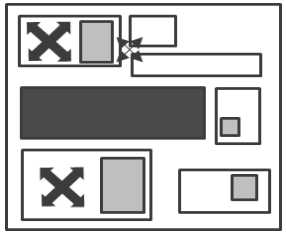
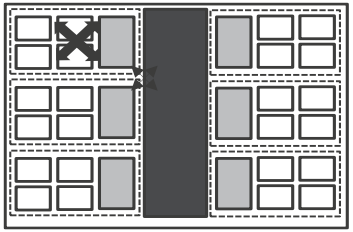
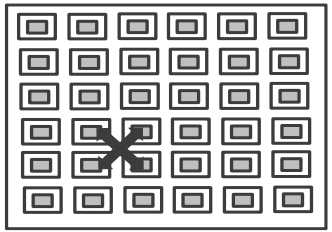
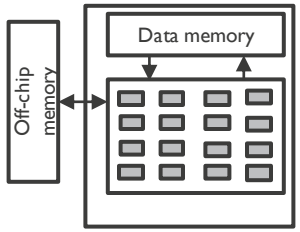
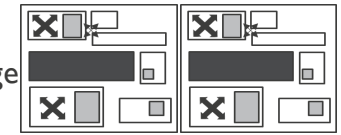
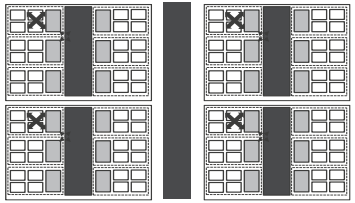
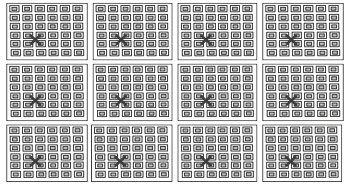
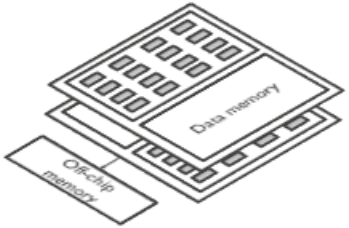


What is the right memory for on-chip weights?

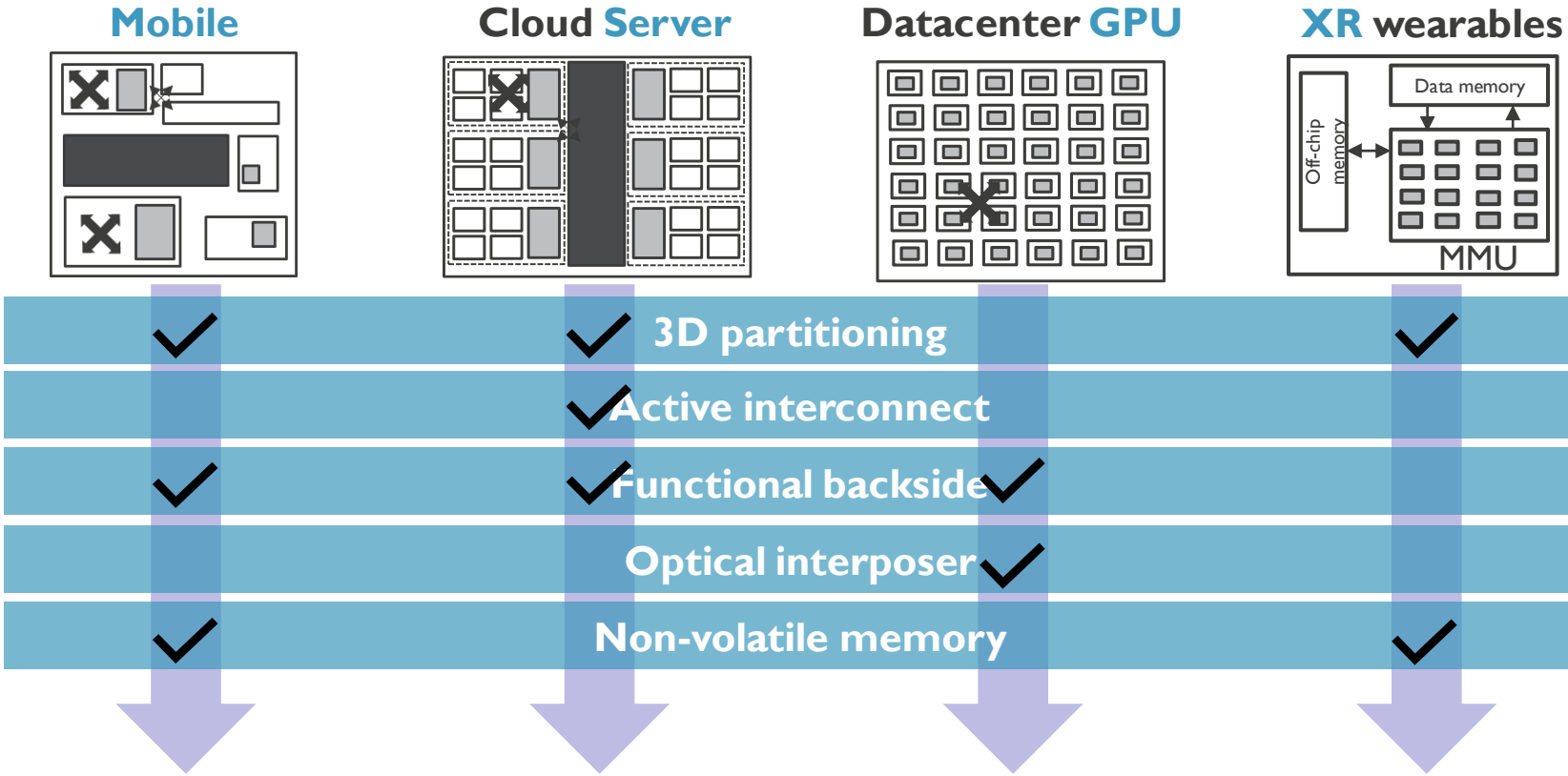
How do we co-design for 10x wearable AI efficiency?

Is this magnetic memory beneficial for AI?

Divergent SoC directions

	Mobile	Cloud Server	Datacenter GPU	XR Wearables
Arch				
Package				
Power	Battery →	TCO & CO_2 →	Scale Up ↗	Form Factor ↘

Technology choices are application dependent



Benefits depend on application benchmark

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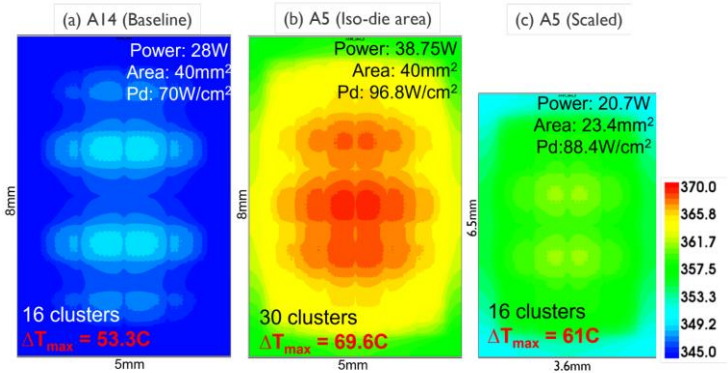
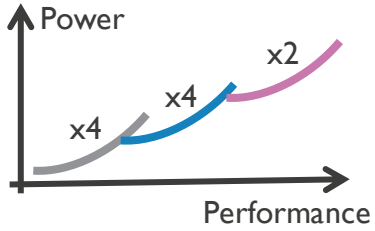
How much does thermal management limit future performance?

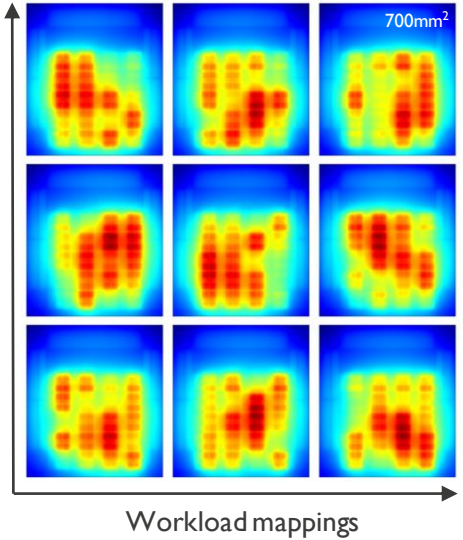
Output: thermally aware CMOS roadmap enhanced for performance at fixed TDP

Process	Device	Circuit	Component	Architecture	Workload

PDK to P&R to package ⟷ DVFS characteristics ⟷ SoC power model







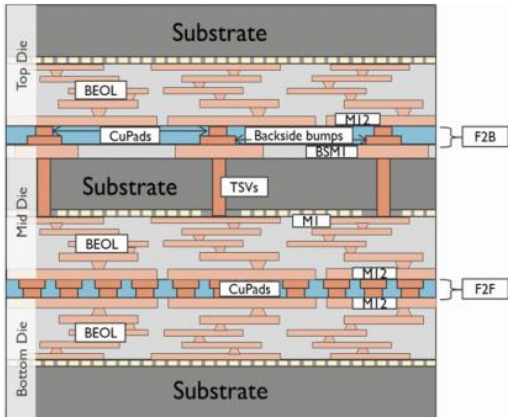
[Towards Chip-Package-System Co-optimization of Thermally-limited System-On-Chips, S Mishra et al, 2023 IEEE International Reliability Physics Symposium, 2023]

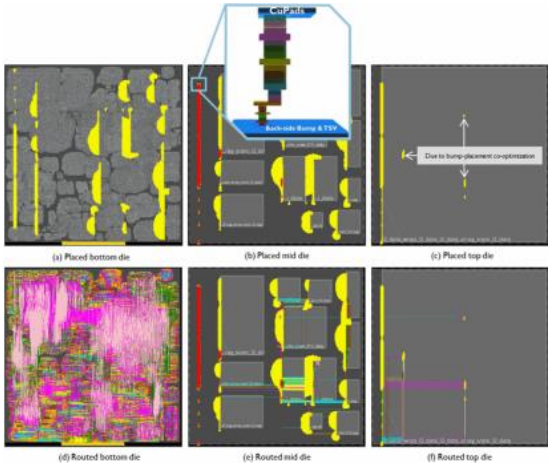
How can we get the most from 3D SoCs?

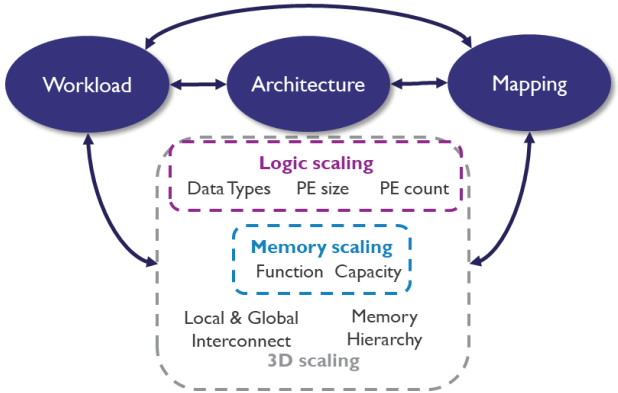
Output: aligned usage model for 3D pitch, CMOS and embedded memory roadmaps

Process	Device	Circuit	Component	Architecture	Workload

Pitches for TSVs and hybrid bonds ⟷ EDA enablement and P&R studies ⟶ 3D native accelerators







[M. Naeim *et al.*, "Design Enablement of 3-Dies Stacked 3D-ICs Using Fine-Pitch Hybrid-Bonding and TSVs," *2023 IEEE International 3D Systems Integration Conference*]

Conclusion

- Imec is a semiconductor technology institute with growing presence in the UK
- CMOS logic density scaling continues but we have many system problems to tackle
- Imec's STCO research enriches future technology roadmaps with system context
- We will increasingly rely on STCO to extend Moore's Law
  - And need more UK designers to get involved in technology research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