## **Evolution and Future of Embedding Technology**

#### **Dr. Andreas Ostmann**

Fraunhofer IZM, Berlin

Gustav-Meyer-Allee 25, 13355 Berlin, Germany email: andreas.ostmann@izm.fraunhofer.de





### **Outline**

- Past
- Presence
- Future
  - ... of Embedded Device Technology





## Past





## **Basic Embedding Concept**

#### **Conventional**

SMD, Wirebond, Flip Chip

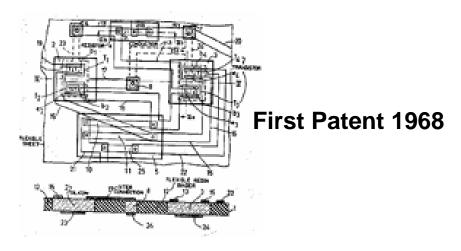
#### **Embedding**







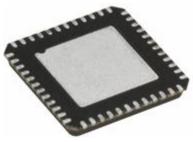
- → components are located on the surface of a substrate
- → components are inside a substrate



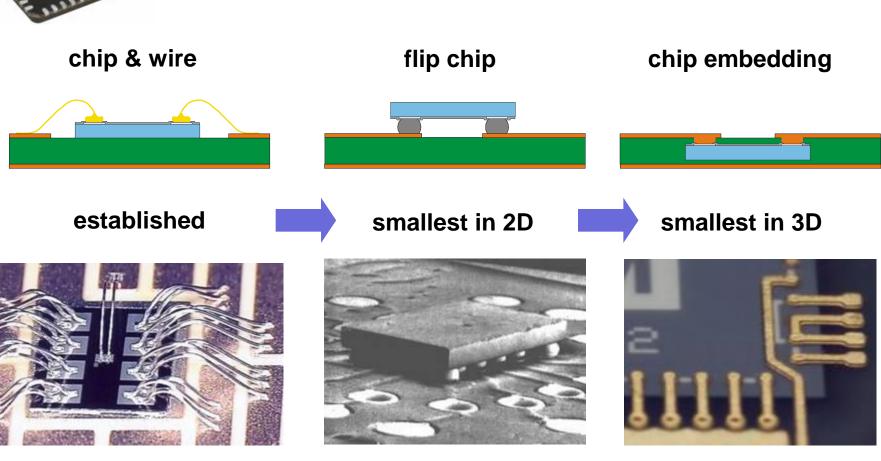




## **Basic Embedding Concept**



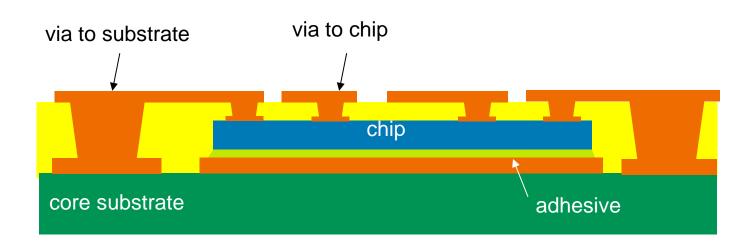
First level chip interconnection technologies inside a package:







## Why Embedding Is a Great Idea



#### **Features**

- chip embedded in planar substrate
- direct Cu contact to chip
- no wires, no solder bumps
- very thin package
- power and logic integration possible

#### **Advantages**

- reduced package thickness
- 3D stacking capability
- improved electrical performance
- good thermal performance
- EMI shielding capability





## Why Embedding Will Never Work

- Si and PCB have different CTEs
- this will not be reliable
- no repair is possible
- PCB yield is too low
- PCB manufacturers can never handle chips
- this does not fit to existing value chain

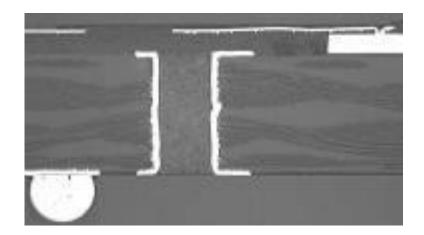




## **Early Approaches for Chip Embedding**

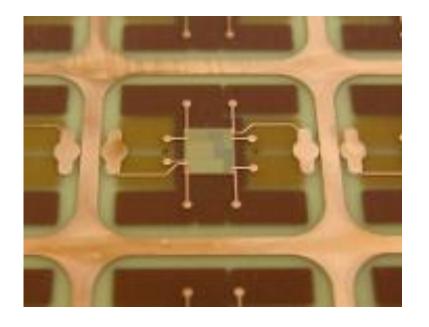
#### Organisations (before 2000)

- General Electrics
- Hofmann Leiterplatten
- TU Helsinki
- Fraunhofer IZM / TU Berlin



### **R&D Projects (selection)**

- Chip in Polymer (DE)
- HIDING DIES (EU)
- TIPS (EU)
- HERMES (EU)





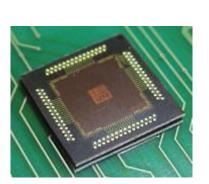


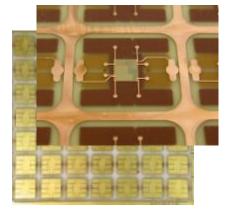
## **Embedding** –Technology Evolution

Chip Embedding in organic substrates

→ use of PCB technology & material

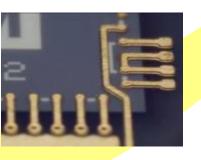














**First Patent** 

1968

2000

**Production Demos** 

**Production** 

**Basic R&D** 

2005

2015





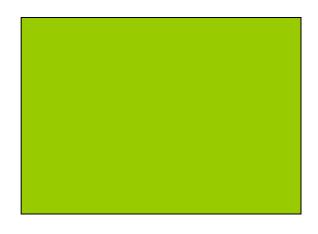
## Presence





## **Embedding Technologies** – Status Today

Embedding in PCB



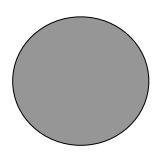


Embedding of bare dies



Embedding of soldered SMDs





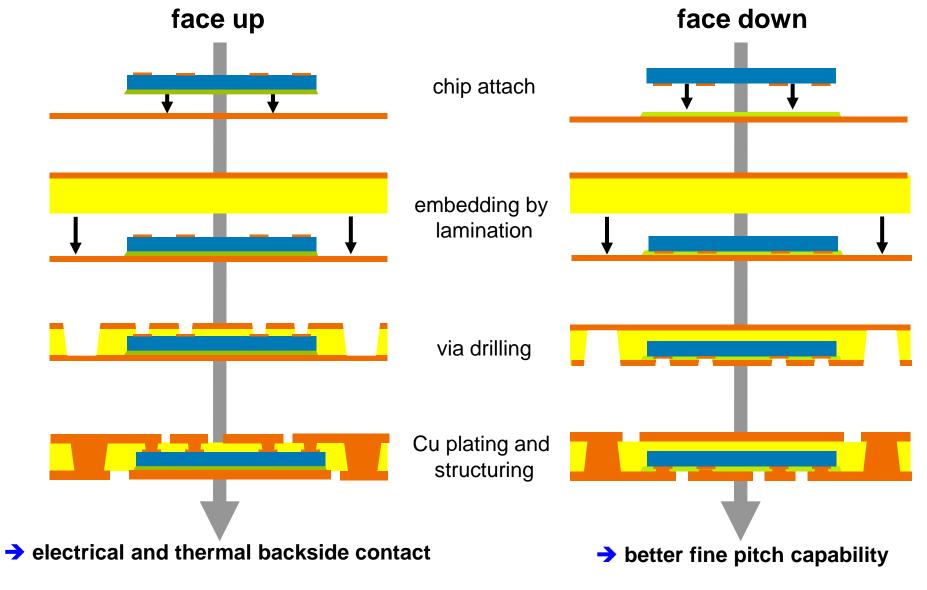


- -Embedding by molding
- -Thin film RDL layers





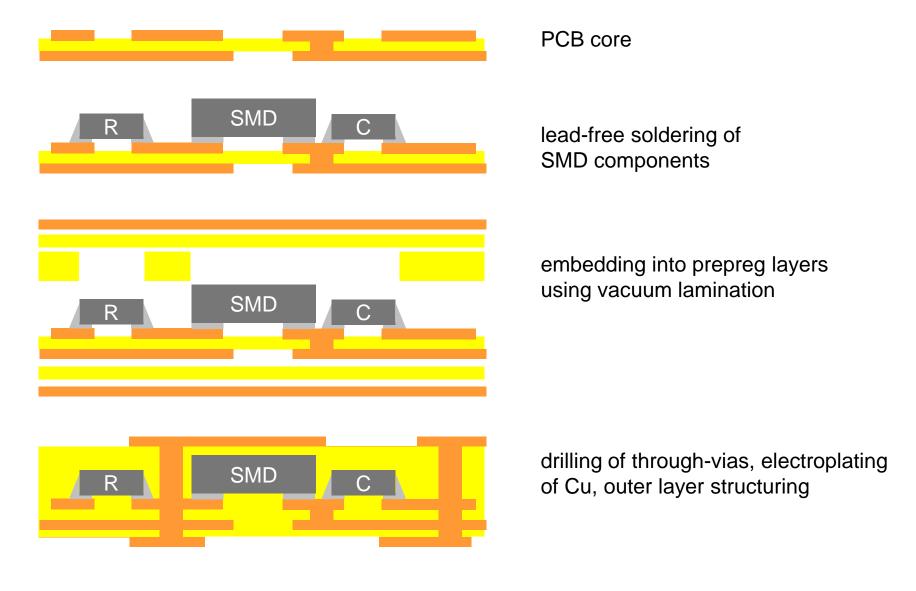
## **Processes** – Embedding Bare Dies







## **Processes** – Embedding Packaged Components







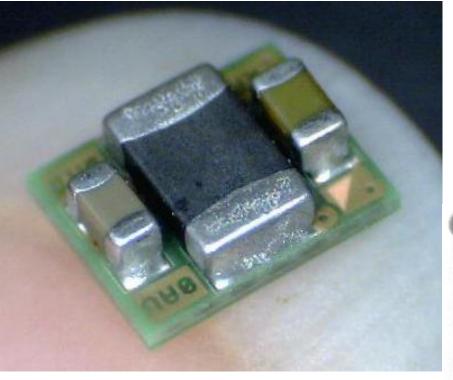
#### **Production** – AT&S



#### MicroSIP Technology - TPS82671, TPS82675

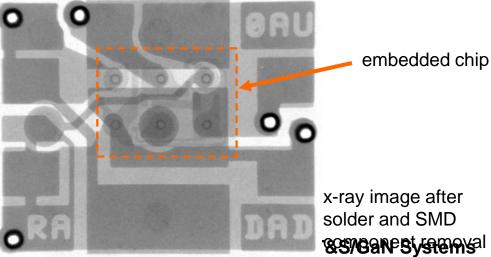
→ embedded chips in SIP substrates

- → product available since 2010
- → manufacturing by AT&S





cross-section of package











### **Production** – AT&S





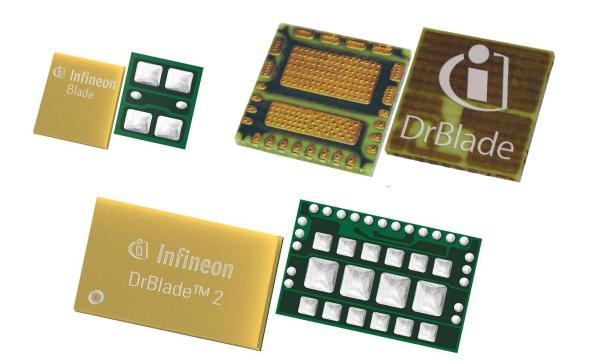


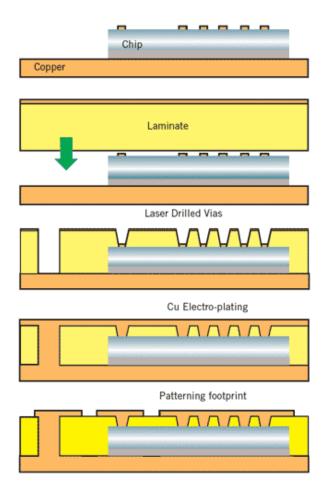


#### **Production** - Infineon

#### **BLADE Packages**

- infineon
- embedded MOSFET / Driver
- manufacturing on PCB format





Licensing and process transfer from Fraunhofer IZM





#### **Production** – Current Status

- > AT&S several products in volume
- ➤ Infineon Blade Packages
- > TDK&EPCOS SESUB Technology
- ➤ ASE a-EASI Technology Packaging Service
- > Würth Electronics different technologies in series
- Hofmann Leiterplatten small volume and prototypes
- Schweizer Electrónics Ready for volume production





## **R&D** - Fraunhofer IZM Substrate Integration Line

#### **Placement**



#### Accuracy



Lamination



#### **Laser Drilling**



Datacon evo/ ASM Siplace CA3



Mahr OMS 600/ IMPEX proX3



Lauffer/ Bürkle



Siemens Microbeam/ Schmoll Picodrill with HYPER RAPID 50

#### $\Rightarrow$

#### Mech. Drilling



**Cu Plating** 



**Imaging** 



**Etching** 



Schmoll MX1



Ramgraber automatic plating line



Orbotech
Paragon Ultra 200



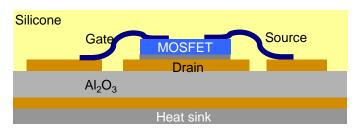
**Schmid** 





#### **R&D** - Embedded Power Modules

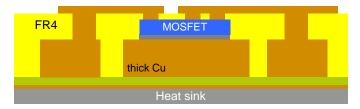
#### traditional power module



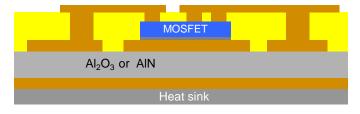




#### embedding on PCB substrate



#### embedding on ceramic substrate



- production panel 610x456 mm² (18"x24")
- isolation and thermal conduction by high-λ laminate
- → module with low to medium power density → modules with high power density

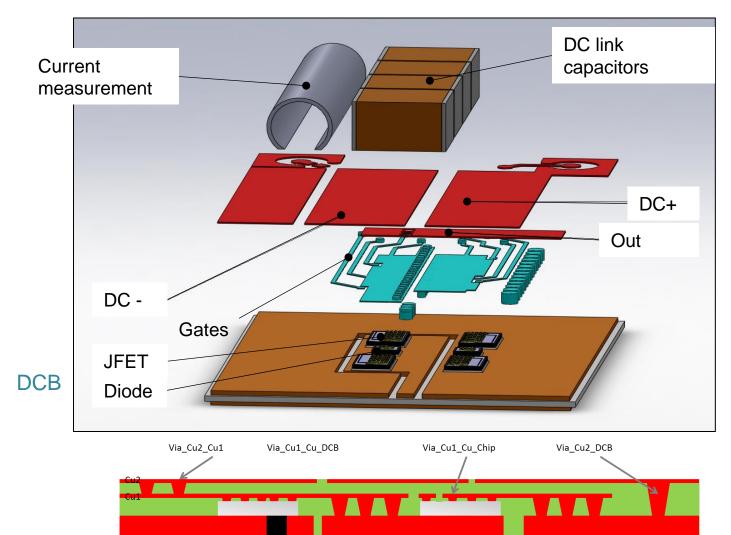
- production panel 125x175 mm² (5"x7")
- isolation and thermal conduction by Al<sub>2</sub>O<sub>3</sub> or AlN DCB





## **R&D** - Ultra Low Inductance Package for SiC



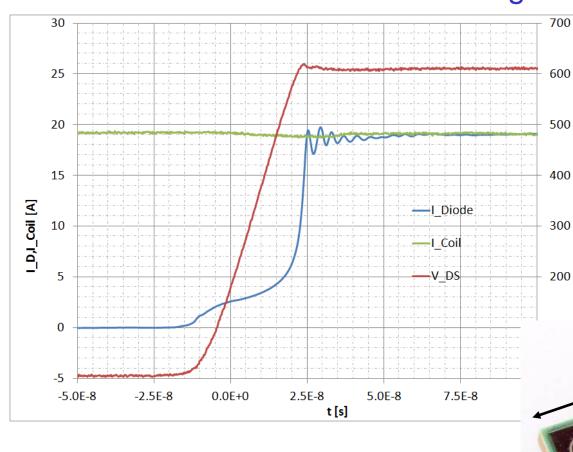


- Full bus bar structure using PCB Process on a DBC
- DC capacitors on the module
- DC link current measurement included





## R&D - Ultra Low Inductance Package for SiC



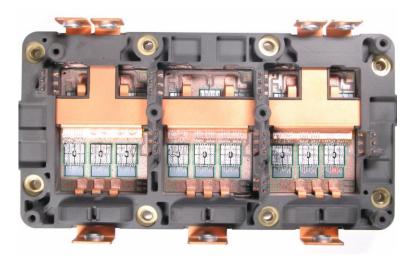
- Switch off at 20 A: Voltage slope 19 V/ns current slope max. 4 A/ns (50% to 90%)
- Low overshot (appr. 10 V)
- very little ringing (frequency 240 MHz)

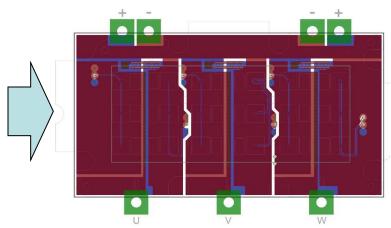
3 cm

\*\*\*\*\*\*\*

0.8 nH DC-link inductance (comparison: wirebond 10-20 nH)

Development of planar power modules for 50 kW motor inverter





#### **Features**

- Reduction of height by 10 mm
- Cost efficient production without expensive packaging
- Integration of control electronics
- Capability for double-side (water) cooling

Project Partners
The project consortium offers
research activities through the
whole supply chain:







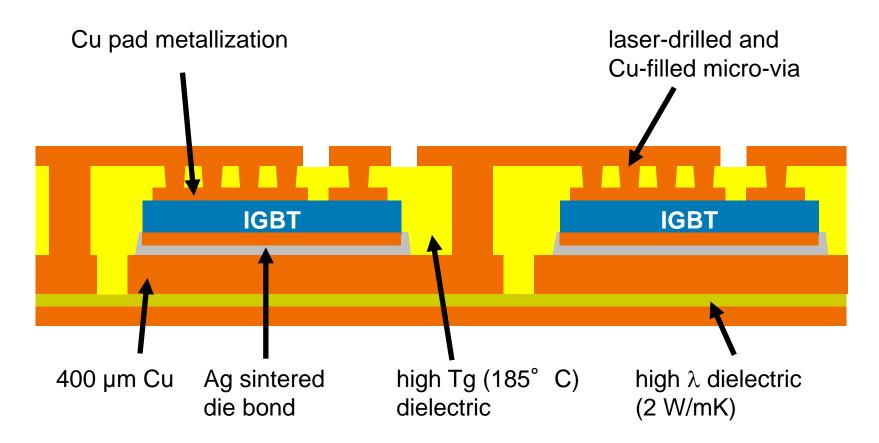
System Design:



Heraeus





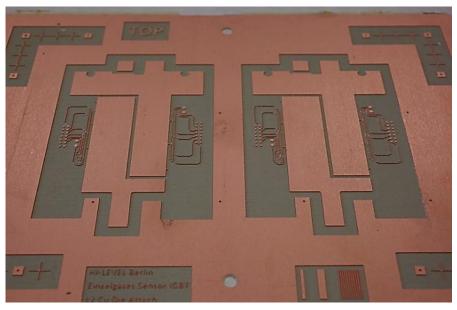


#### Topics of current investigations

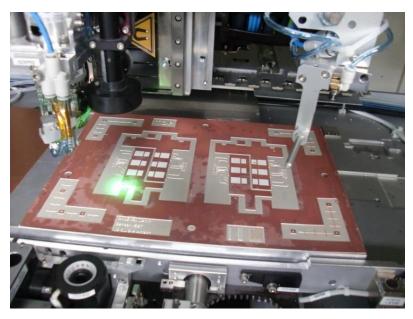
- pressure-less / low-pressure sintering on large panels
- application of 5 µm Cu bumps on thin IGBT wafers
- high voltage isolation of thermally conductive dielectric



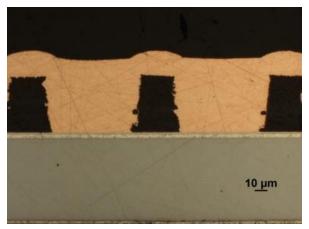




400 µm Cu on thermal laminate substrate.



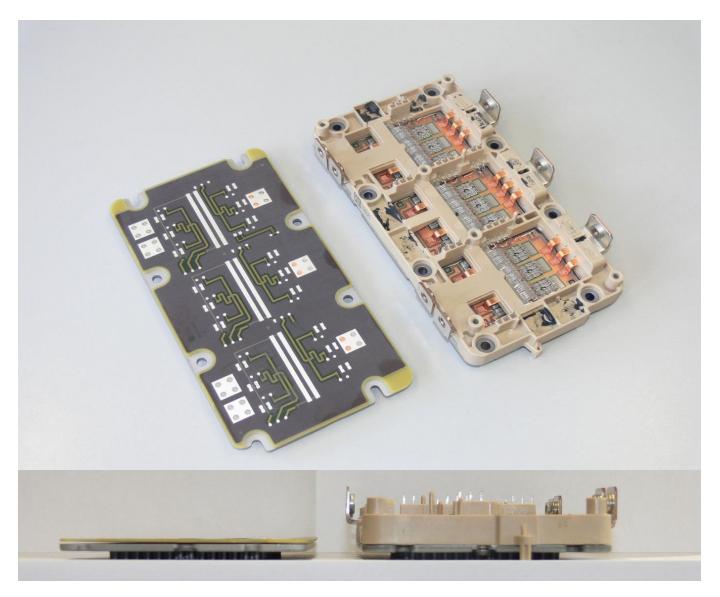
Die bonding on sinter paste.



Microvias on top of IGBT











### **R&D** - Project EmPower



- Embedded power components for electric vehicle applications
- Started in September 2013, duration 3 years
- Project goals:
  - Industrialize double sided copper plating on wafer level
  - Industrialize next generation automotive power modules
- Benefits:
  - High performance power products with embedded MOSFET, IGBT, GaN, etc.
  - Smallest form factor power supplies
- Partners:



















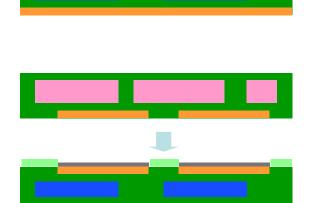


## **R&D** - Project EmPower

#### Stacking by combined sinter/lamination → Process Flow

- Stacking of Functional Layers by combined sinter/lamination technology
  - stencil printing of Ag sinter paste on Functional Layer, paste drying
  - 2. lay-up of prepreg sheet with opening for paste locations

3. lay-up of 2. Functional Layer on top, vacuum lamination at 3 MPa, 10 min./230 °C, 60 min./200 °C



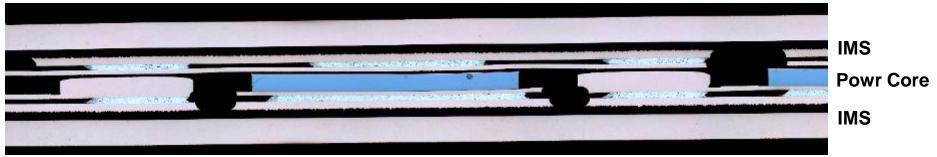
Result: a monolithic stack, thermally and electrically interconnected by high-reliable Ag joints, all gaps are filled by an isolating dielectric



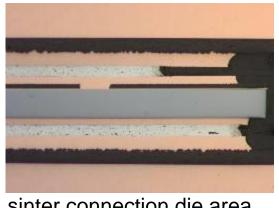


## **R&D** - Project EmPower

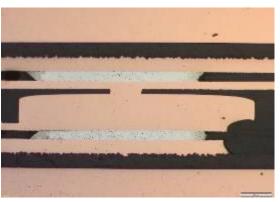




cross section of IMS/power core/IMS sinter interconnects



sinter connection die area



sinter connection copper inlay area

#### → no large voids in Ag sinter interconnects





Motivation: to demonstrate the realization of a complex module

using Panel Level Packaging with embedded components

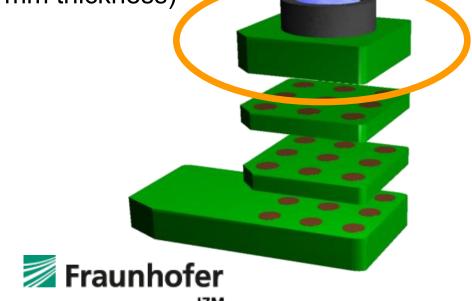
Demonstrator: a stand-alone Modular Micro Camera (MoMiCa)

with integrated real-time image processing

Technology: SMD component embedding on PCB panel format

Components: commercially available components

in small packages (≤ 1 mm thickness)





### **System component selection**

- CV2201 image cognition processor from CogniVue
- COGNIVUE®

  Innovating With Vision

- 32 bit ARM9 processor core. 350 MHz
- 96 parallel Computational Units
- 16 MByte stacked DDR SDRAM
- 15 30 frames per second rwal time image processing
- 3 MPixel CMOS image sensor from Omnivision, CSP wizh solder balls
- 16 MByte flash memory for firmware storage
- USB 2.0 module interface

#### **Software (module firmware)**

Nucleus 32 bit RTOS (real time operation system) from Mentor



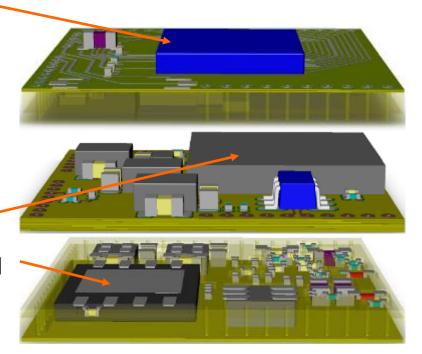


#### 13 Components on top

- 3 MPixel Image Sensor Omnivision 3642
- lens CMT746 + lens holder
- 7 capacitors (0201)
- 1 resistor (0201)
- 1 inductor (0603)
- 1 microswitch

#### 74 Embedded Components

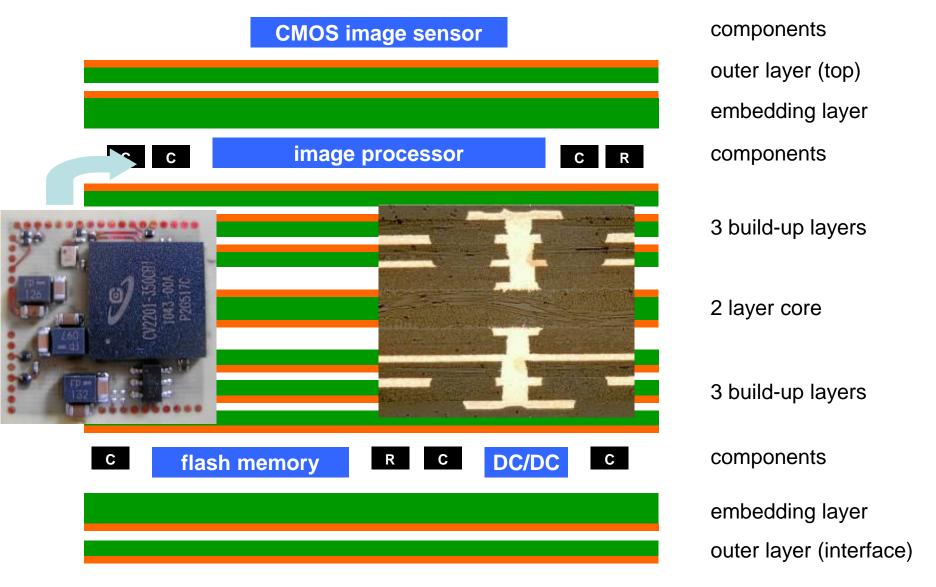
- 32 bit microcontroller with image sensor interface (CogniVue CV2201 BGA 236)
- 256 Mbit Flash Memory (Macronix 8WSON
- MOSFET switch (IRF SOIC)
- USB ESD protection (NXP SOT457)
- 5 DC/DC-converters (Murata)
- oscillator 24 MHz (NXP
- 2 LEDs (0402)
- 34 capacitors (0201, 0603)
- 25 resistors (0201)
- 3 inductors (0603)



→ 13 active components from 8 different manufacturers



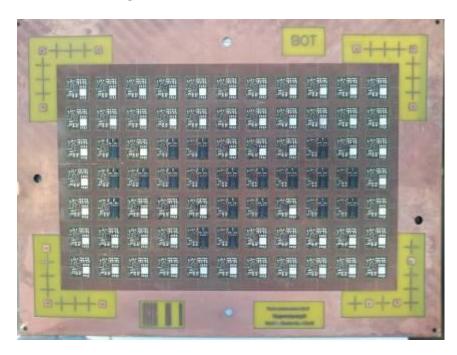






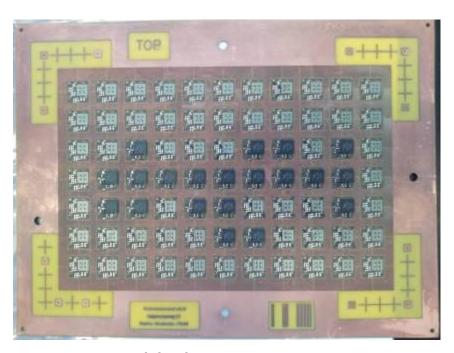


- manufacturing on quarter format (12" x 9")
- 77 modules per panel (only partially with components)
- double-side component assembly on PCB core
- embedding by prepreg lamination
- assembly of image sensor on top
- testing on panel-level



assembled components on bottom PCB core





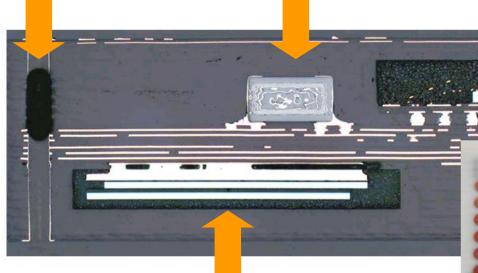
assembled components on top PCB core



through hole

capacitor

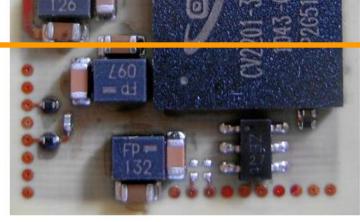
CogniVue Image Procesor 3 stacked chips in a package



Macronics Flash Memory 2 stacked chips in a package

### **Camera Geometry**

- size 16 x 16 mm
- thickness w/o sensor 3.6 mm
- weight 2 g w/o lens

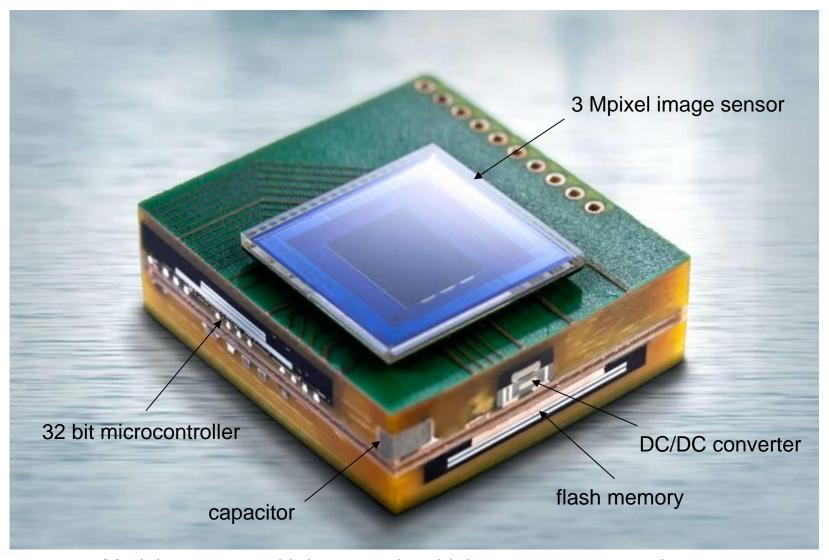






cross

section



Modular camera with integrated 32 bit image processor and memory





# Future





## **Electronic System - Quo Vadis?**



board from Zuse Z23 computer, 1963



SMD board with 01005 components, early 21. century

2000









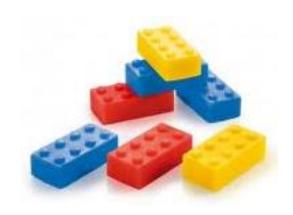
## **Electronic System - Quo Vadis?**



board from Zuse Z23 computer, 1963



SMD board with 01005 components, early 21. century



Modular Electronics?

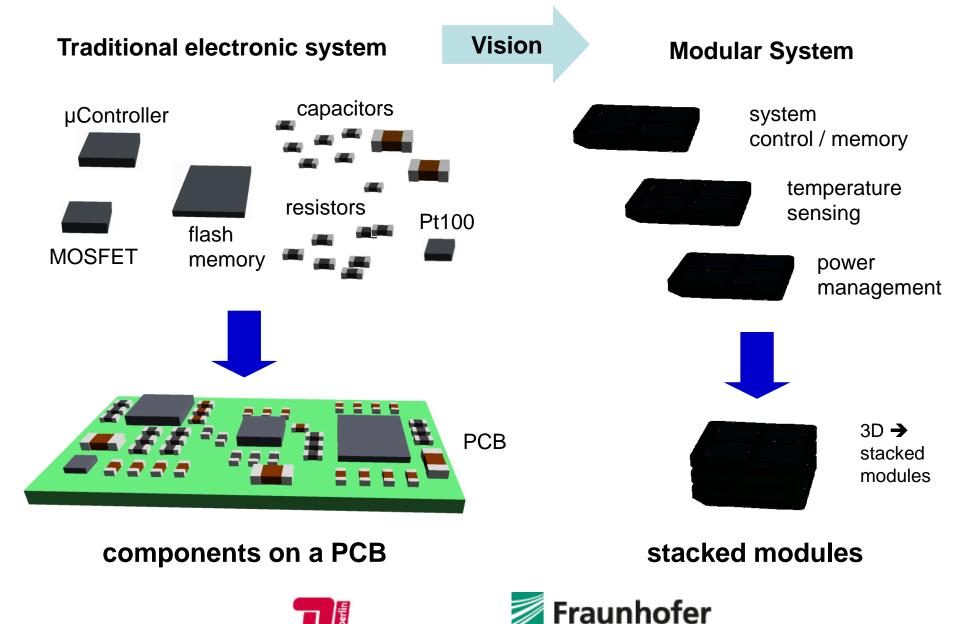


1950 2000 2050



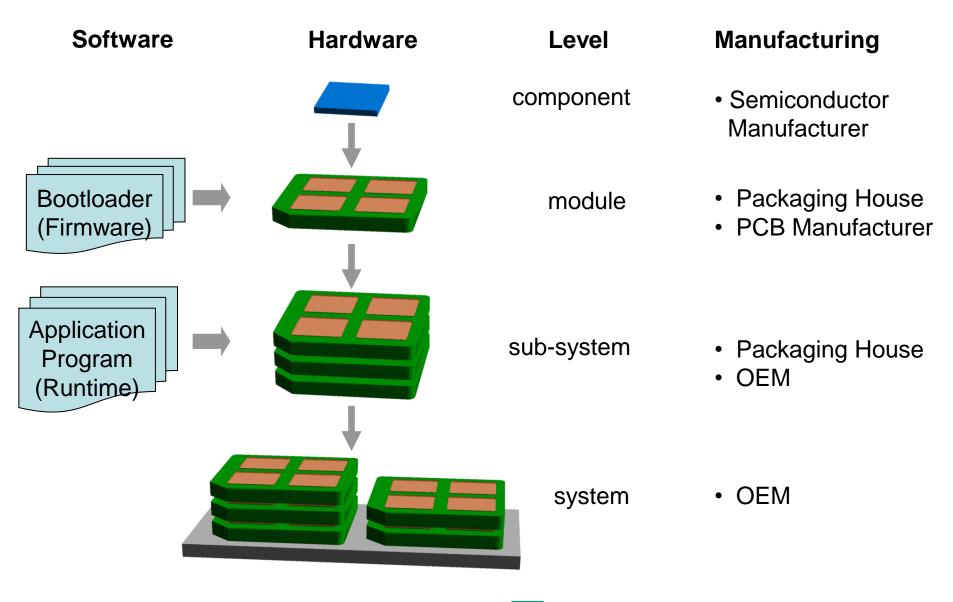


## **Modular Microelectronics** – Concept



IZM

## **Modular Microelectronics** – From Chip to System



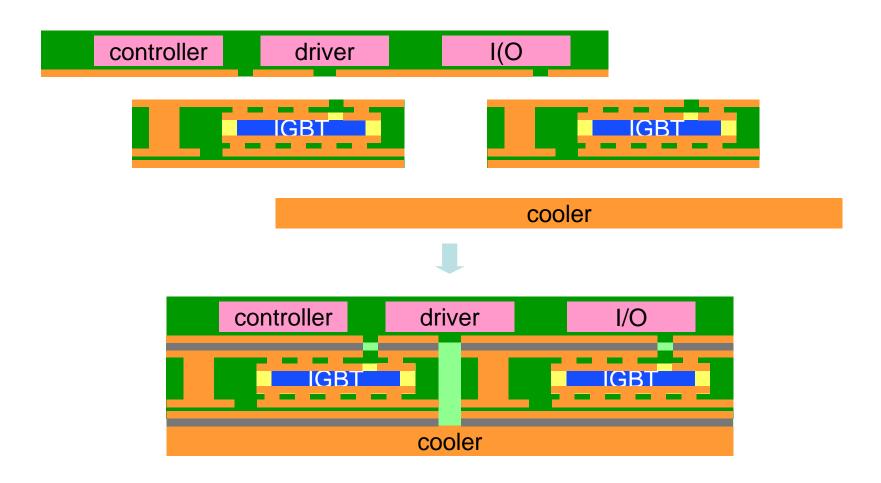




#### **Modular Power Electronics**

#### What is a Modular 3D Power Stack?

Stacking of Functional Layers by combined sinter/lamination technology





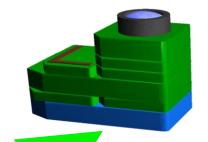


#### **Outlook**

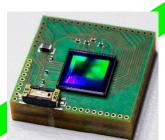
 Embedding technology opens a way over small and robust SiPs towards Modular Microelectronics

 Modular Microelectronics offer much shorter design cycle times

 It can simplify the realisation of complex systems by use of tested functions



Modular System Architecture



**Modular System Software** 

**Modular System** 

**Module Stacking** 



**Embedded SiP** 



**Embedding Technology** 













