3D Embedded Device Technology -

Technology Options for 3D Heterogeneous Integration

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Embedded Die Technology

Mitel Caldicot, 22 Sept 2016

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- Technologies
- Markets
- Who and What

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Covering the Bases

- Subscription Services
  - PCB Information Service
  - Flex & Flex Rigid Forecast Service
  - Compass Programme
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- Custom Programmes
- Custom Reports and Surveys

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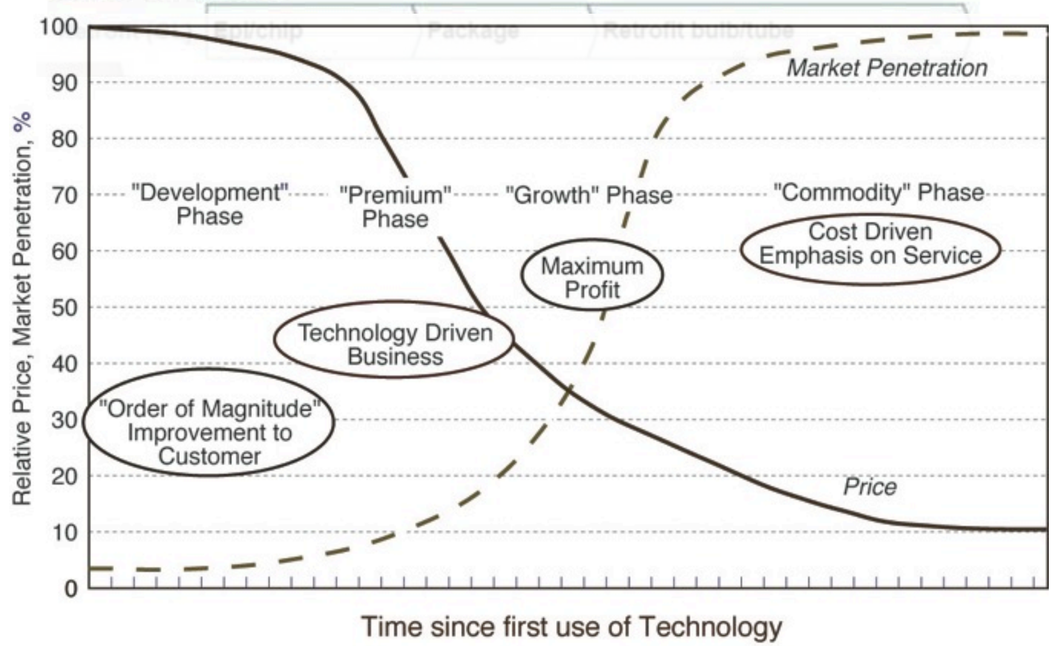
Core Competencies

- Helping One Industry Understand Another-
  - analyse, quantify, and qualify technologies and markets
- Value Chain Analysis-
  - components
  - substrates
  - systems
  - process equipment
  - materials
- "Innovation-to-Market"

Value Chain Analysis

	Upstream		Midstream		Downstream	
LED value chain	Epi/chip	Package	Module/light engine		Lighting fixture[1]	System/ solution[2]
Description	▪ Grow epi layer on sapphire wafer ▪ Structure and dope the sub-strate ▪ Cut the chip into dies	▪ Encapsulate and make contacts and primary optics ▪ Coat with phosphor (for white LED)	▪ Mount LED package(s) on a PCB ▪ Optimize in each appli-cation	▪ Integrate light modules with optics and thermal/power management components	▪ Combine mod-ule and ballast, with a fixture that plays a key role in the optics, and a heat sink	▪ Attach external control unit for fixtures ▪ Combine into system
Application specifics						



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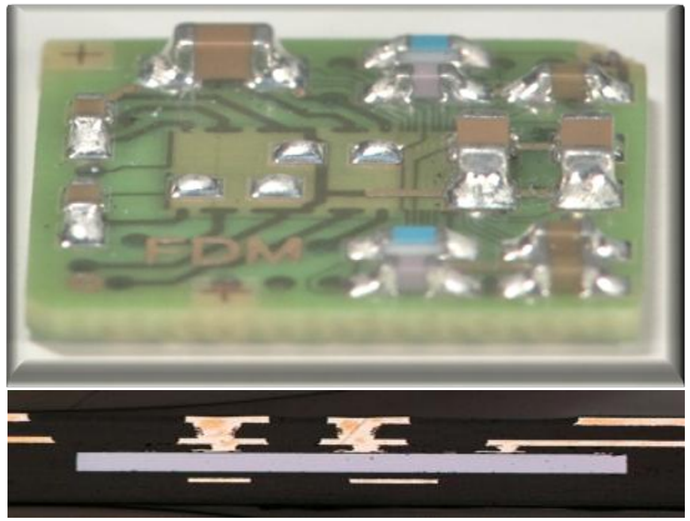
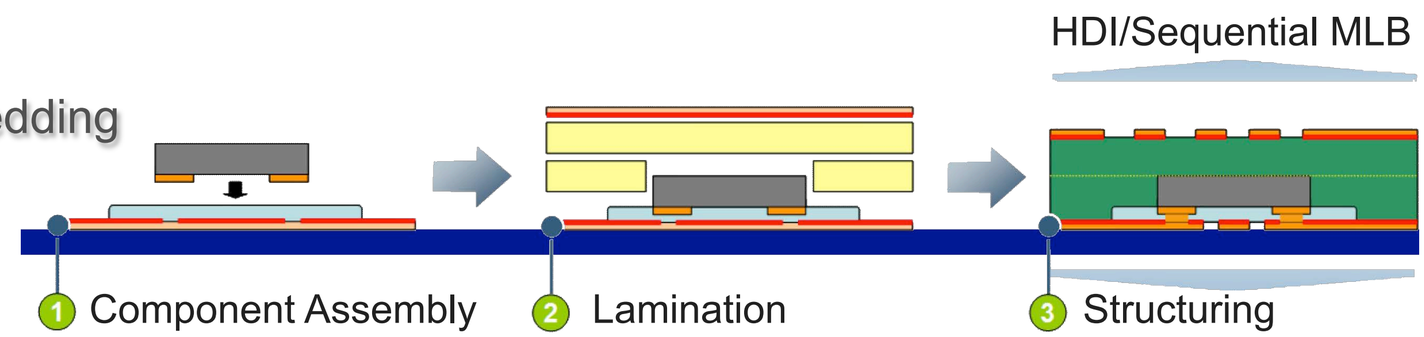
What is "Embedding"..?

- Embedding uses the space within an organic substrate for active and passive components
- Typically <400 embedded connections
- Embedding requires a new business model, integrating component, substrate, and assembly operations: the "Organic Fab"
- Components are embedded inside an organic substrate (PCB core) by combination of:
  - Component placement/bonding
  - Component encapsulation/embedding
  - Substrate buildup (lamination)
  - Circuitization
  - Final Finishing/Singulation/Test





source: AT&S, BPA Archives

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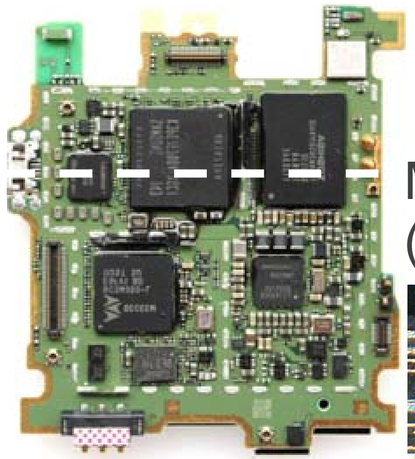
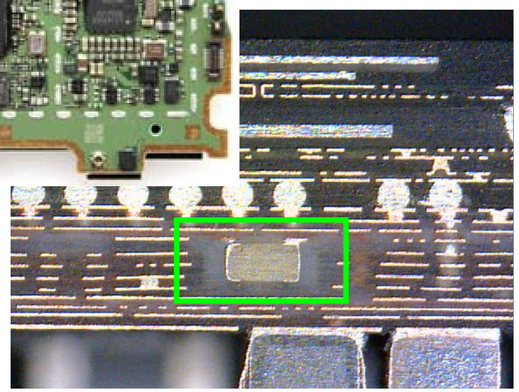
Hitting the Mainstream

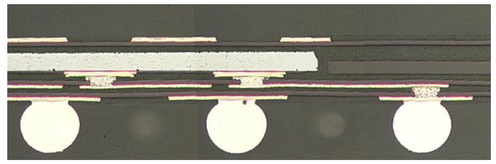
ECWC
13th Electronic Circuits World Convention
Nuremberg, Germany



Motherboard (DNP)

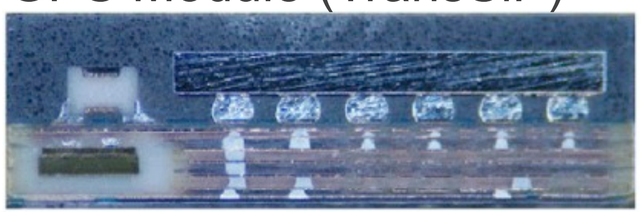


Package Substrate (Fujikura)

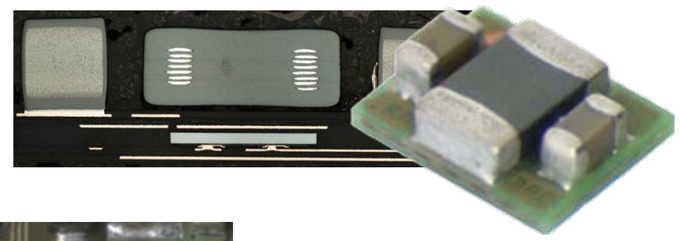


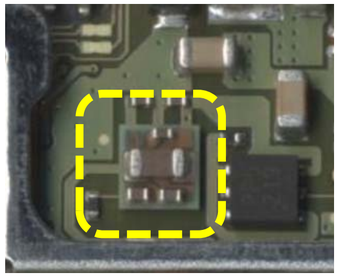
PMU (TDK)

GPS Module (TransSiP)



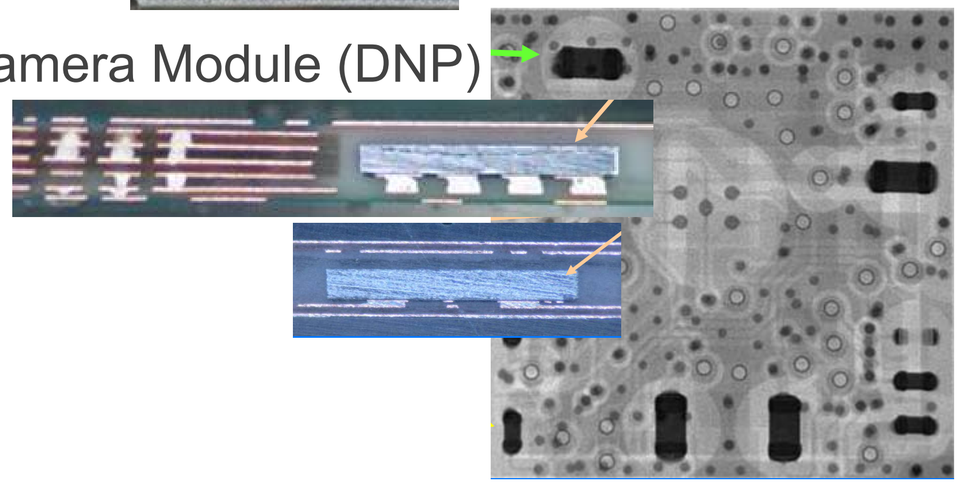
Buck Converter (TI)





Charge Pump Module (TDK)

Camera Module (DNP)



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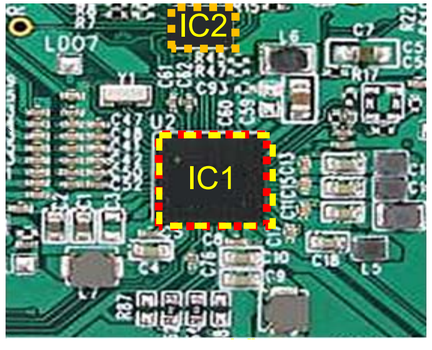
Kei-Haku-Tan-Sho (light-thin-short-small)

source: TDK

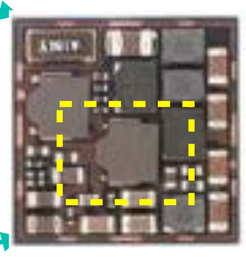
Smaller Size

Discrete Solution
350mm2

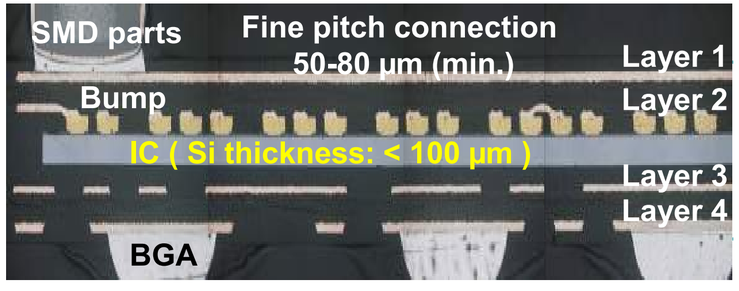


EDT Solution
120mm2

-65%

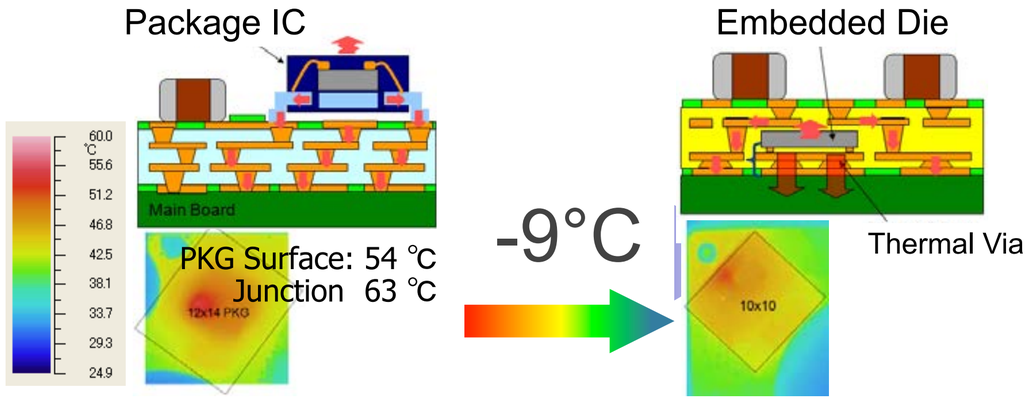


Reduced Skyline

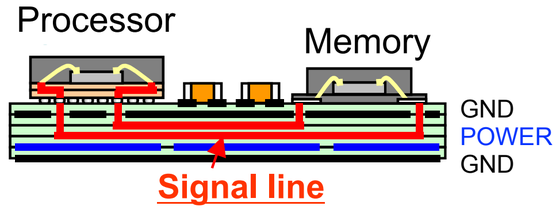


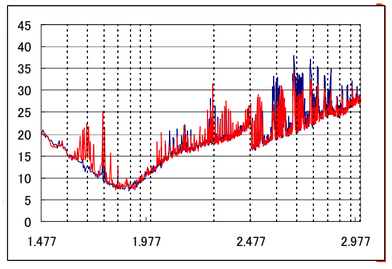
4L Substrate
including die
300µ

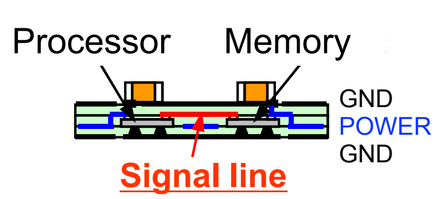
Improved Heat Dissipation

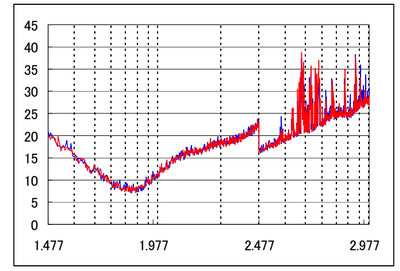


Low Noise









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Putting It All Together

Device I/O	Market 2015 (Bn Units)	Applications	Packaging Technology
> 400 Pins	~20.4[1]	• Application processor	• Substrate • PoP
– 400 Pins		• Baseband processor • Memory	• Hybrid (FOWLP, BGA...) • Embedded Die (development) • 3D Heterogeneous (future)
< 100 Pins	~15.7[2]	• RF, Audio, Video, MEMS, Sensor, Power Mgmt. • Resistor, capacitor, diode	• Wafer Level Package (WLP) • Embedded Die • 3D Heterogeneous

1) BPA, 2) TransSiP, Inc.

- Large Markets
- Need for Miniaturization
- Fastest Growing
- "More than Moore"

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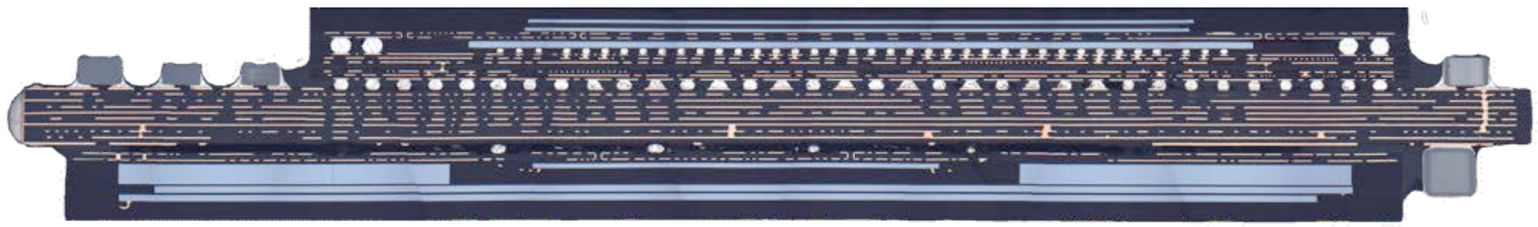
Where The Rubber Hits the Road

- "Processing"
  - active devices
  - more transistors per unit area = higher cost
  - 3D packaging = higher interconnect complexity



source: Chipworks

- "Experience"
  - actives, passives, MEMS, power, RF
  - non-digital functions = mixed component types
  - mixed signals / RF = layout, floorplan, parastics issues

source: Georgia Tech PRC

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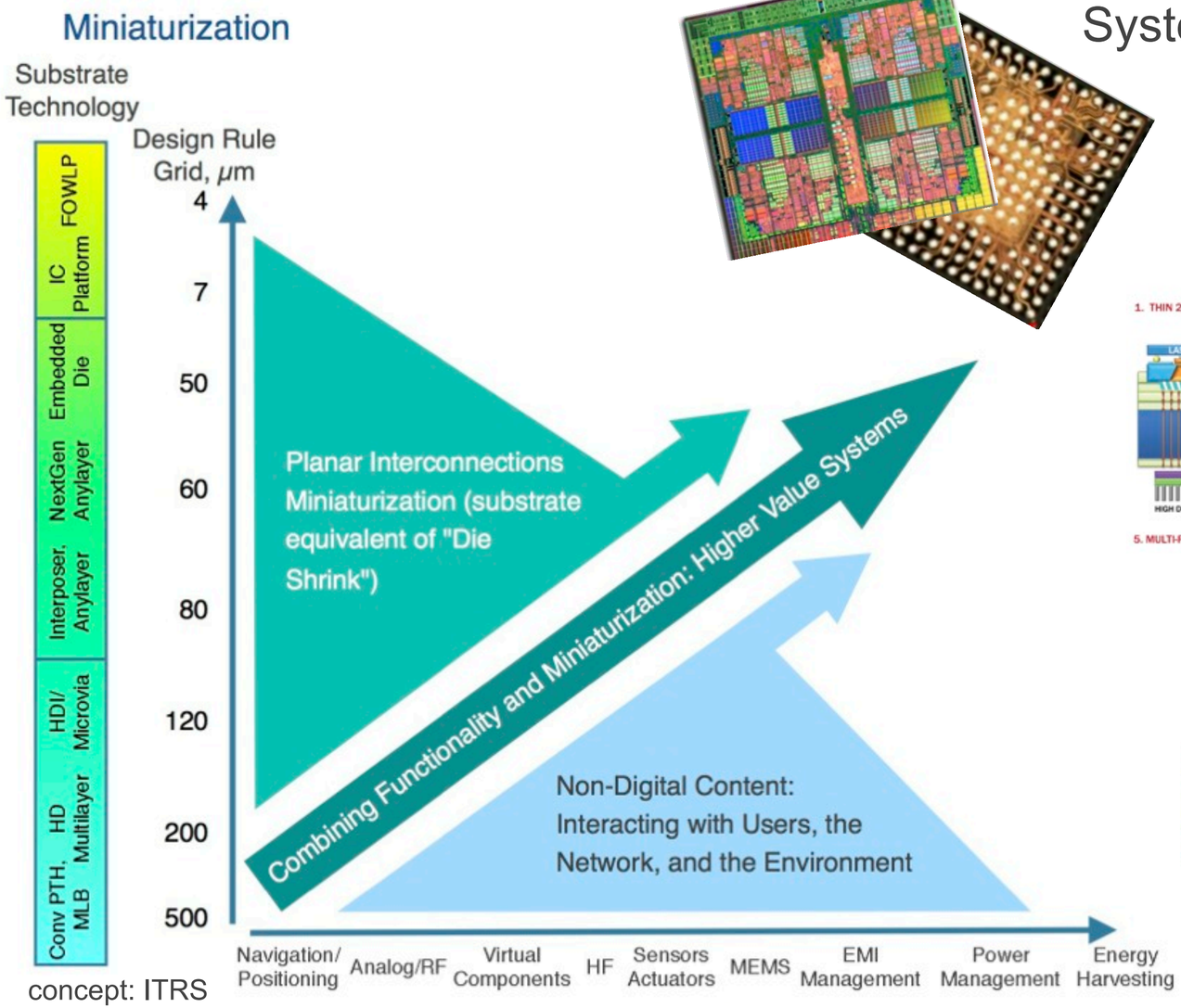
Diversification- the New Dimension

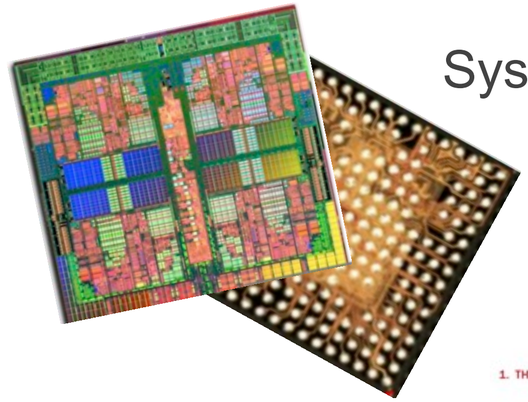
3D Embedding Technologies

- "Processing"

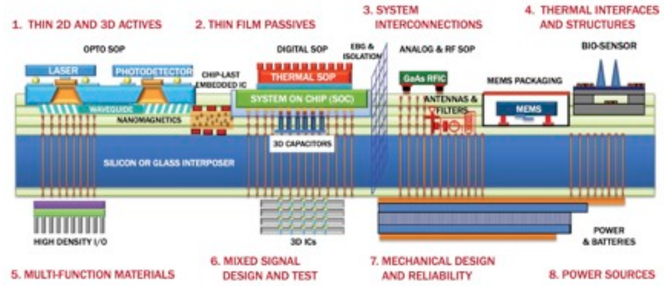


concept: ITRS

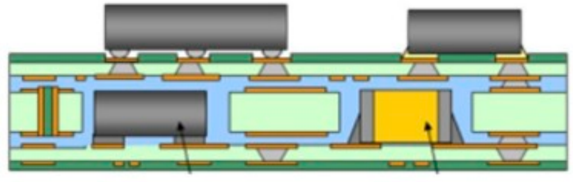
System-on-Chip



System-in-Package



System-in-Board



- "Experience"

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How to Get There from Here

Fabless Semiconductoring

- Standard functional building blocks
- Characterized, standard processes
- Front end - Back end integration
- Single interface: functional schematic + package design/pinouts

Fabless Embedding

- No building blocks (yet)
- Component availability (die/passives)
- RDL-layout interface problematic
- Multiple interfaces: wafer backend / embedding strategy / circuit design, subpanel array for molding/singulation

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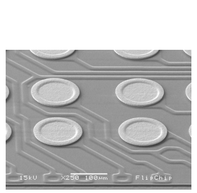
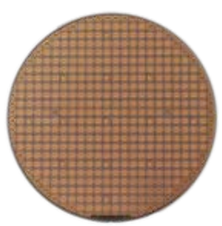
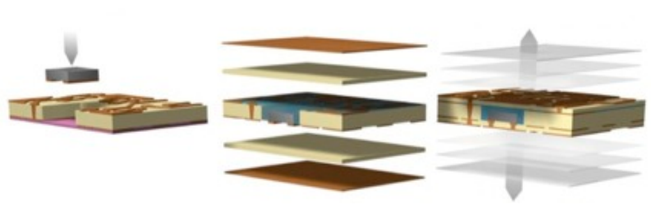
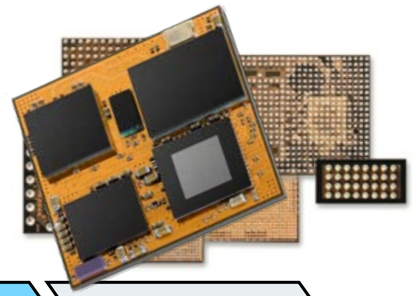
Embedding Today.. State of the Art

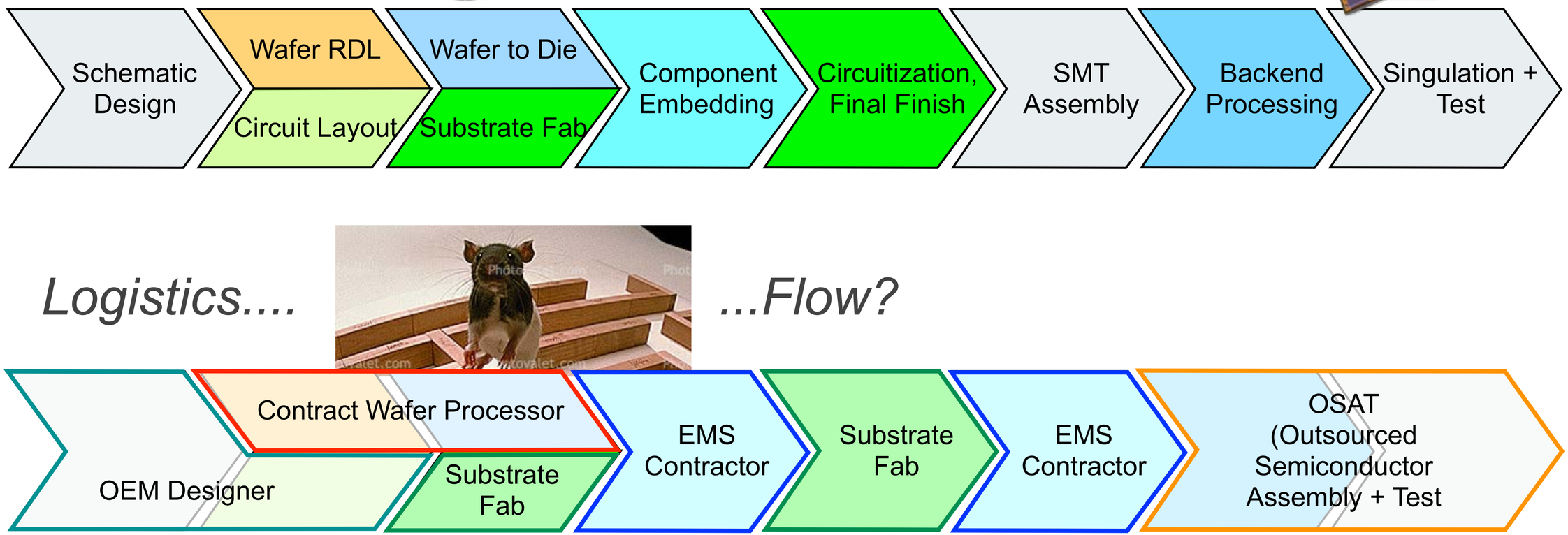
Process Flow...











Logistics....

...Flow?

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A New Paradigm: The "Organic Fab"

Conceptual Flow...

Product Concept

Combine with "functional building blocks" from library

Build with readily embeddable components from library

Advantages for Chip/Component Vendors
- ✓ Broaden market
- ✓ Shorten silicon time-to-market

Existing IP: wiring/package design

Advantages for Systems Designers
- ✓ Reduced development time
- ✓ Minimal learning curve (proven IP)

Feedback Loop
- ✓ Library Additions
- ✓ Licensable IP

New IP created

Advantages for Systems Designers
- ✓ Product differentiation
- ✓ Cross-licensing opportunities

- Accelerates adoption rate
- Shorten time-to-market
- Readily available components from library
- Proven IP
- Promote IP reuse (cross-licensing)

concept: TransSiP

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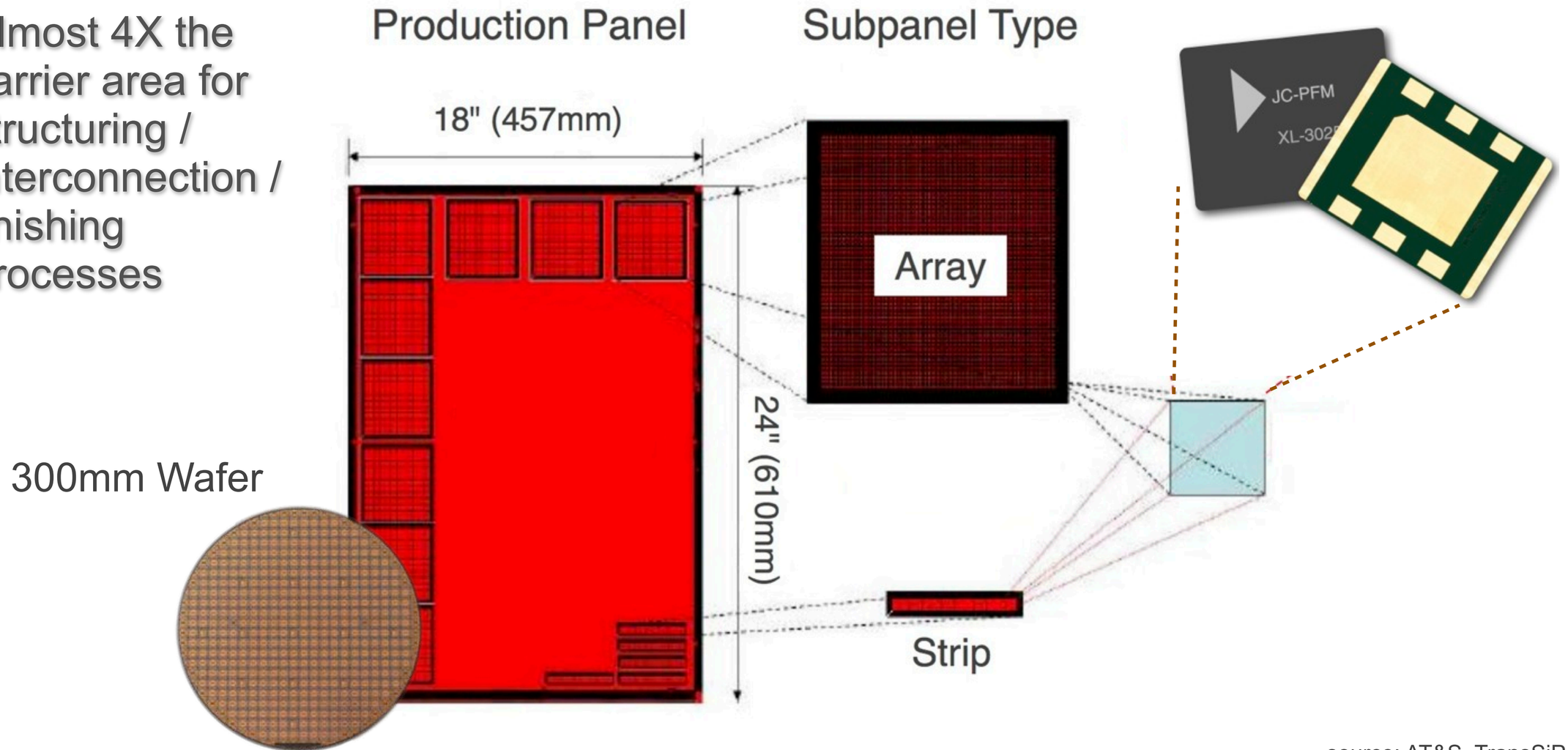
The Integration Advantage- "Organic Fab"

- Almost 4X the carrier area for structuring / interconnection / finishing processes



source: AT&S, TransSiP

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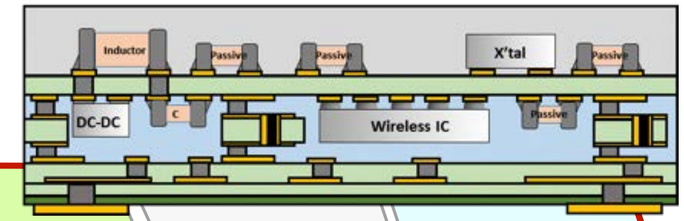
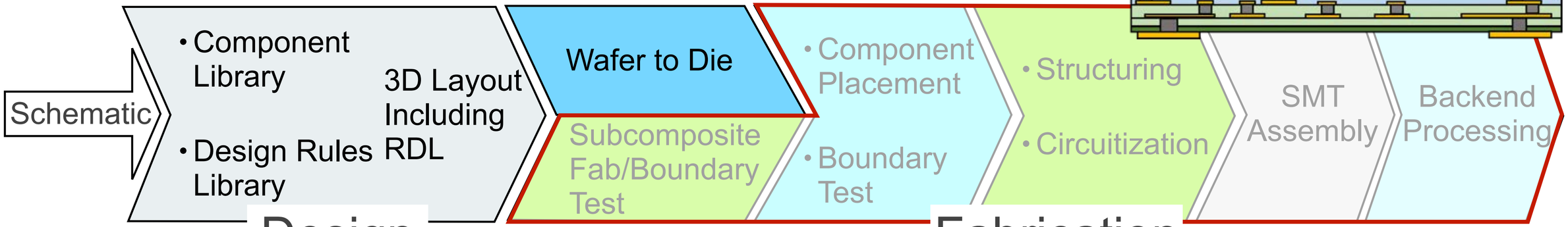
"One-Stop Shop"

"Organic Fab" Logistics Flow





Standard Tools + Libraries

The "Organic Fab": Via or Pads Processing

concept: TransSiP

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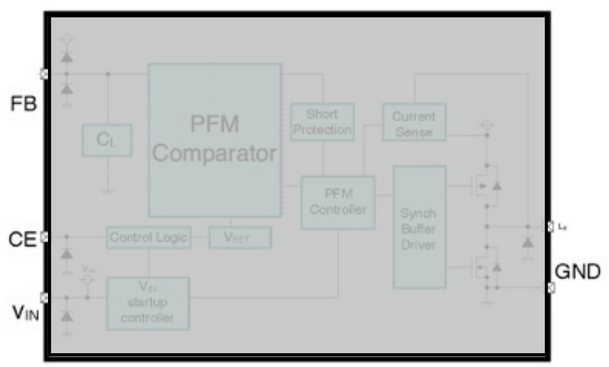
Applied "Organic Fab" Example..

- "Off-the-shelf" silicon: DC-DC microconverter
- "Out of the Library" SNJ Conditioner
- New Product



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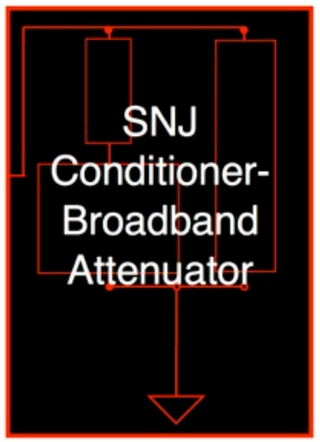

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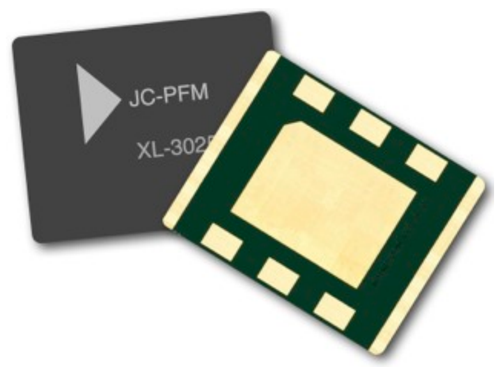

>90% Efficient DC-DC Conversion for Noise-Sensitive Applications

source: TransSiP

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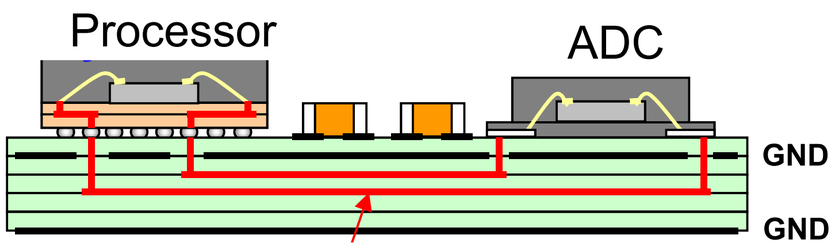
Turning Liabilities into Assets

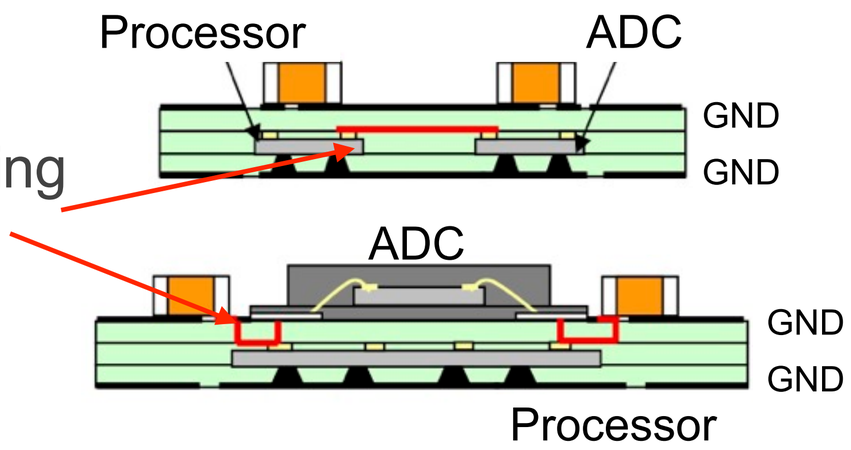
The Problem:



Parasitics in signal lines are a factor in high speed / RF design

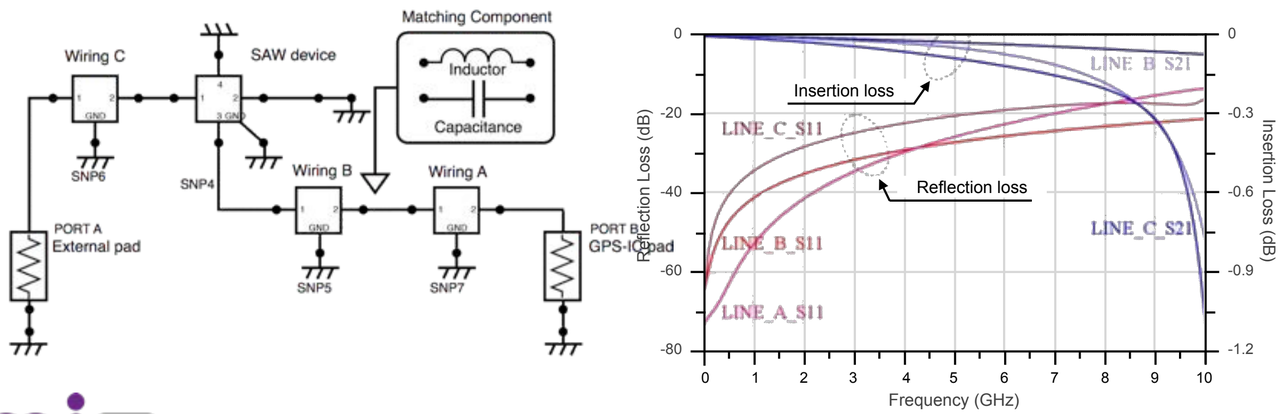
The Solution: Embedding Enables-

1. Reduced wiring length

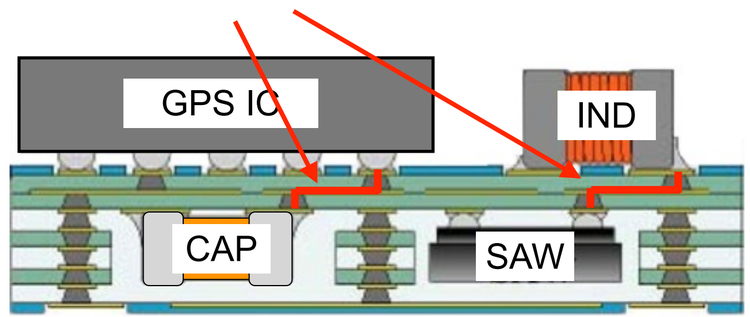


2. Controlled Equivalent L, R, C

Transmission Line Characteristics of GPS SIP Internal Wiring



Short, controlled Zo tracks



source: TransSiP

"Embedded Die Technology"

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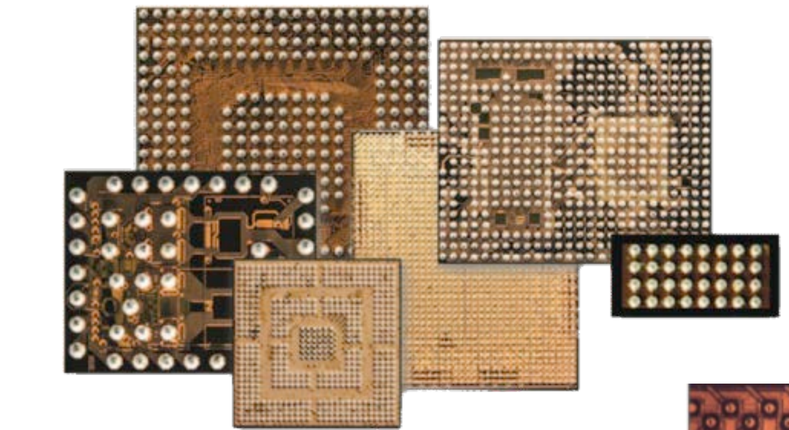
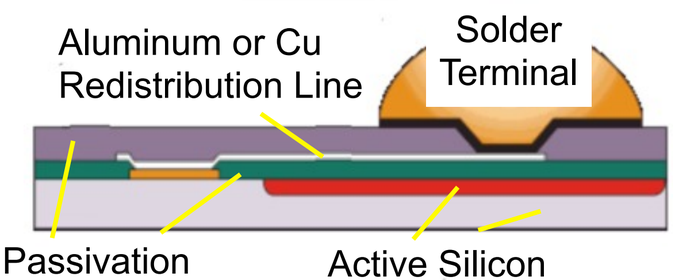
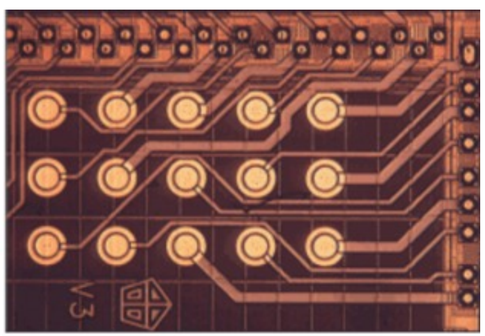
Embedding Options

"Wafer Level" Packages

- Single Sided Fan-out or Fan-In
- Adjust semiconductor footprint through design rules and redistribution layers



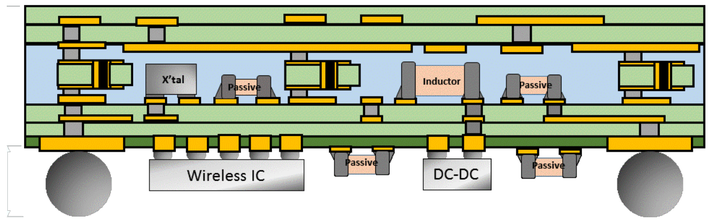


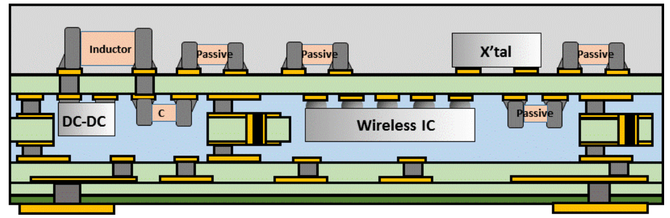


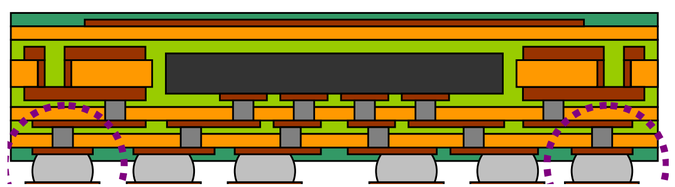
source: STATSChipPac

"Laminate Embedded" Packages

- "Via" Type
- "Pad" Type







source: TransSiP

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Ways to Skin the Cat- 1

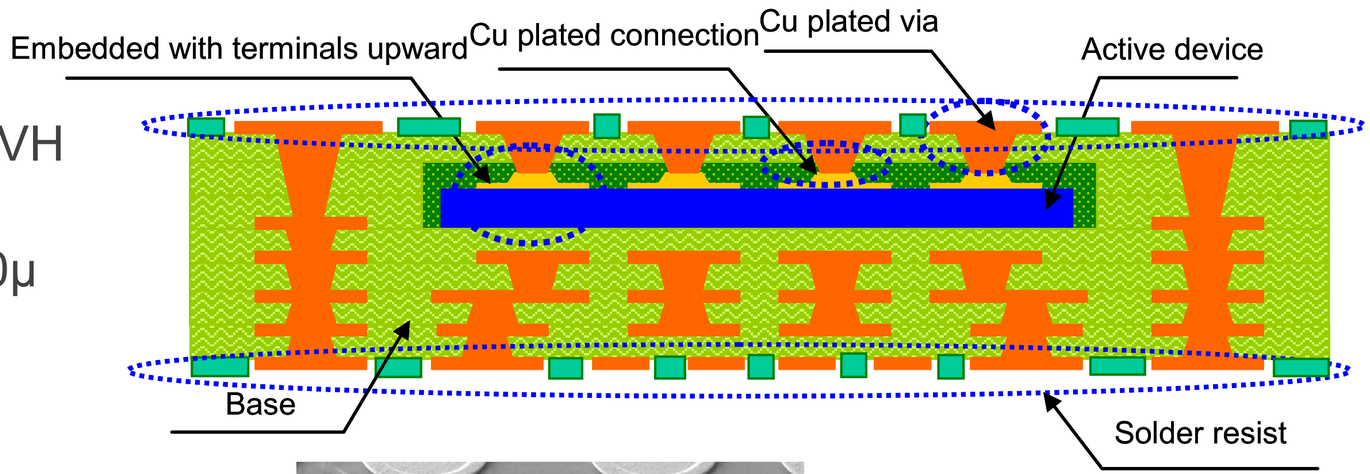
- "Via Connection"

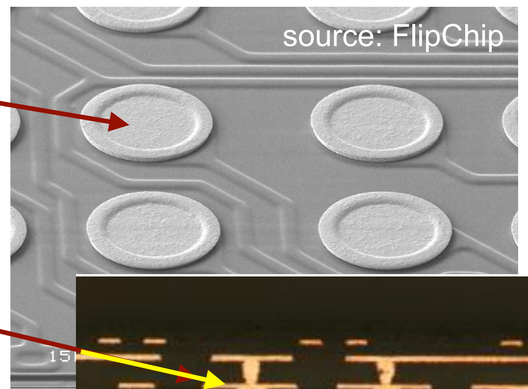
Pro

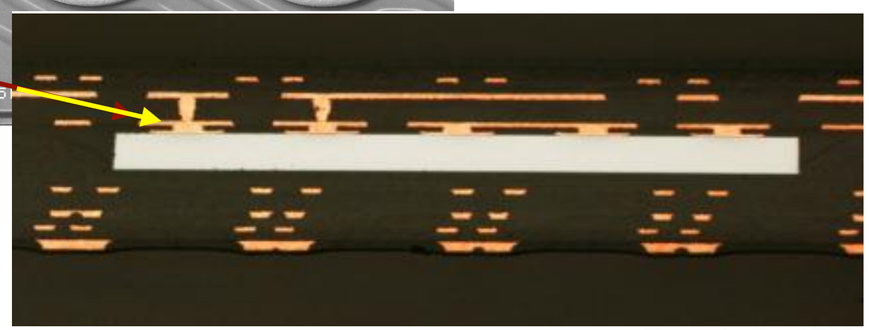
+ compatible with industry standard LVH (laser via hole) buildup processes
+ On-chip design rules (40µ pads/100µ pitch)

Con

- copper plating required on devices- additional cost
- registration is an issue
- no wiring on encapsulating layer







source: Fraunhofer IZM

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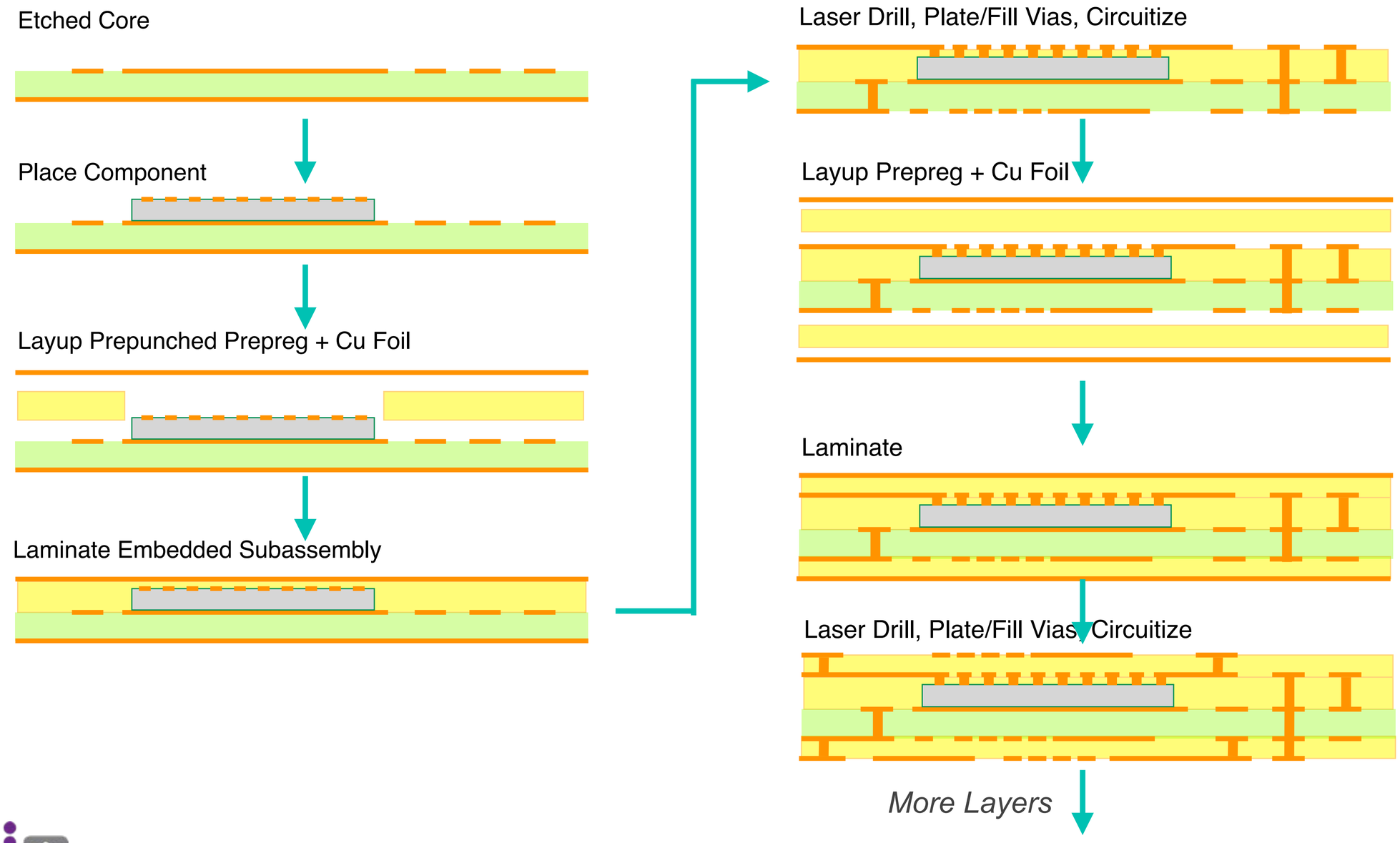
Via Connection Generic Process Flow



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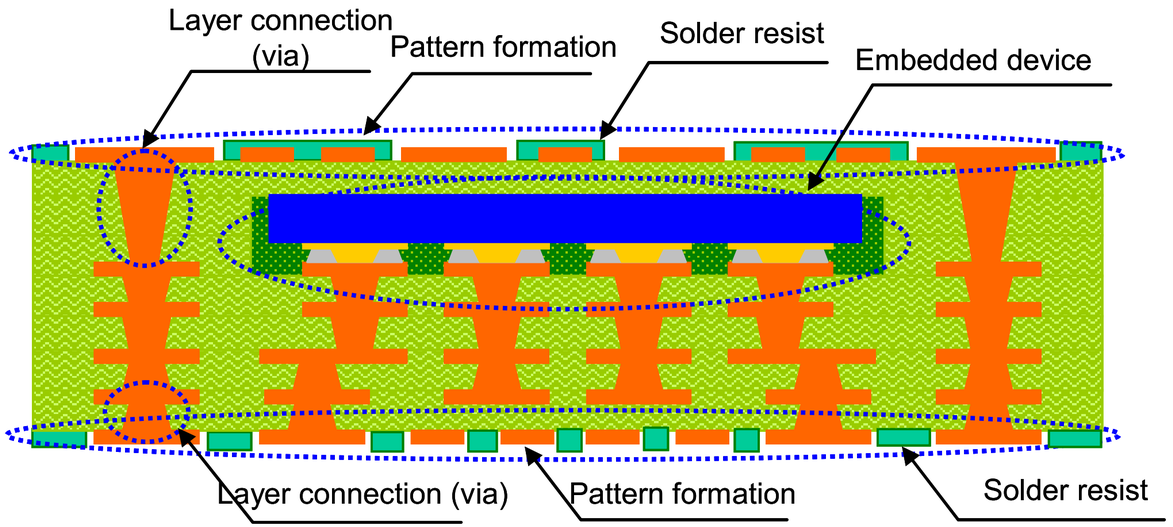
Ways to Skin the Cat- 2

- "Pad Connection"

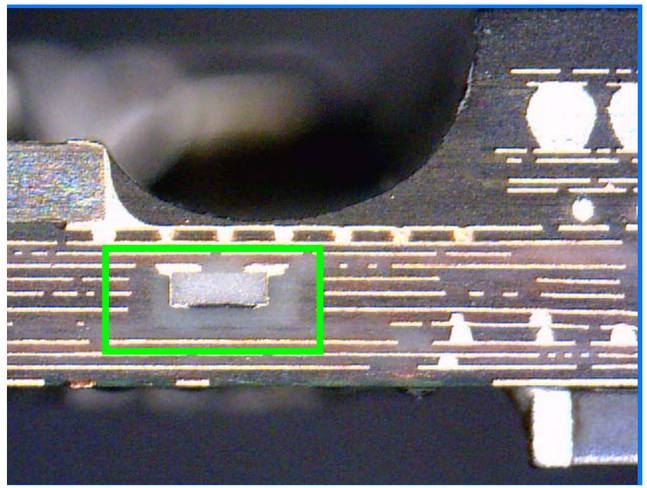
Pro
+ standard components and assembly processes used (solder / conductive adhesive)- no added cost
+ pad-to-device registration issues confined to well-known assembly issues and tolerances
+ hybrid processes (conductive post / LVH) can be used for maximum flexibility
+ wiring channels available in encapsulating layer(s)



Embedded WLCSP- Camera module

source: DNP

Con
+ most solutions are proprietary or derivatives of proprietary technologies (ALIVH, B2iT)
+ Density for conductive post solution limited to 0.2mm pitch



SSD Motherboard- 250 embedded passives

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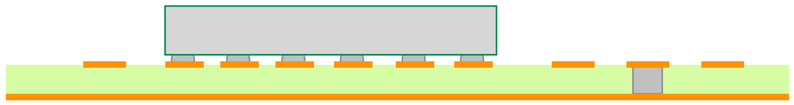
Pads / AnyLayer Post (ALP) Vias Process Flow *3D Embedding Technologies*

Subassembly 1: Print Bumps on Cu Foil, Laminate, Etch, Print Connectors

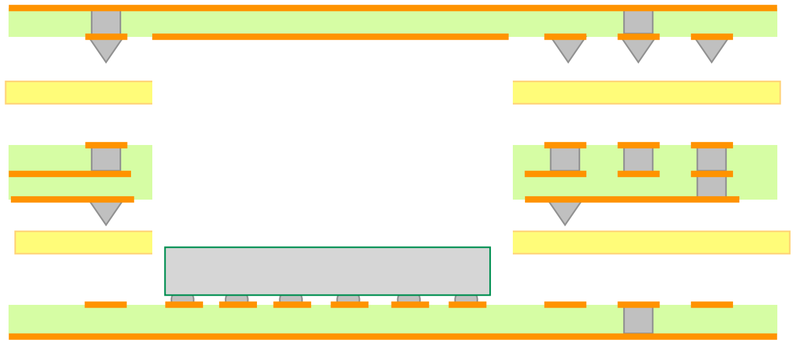
Subassembly 2: Print Bumps on Cu Foil, Laminate, Etch, Print Bumps, Laminate, etch, Print Connectors

Subassembly 2: Route Embedding Cavity

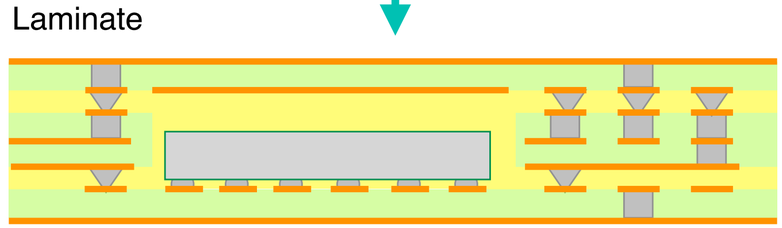
Subassembly 3: Copper Foil, Print Bumps, Laminate, Etch, Place + Reflow Component (underfill..?)



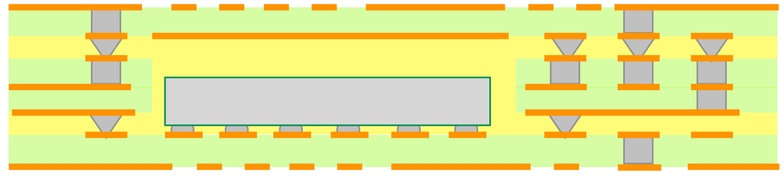
Layup with Prepunched Prepreg



Laminate



Circuitize, Final Fab



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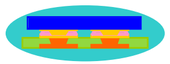
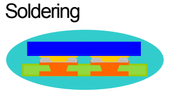
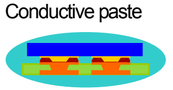
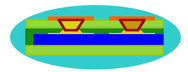
Mounting and Interconnection Options

Mounting Method		Device	Interconnection		Structure
			Process	Interconnection	
Pad bonding	Die bonding	Chip	Wire bonding	Wire melt-connection	
			Flip-chip bonding	Metal bonding Contact connection	Metal bonding Contact 
	Mounting	Wafer level packaging (WLP)	Reflow Polymer bonding	Soldering Conductive paste	Soldering
		Package	Reflow Polymer bonding	Soldering Conductive paste	Conductive paste
		Rectangular chip	Reflow Polymer bonding	Soldering Conductive paste	Soldering Conductive paste
		Rod-type chip	Reflow Polymer bonding	Soldering Conductive paste	
		Module	Reflow Polymer bonding	Soldering Conductive paste	Soldering 
		MEMS	Reflow Polymer bonding	Soldering Conductive paste	Conductive paste 

Mounting Method		Device	Interconnection		Structure
			Process	Interconnection	
Via bonding	Die bonding	Chip	Via connection	Copper plating Conductive paste	Copper plating Conductive paste 
		Wafer level package (WLP)	Via connection	Copper plating Conductive paste	
	Mounting	Package	Via connection	Copper plating Conductive paste	
		Rectangular chip	Via connection	Copper plating Conductive paste	Copper plating Conductive paste
		Rod-type chip	Via connection	Copper plating Conductive paste	
		Module	Via connection	Copper plating Conductive paste	
		MEMS	Via connection	Copper plating Conductive paste	

- Pad Bonding
  - multiple connection options
  - supports components of different thicknesses
- Via Bonding
  - compatible with industry standard processes
  - potentially higher I/O densities

source: JPCA

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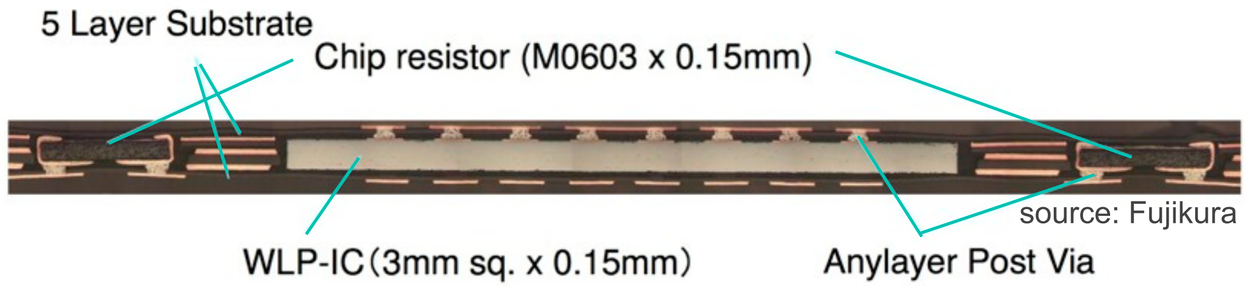
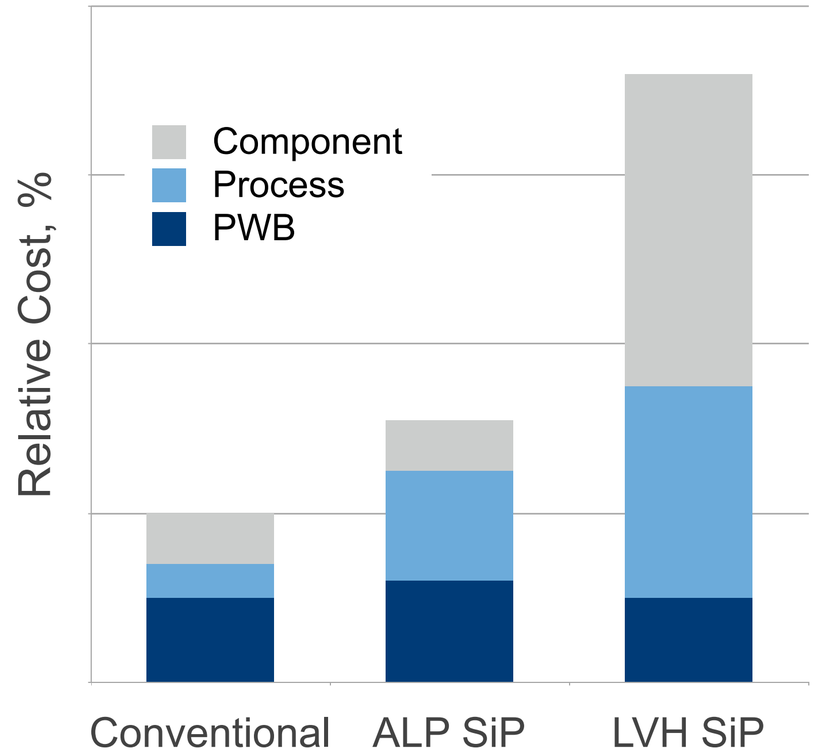
3D Embedded SiP ("3D SiP")

- Supports multiple device types: actives, discrete passives
- Off-the-shelf components can be used (WLP, CSP) ensuring industry-standard depth / breadth of supply
- ALP (Anylayer post) connections enable maximum layout flexibility and wiring density



- Overall cost advantage compared to Via/Laser Via Hole (LVH) SiP processes



Comparative Production Cost and Assembly: 250 embedded passive components

source: TransSiP

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