FPGA Network

Semiconductors to Systems

11 October | Swindon

Design Tools and Methodologies.

Agenda

Sponsored by

9:30 Registration & Coffee

– Networking and Sponsor Table-tops

10.00 Welcome and introduction

Flexible debug and visibility techniques to enhance all FPGA design and deployment

– Andy Jolley, ***Synopsys***

FPGA platform development kit enables fast TTM

– Chad Hamilton, ***BittWare Inc.***

Staying competitive by evolving your FPGA verification methodologies

– Alex Grove, ***Mentor Graphics***

Break

A game changer for VHDL verification: advanced HDL verification – made simple for anyone

– Espen Tallaksen, ***Bitvis AS***

12:45 Lunch

FPGA real-time debug with vastly increased operational capture time – live demo

– Nick Hardy, ***Telexsus***

100M gate designs in FPGAs – fact or fiction?

– Jonathan Meadowcroft, ***Cadence***

Zen and the art of high-speed design

– Mark Connor, ***ALTERA now part of Intel***

Break

Vivado HLx design methodology

- John Blaine, ***Xilinx***

Static code analysis using Blue Pearl software

- Andy Culmer, ***ITDev***

16.00 Networking Coffee, Event Close

Presentations Details

Static code analysis using Blue Pearl software

More details coming soon.

Andy Culmer, Engineering Director

Andy Culmer is ITDev's Engineering Director and has held this role for the past ten years. Having started his career as a design engineer at Philips Semiconductors back in 1998, He has worked on and managed a wide variety of projects spanning digital, mixed-signal and software design. Andy now uses this experience to garner an operational overview of all ITDev's projects as well as taking a more hands-on role in system architecture and requirements capture.

Andy joined ITDev from Semtech, where he led a team of engineers in the development of a family of telecoms synchronisation products.

Andy lives in Winchester with his wife and two children and enjoys mountain biking and water sports.

Staying competitive by evolving your FPGA verification methodologies

FPGA vendors continue to create new ways for FPGA users to efficiently design into complex FPGAs. This has created a widening gap between design abstraction and verification on which traditional verification approaches come up short. As a result, more FPGA users want and need to adopt modern verification practices to be competitive. Unfortunately, they don't always know where to start or find the cost/risk too great.

You will learn about themes that are pushing the need for advanced verification, understand how FPGA users are adapting and how a new look at verification methodologies helps build higher quality, on-time products.

Alex Grove, Application Engineer

Alex Grove has over 20 years' experience in the EDA industry having worked for Synopsys, ARM, Synplicity, Aldec, OneSpin Solutions, and Mentor Graphics.

He has experience in the design and verification of ASICs and FPGAs, functional safety, and a broad knowledge of the EDA industry. After graduating from Aston University, with an honours degree in Electronic Engineering & Computer Science, Alex joined Synopsys Northern Europe to work on synthesis and test.

During his time at Mentor, Alex has worked as a product specialist for High-Level Synthesis and Virtual Prototyping and is now working as European Application Engineer for functional verification with a focus on simulation and FPGA-based prototyping.

Flexible debug and visibility techniques to enhance all FPGA design and deployment cycles

The need to visualize and debug FPGA designs through all stages of the development and verification stages and at multiple levels of abstraction is the key to any effective design and deployment cycle. This session provides an overview of how the latest flexible debug and visibility technologies can be deployed to address specific implementation and verification challenges. The technologies are applicable to those using FPGAs for product or for FPGA based physical prototyping.

Andy Jolley, Solutions Corporate Application Consultant – FPGA-Based Prototyping

Andy has been working with FPGA technologies for over 28 years, originally in a design capacity in the telecommunications, radar and video industries before supporting FPGA synthesis and prototyping technologies at Synplicity and then Synopsys. Most recently, Andy has been supporting UK customers with their complex CPU SoC and GPU IP prototyping needs on the Synopsys HAPS platforms while also providing support for worldwide engagements to deploy the same SoC and GPU IPs embedded into user applications.

Andy holds a 1st Class Bachelor's Degree in Electronic Engineering from the University of Brighton, England.

FPGA Platform Development Kit Enables Fast TTM

FPGA designers would much rather spend their time developing their "secret sauce" than working on interfaces that should "just work"! It's no secret that too large a percentage of time is spent on getting the FPGA interfaces working before integrating any custom IP.

BittWare's FPGA Development Kit (FDK) provides a development environment where the low level IP blocks do "just work", enabling rapid development of their custom FPGA on BittWare board platforms. By leveraging standard tool flows from Altera and Xilinx, with a library of preconfigured IP components and example projects, the FDK drastically cuts development time.

Chad Hamilton, Vice President of Intellectual Property (IP), Software & Support

Chad Hamilton leads the effort to add value to BittWare's boards via software products and tools, soft IP products and examples, and technical support to BittWare's customer base.

Prior to joining BittWare, Hamilton spent several years developing FPGA & ASIC based products at Cabletron Systems, Northchurch Communications (start-up acquired by Newbridge Networks) & Applied Micro Circuits Corporation.

He also has extensive experience in Field Applications Engineering at Arrow Semiconductor and Sales at CompRep Associates.

Hamilton holds a Bachelor of Electrical Engineering from the University of New Hampshire (Durham, NH).

A game changer for VHDL verification: advanced VHDL verification made simple for anyone

Verification overview, readability, maintainability and reuse are vital for FPGA development efficiency and quality. UVVM VVC Framework was released in 2016 as a free, open source methodology - and is a true game changer for VHDL test benches. The VVC (VHDL Verification Component) approach makes it Lego-like to build. A key benefit is the simple SW-like VHDL test sequencer that controls the TB architecture. This takes overview, readability and maintainability to a new level.

This presentation will show the simplicity of UVVM and explain what a VVC it is doing and how easy it is to understand the test sequencer controlling them. It will also show how randomisation and coverage may be controlled.

Espen Tallaksen, Managing Director

Espen Tallaksen is the managing director and founder of Bitvis, an independent design centre for embedded software and FPGA. He graduated from the University of Glasgow in 1987 and has 29 years experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway, including his earlier founded company Digitas. Espen delivers courses on how to design and verify FPGAs more efficiently and with a better quality.

Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement. One result of this interest is the UVVM verification platform that is currently being used by companies world-wide.

100M gate designs in FPGAs - Fact or Fiction?

Today's FPGAs are large , one can now design with 10M gates , even 20M gates is possible , and every few years, this capacity is doubled again.

But how do I get larger designs onto an FPGA, how do I get it implemented, and perhaps the most important question, how do I get it verified?

The presentation will look at the issues of large designs in FPGAs and discuss how methods and tools from ASIC design and verification make the development of ultra-large FPGA designs manageable. Special attention will be given to memories, clocking and verification.

Jonathan Meadowcroft, Senior Sales Technical Leader

Jon Meadowcroft is a Senior Application Engineer at Cadence Design Systems, responsible for hardware emulation and FPGA prototyping.

He previously spent 16 years as a designer of ASIC, FPGA and systems in areas such as signal processing, graphics, mobile and wireless

Vivado HLx Design Methodology

Making an SoC design for an FPGA is a task that requires a lot of manpower. The HLx methodology is a process to enable focus on your value add portion of the design. What makes HLx a higher level methodology? In this presentation we focus on the 4 key enablement steps of methodology and some features we are adding to the tools to enable this.

John Blaine, Software Application Engineer

Over 15 years of Xilinx experience mostly served working with customers from different domains. Recently moved to a software applications position working on Vivado implementation software.

Zen & the art of high speed design

Designing for high-speed has long been the black art of electronic design. The "art" is essential for system performance and it can also reduce system cost. It's an essential skill for advanced FPGA designers.

This presentation will highlight the thought processes and techniques used throughout the design process and features within silicon to achieve system-wide clock speeds up to 1GHz.

Mark Connor, Staff Field Application Engineer

Mark Connor joined the Altera Northern Europe team in 1997 he has held several positions including Design Specialist FAE before his current position. These roles involved helping customers implement their designs, closing timing, benchmarking designs against competing solutions and imparting knowledge through training.

FPGA real-time debug with vastly increased operational capture time – live demo

Traditional FPGA debug tools are limited in their capability to provide the depth of data capture required for debugging modern designs. The small window of observation often leaves engineers guessing which signals to scrutinise as well as which conditions to trigger upon. FPGA designs can take hours to compile, meaning the debug 'guessing' process can cause serious delays to the resolution of issues and therefore to entire projects.

This new methodology provides capturing of up to 200,000 times more FPGA operations than standard embedded instrumentation tools - rare or non-repetitive events can then be captured with these deep trace depths.

Nick Hardy, Director

Nick Hardy is a co-founder of Telexsus Ltd and has over 15 years' experience in electronic design, manufacturing and consultancy, in sectors from defence to semiconductor.

Nick's experience working for start-ups and large corporations has given him a clear understanding of the challenges faced by companies from design concept through to product manufacture and support. Particular areas of focus include FPGAs, high speed interface standards and JTAG Boundary scan.

Telexsus delivers world class electronic engineering development and test tools combined with support and training.