FPGAs for Reconfigurable 5G and Beyond Wireless Communication

Dr. Milos Milosavljevic
Senior Lecturer in Digital Communications and Electronics

www.herts.ac.uk
Outline

- FPGAs for a new paradigm shift in networks
- High-speed back/front-hauling research activities at UH
- Examples of a few FPGA developments for high-speed comms.
- Future of FPGAs for 5G
5G Needs FPGAs

- Centralised baseband processing to serve many hundreds or thousands of remote radios
- Front/backhauling capacity will increase significantly
- 5G will also exploit software defined network (SDN) capabilities resulting in more software centric architecture

Source: Lund University
Next Generation Back- and Front-hauling for 5G

Software Definable Transceivers for Future Networks

- Development board used for fast prototyping new algorithms
- High speed ADC/DAC provided through the FMC connectors

- IP Cores development for DSPs and MAC blocks
- The target is to achieve very fast bidirectional real-time transmission
FPGA based Transceivers

[Block diagram of FPGA based Transceivers]

University of Hertfordshire

IP Core Development

- All required high performance IP cores have been developed
  - FFT / IFFT
  - CORDIC
  - Equalizer
  - Divider
  - Correlator

- A synchronization mechanism for the ONUs has been developed
  - Implementation of Schmidl & Cox Sync detection
  - Local and sampling oscillator are phase locked to OLT oscillators

### IP Core Development

<table>
<thead>
<tr>
<th>Component</th>
<th>Max. Frequency</th>
<th>LUTs used</th>
</tr>
</thead>
<tbody>
<tr>
<td>ONU – Sync</td>
<td>266.8 MHz</td>
<td>62304 (25% of 380T)</td>
</tr>
<tr>
<td>ONU - FFT 32</td>
<td>583.0 MHz</td>
<td>18079 (7% of 380T)</td>
</tr>
<tr>
<td>ONU - RX Total</td>
<td>215.1 MHz</td>
<td>103389 (42% of 380T)</td>
</tr>
<tr>
<td>ONU - TX Total</td>
<td>231.5 MHz</td>
<td>20917 (8% of 380T)</td>
</tr>
<tr>
<td>OLT - Sync</td>
<td>360.5 MHz</td>
<td>3433 (0% of 565T)</td>
</tr>
<tr>
<td>OLT - FFT 256</td>
<td>561.7 MHz</td>
<td>121748 (33% of 565T)</td>
</tr>
<tr>
<td>OLT - RX Total</td>
<td>360.5 MHz</td>
<td>130070 (36% of 565T)</td>
</tr>
<tr>
<td>OLT - TX Total</td>
<td>436.5 MHz</td>
<td>115711 (32% of 565T)</td>
</tr>
</tbody>
</table>
Developed FPGA IP Cores (cont.)

**Synchronisation**

**FFT**

- Stage 1: 256 butterflies
- Stage 2: 64 butterflies
- Stage 3: 16 butterflies
- Stage 4: 16 butterflies

**NCO**

- FFT Synchronisation
- NCO

**University of Hertfordshire**

General Board Design
Complete Testbed with FPGAs
VHDL Simulation with ModelSim
100Gbit/s Transmission

<table>
<thead>
<tr>
<th>Type</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol duration</td>
<td>12.8 ns / 78.125 MHz</td>
</tr>
<tr>
<td>Cyclic suffix</td>
<td>1/4</td>
</tr>
<tr>
<td>OLT sample rate</td>
<td>25 GS/s</td>
</tr>
<tr>
<td>OLT FFT size</td>
<td>256 points</td>
</tr>
<tr>
<td>OLT symbol size</td>
<td>320 samples</td>
</tr>
<tr>
<td>ONU sample rate</td>
<td>3.125 GS/s</td>
</tr>
<tr>
<td>ONU FFT size</td>
<td>32 points</td>
</tr>
<tr>
<td>ONU symbol size</td>
<td>40 samples</td>
</tr>
<tr>
<td>Symbols per frame</td>
<td>8250</td>
</tr>
<tr>
<td>Frame duration</td>
<td>105.6 µs / 9.4697 KHz</td>
</tr>
</tbody>
</table>
Dynamic Resource Management on FPGAs

- Embedded Leon 3 processor with Linux controls the IP cores and the MAC unit
- C implementation of dynamic MAC successfully demonstrated

Allowing the FPGA modify the IP cores dynamically depending on the demand on the network

Alternative 5G Fronthauling Solutions

Standard CPRI Implementation

RRH

LTE RF

0 1 0 1 0

User Data

Control and Management

Synchronization

BBU

LTE PHY

LTE

0 1 0 1 0

CPRI Basic Frame

CPRI Overhead Control Word (8 bits)
CPRI Payload IQ Data Block (120 bits)

CPRI Hyper Frame

#0 #1 #255

66.67 μs

CPRI Control Plane

Fast C&M
Slow C&M
L1 Inbound Protocol
Vendor Specific
Timing and Synchronization
The FPGAs at RRH and BBU create CPRI data which is dynamically compressed before Ethernet encapsulation takes place.

Different networks topologies and SDN applications can be programmed using Mininet within a Linux environment to test different scenarios.

NetFPGAs can be used for implementing OpenFlow Switches providing at least 100Gbps connectivity with Xilinx Virtex-7 690T FPGA.

Future of FPGAs for 5G

FPGAs will be used for prototyping 5G wireless infrastructure over the next few years.

With more serial transceivers, DSP slices, block RAMs, DLLs, PCIe interfaces, and other blocks, the FPGA's hardware penalty for re-programmability continues to diminish.

It is likely the 5G wireless infrastructure OEMs will bet on programmability to reduce design risk and speed time to market.

As we look to 2020 for widespread 5G deployment, it is likely that most OEMs will sell production equipment based on FPGAs and All Programmable SoCs.

The hardware complexity of 5G’s physical layer is just too challenging to guarantee that ASIC implementations will be free of severe hardware bugs.