Using Test Access Standards Across The Product Lifecycle

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Outline

• Background & Previous Work
• Revision - Boundary Scan
• Extension to iJTAG IEEE1687
• iJTAG Programing
• Case Studies
• Summary and References
Background 2015/16

• 2015/16: Work for EC – ICT3 “Smart Systems” & ICT25 Nanoelectronics
• DfT Training: Singapore and Penang
• Research into prognostics & on-line test – Lancaster University
• Work on Prognostics (Pressure and Electrochemical Sensors)
Through Life Support

- Need a method to test & monitor devices in application
- Ideally detect evolving faults
- Requires hardware monitoring
  - Need to measure simple parameters
  - No complex stimuli
- Needs simple integration into the device and system (Test Access Standards!)
- Numerous self-test structures developed by little uptake due to cost and complexity of integration
Previous Work

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Boundary Scan is an IEEE standardised architecture for test access to complex PCB’s and the integrated circuits on those PCB’s, as well as the control of on-chip test features such as scan paths.


– In 1988, a proposal from this group for a boundary scan standard JTAG Version 2.0 was offered to the IEEE Testability Bus Standards Committee (P1149) for inclusion in the standard being developed. This submission became the basis for the IEEE standard and JTAG became the working group developing the standard.

– IEEE std. 1149.1 was accepted in 1990. The latest revision was published in 2012.
Principle Of Boundary Scan

Each boundary-scan cell can:
- Capture data on its parallel input PI
- Update data onto its parallel output PO
- Serially scan data from SO to its neighbour’s SI
- Behave transparently: PI passes to PO

Test Data In (TDI)
Test Clock (TCK)
Test Mode Select (TMS)
Test Data Out (TDO)
IEEE1149.1 Architecture

Boundary-Scan Register

Internal scan path

Note: *all* digital logic must be contained inside the boundary-scan register.
• Internal scan paths are also connected via the test-bus to the pins *TDI* & *TDO*.

• The normal I/Os of the core logic are connected via the boundary scan cells to the same pads.

• The test bus itself consists of the boundary scan registers, a 1-bit bypass register, an instruction register, several other registers and the *TAP*.

• In addition to the *TDI* & *TDO* pins, a test clock and a test mode pin have to be provided. *TDI* receives test instructions and test data, test results are read via *TDO*, test control is applied via *TMS* & *TCK*. 
TAP Controller

Test logic reset

Run test / Idle

Select DR Scan

Capture DR

Shift DR

Exit 1 DR

Pause DR

Exit 2 DR

update DR

Select IR Scan

Capture IR

Shift IR

Exit 1 IR

Pause IR

Exit 2 IR

update IR

DR – Data Register
IR – Instruction Register

NMI: 12th May 2016
Basic Boundary-Scan Cell

**Normal**: Mode=0: data passes from PI to PO to core logic; cell is transparent

**Scan**: ShiftDR=1: cells form scan path via SI/SO connected to TDI & TDO

**Capture**: ShiftDR=0: data on PI can be loaded into the scan path when ClockDR

**Update**: Mode=1: Content of Scan Cell (from scan or capture operation) is applied to PO when pulse on UpdateDR
Extensions of IEEE 1149.1

• IEEE 1149.1-2012 / 2013 extends the standard to:
  – support a redefined initialisation data register to support analogue parameters for configuring high speed I/O
  – Enables on-chip PLL’s to be controlled
  – See [http://grouper.ieee.org/groups/1149/1/ieee-1149-1-2012-changes.pdf](http://grouper.ieee.org/groups/1149/1/ieee-1149-1-2012-changes.pdf) for more details

• IEEE 1149.7 reduces the pin count to 2 and offers four selectable power modes to enable ultra-low power devices.
What about Adoption of Boundary Scan

IEEE 1149.1 - Standard - Widely adopted  
IEEE 1149.4 - Standard – little/no adoption  
IEEE 1149.5 - Withdrawn - System Level Standard  
IEEE 1149.6 - Standard – Good acceptance for AC-coupled  
IEEE 1149.7 - New Standard - little adoption – Royalties\(^5\)  
IEEE 1532 - Admin Withdrawn - bit/pof and SVF work fine  
IEEE 1500 - Standard – little adoption, NXP, Virage, Synopsys

• None of these standards are really optimised to support embedded test structures and monitoring instruments – previous work around 1149.4 has little infrastructure to build on.
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Is IJTAG? (IEEE P1687) an option

- IJTAG was proposed to address the following shortcomings and weakness identified in both IEEE 1149.1 and IEEE 1500:
  - Identified weaknesses regarding test scheduling and operating trade-offs
  - Concerns with respect to limitations in scalability with growing number of embedded instruments

- Through life testing demands access to internal test resources within the application
  - iJTAG supports access to “embedded Instruments” via a standardised JTAG interface
What does iJTAG include?

• iJTAG 1687 is an IEEE Standard

• It is made up of 3 components
  – A flexible instrument access architecture leveraging a network of serial scan chains
  – A programming language to describe the network (Instrument Connectivity Language: ICL)
  – An instrument vector language (Procedural Description Language: PDL)
Current Status

• Published as IEEE 1687-2014 on the 5\textsuperscript{th} of December, 2014

• Active Committee Members included:
  – 12 Chip Providers (including TI, IBM, AMD, Qualcomm, Broadcom etc.)
  – 14 Tool Providers (including ASSET, Intellitech, Mentor, Cadence, Goepel etc.)
  – 2 Instrument Providers (Tektronix and Agilent)
  – 1 ATE provider (Teradyne)
  – 5 End Users (including Cisco, Alcatel-Lucent etc.)
iJTAG 1687 Solution

- Adds an interface to JTAG in the form of a Test Data Register – “The Gateway”
  - Routes TDI and TDO to instrument networks
  - Enabled through IR scan then use of RD scans to load all data
The Gateway Structure

- The gateway contains one or more Segment Insertion Bits (SIB’s) – acts as a switch that is controlled by the GWEN instruction and shifted in data to either open (scan-in to HIP scan in), Scan-out to HIP scan out) or closed – Scanin to Scanout.
- Also must route clock, select, shift-enable, capture-enable and update-enable to each lower level SIB
Opening and Closing SIB’s in the gateway:

- In Shift-DR, each control bit is placed into the register of each SIB in the gateway.
- Update-DR state: The control bit for each SIB is transferred into the SIB’s State Register,
- back to Shift-DR - shift out the output vector and shifting in the next input

The above represents one control cycle which takes 6 TCK cycles.
A Simple 1687 Network

- Access Link Instruction
- Not Part of the 1687 Standard
- Used 1149.1 TAP Controller

- Instrument Interface & Instrument Vectors
- Scan Path Network & Plug-n-Play Features
- Scan Path Management (SIBs, NIBs, LRs)
- Local Selection & Configuration Decode

- Embedded Instrument (or device)
- Not Part of the 1687 Standard

NMI: 12th May 2016
Test Data Registers

- The Instrument Interface Register is a variable length IEEE1149.1 TDR
- Each instrument in a 1687 Compliant architecture should be paired with a “size appropriate” TDR
- The cells can be Read-Only, Write-Only or Read-Write
Test Data Registers: organisation

- TDR’s can be organized in different ways to minimize the **Access Time** overhead

*Ibrahim A, Kerkhoff, HG: IJTAG Integration of Complex Digital Embedded Instruments, 9th International Design and Test Symposium, 2014*
Scan Insertion Bit (SIB)

- SIB is a single bit TDR
- Any number of them can be placed anywhere in the network
- SIBs are used to include scan-paths, allowing dynamic reconfiguration of a P1687 network
- SIB acts as a gateway with two states, open or closed
Scan Insertion Bit (SIB)

When closed the “select” is de-asserted and freezes the TDR
Scan Insertion Bit (SIB)

When Closed
The SIB represents a single bypass bit

TDI
Select
ShiftEn
TCK
TDO
UpdateEn

To TDI 2
From TDO 2
Select
Scan Insertion Bit (SIB)

When Open:

A pre-SIB inserts the added scan path in front of the control cell

A post-SIB inserts the added scan path after the Control cell
Scan Insertion Bit (SIB)

Variable length scan path closes on Reset
Network; Embedded Instruments

• Types of Embedded Instruments:
  – Design-Ware
  – Reused legacy design
  – 3\textsuperscript{rd} Party IP
  – EDA-Generated

• Embedded Instruments Access for:
  – \textbf{Test}: Scan, BIST etc.
  – \textbf{Debug}: Trace, Buffer Capture, Triggers etc.
  – \textbf{Monitor}: I/O monitoring etc.
  – \textbf{Functional Configuration}: Bus Configuration, IO Tuning, PLL Settings etc.
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Why not extend BDSL (Boundary Scan Description Language?)

- BDSL provides only a static structural view of the system.
- The boundary scan chain is detailed as an ordered succession of bits.
- Internal chains are defined only by name and fixed length.
- BDSL has no procedural or algorithmic capabilities.
- BDSL can define new rules through language extensions.
Procedural Description Language

• Two languages have been developed
  – hardware description language (ICL) that contains the hierarchical connectivity of the scan network between the IEEE 1149.1 Test Access Port (TAP) and the instruments
  – procedure description language (PDL) that contains the patterns used to interact with the instruments.
Instrument Connectivity Language (ICL)

- The ICL is used to describe the access mechanisms and network of embedded instruments
- ICL documents and describes Instruments, their interfaces and documents their pathways
- The “soft” knowledge of the pathways allows for dynamic reconfiguration of test vectors
- The ICL can be (informally) perceived of being of two types:
  - instrument-ICL (i-ICL) describing the instrument and its interface(s)
  - network-ICL (n-ICL) describing the network and pathways
Procedural Description Language (PDL)

- PDL documents the operations of embedded instruments
- The instrument whose operations are described can be at any network level. PDL is used in conjunction with ICL.
- PDL allows automated tools to retarget the instrument’s procedures and test vectors
- There are two levels of PDL programming:
  - Level 0 PDL: Allows for static programming. There are no loops, conditional branching commands or interactive features.
  - Level 1 PDL: This is essentially “Tool Control Language” (TDL) that has all the features of a fully mature programming language. It is a widely used in EDA.
Example of PDL for an adc_bist module

iPDLLevel 1;
iProcsForModule adc_bist;
##This declaration binds all following commands to adc_bist module

iProc BIST_Stim{mode default}{
iClock clk;  ## Clock
set cycles(default) 5000;
set cycles(thorough) 20000;

iRead status[2];  ##read power status
iRunLoop $cycles($mode) –sck -clk;  ##wait for n clock cycles
iApply;

iWrite enable 1;  ##enable the device
iApply;

iWrite data 0xA5;  ##write an 8bit test sequence equal to mt_b
iApply;

iWrite trigger 1;  ##initiate signal stimulus
iApply;

iRead testEnded 1;  ##testEnded expected value ‘1’ (test ended)
iWrite enable 0;  ##disable the device
iApply;
}

Module Set
Procedure to run BIST_Stim in default mode

Clk is set
Setting mode specific run cycles

Wait for n clock cycles

Enable Device
Load “mt_b” test values as stimulus
Trigger test based on stimulus

Read Test output, Disable instrument
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Using IJTAG digital Islands to Perform Trim and Test (2015)

- Dialog Semiconductor, Germany
  - Demonstrates the use of IJTAG islands to hold test and trim functions.
  - These digital islands were integrated with analogue circuits with minimal digital overhead
  - Demonstrates the use of a hardwired mapping between the legacy $I^2C$ and TAP allowing the use of $I^2C$ to access IJTAG resources

Using IJTAG digital Islands to Perform Trim and Test (2015)

Fig 1: Initialization
Data flow for digital core registers

Fig 2: Proposed IJTAG island architecture with address register bank

Fig 3: I²C mapped to TAP controller connected to IJTAG chain
An MPSoC demonstrator using IEEE P1687 (2014)

- Ericson AB, Lund University & Semcon Sweden (2014)
  - MPSoC demonstrator developed to enable Fault Injection and Fault Handling experiments
  - Instrument Access Infrastructure (IAI) defined using IEEE P1687. It defines a network of instruments equipped with fault detection features on the MPSoC
  - Use of IEEE P1687 to inject faults in targeted instruments
  - Use of IEEE P1687 to assist in fault handling
  - Demonstrated:
    - Improvement at the rate of component level fault detection
    - Improved system-level fault action
    - Flexible access to all components on the network

An MPSoC demonstrator using IEEE P1687 (2014)

Tree-like “Instrument Access Infrastructure” & “Fault Indication and Propagation Infrastructure”

Error Indication Flag
Case Study – Agilent / Avago

- Bit Error rate Testing and Eye Mapping for a HSSIO.
- Use of P1687 to control, seed, execute and capture outputs from the test resource
- Targets portability and access via standard TAP and P1687 interface
Traditional v Embedded

- Traditional BERT:
  - no externally accessible point at which to probe the post-equalized signal in the receiver

- Embedded BERT
  - not necessarily well-calibrated compared to a lab instrument since it resides on the same silicon as the circuit it is measuring.
HSSIO Instrument

- Target is a digital BIST for BER and Eye mapping
- Potential to generate compensation feedback
- Features margin analysis for rapid generation of low BER metrics
Case Study – Agilent / Avago

- complete register based interface to all HSSIO instrument resources
- third latch controlled by an Update signal, so that the act of shifting the scan chain is not destructive to the Q-outputs of the flip-flops.
Conclusion

• iJTAG Well suited to the control of many structural test & monitoring solutions in Digital and Mixed Signal systems.

• Support for use of the standard is good – eg. Mentor Graphics “Tessent”

• Interest in building solutions including Bias Superposition into industrial demonstrators using iJTAG.

• If hardware can be monitored on-line, can prognostics and self-repair also be implemented? – leading to a complete through life solution.
References


• IEEE Std. 1149.7™ Standard for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture, DOI 10.1109/IEEEESTD.2010.5412866 Feb. 2010.

• JTAG Development tools and products see for example


