Challenges and opportunities of debugging FPGAs with embedded CPUs

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Agenda

- How system bring-up has got more complicated
- Board Bring up strategies
- IP Integration and test
- Debug and deployment – can the processor help?
- Final thoughts

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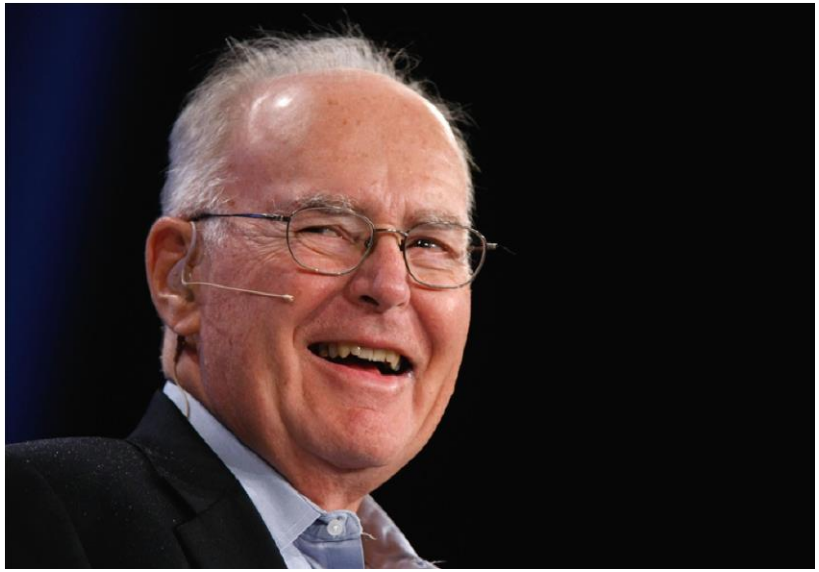
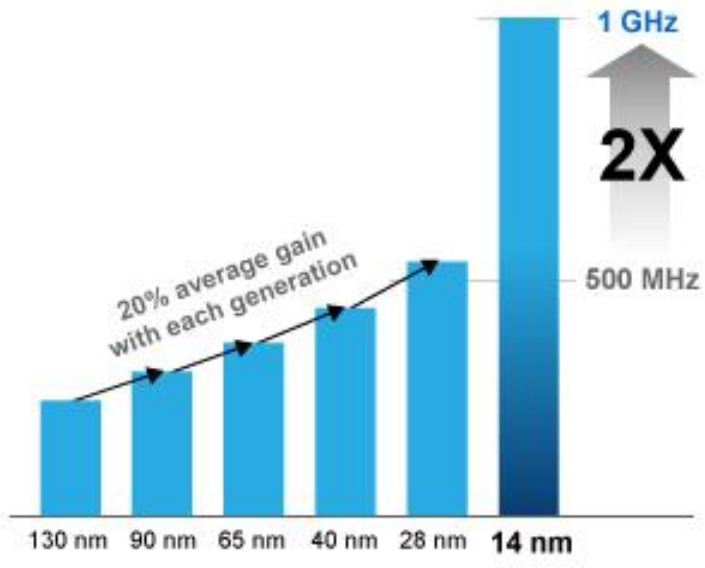
FPGA Complexity continues to rise

- Moore's law has kept FPGAs on the leading edge of process technology for decades
- FPGAs have gone from simple glue logic to the centre of complex systems
- Processor integration into FPGAs has taken this centralization further than ever before



Gordon E Moore



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Bring up of processors + logic in the past

- Lots of access to test points
- Discrete functions, loads of visibility

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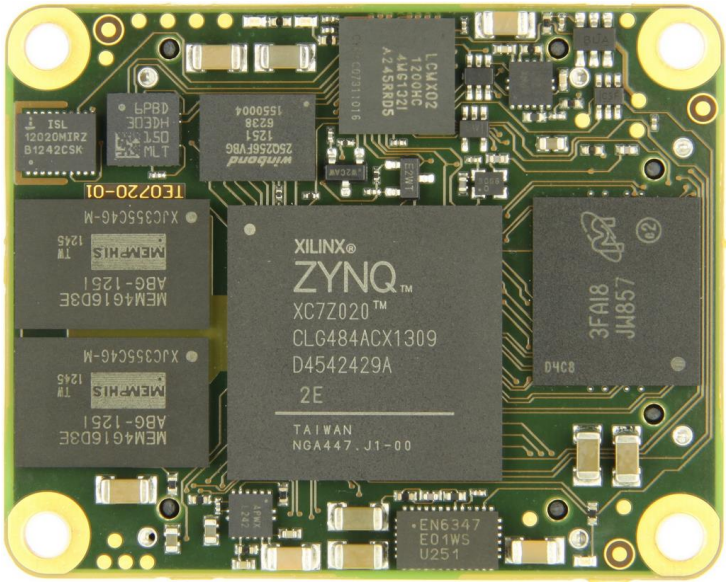
Bring up of modern processors in programmable logic – is it as easy?

- SoC FPGAs embed more functionality “under the hood”
- How do you bring up these devices with custom code?
- How to debug signals when things go wrong?
  - Where can I probe?



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Question:
What strategy should I use for bringing up my board? How Should I test it when things go wrong?

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System Bring up Strategy #1
Build the whole design and run it - “Vegas or Bust”

Not feasible for the majority of custom designs

Risk of failure too high – where to start debugging? Does it even power up?

Strategy #2 – Incrementally Piece together the design, testing as you go. The "Slowly Slowly" Approach

Far more likely to succeed

Classical FPGA Board Bring up

- Incremental interface bring up:
  - Interface based approach. This varies from customer to customer
  - Sometimes Critical interfaces first
  - Sometimes historically tricky interfaces first – if a customer has been burned!
  - Incrementally build up interfaces – sometimes in isolation, sometimes incremental, or logical blocks
    - Isolation to test functionality without crosstalk
    - Incremental, with environmental testing
    - Use on-chip debug tools to trace transactions and debug physical and logical errors and inject test patterns/data

Question: Can an embedded processor assist with this debug, or are they just something else to test?

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Hardened Processors have their own challenges

- First we have to get the processor running
  - Power, Clocks, resets
  - DDR, peripheral multiplexing

- Challenges
  - Fixed architecture – no bit swapping, no shim logic. Inverted a signal on a board? Limited options!
  - Incremental bring up of peripherals can be challenging in an OS environment. Vegas or broke? Bare metal minimal device drivers? Linux with device tree, enabling one peripheral at a time?
- Once we have the processor up what does that give us?
  1. The processor that we need for complex SoC designs
  2. **A powerful, configurable debugging and test engine on-silicon!**

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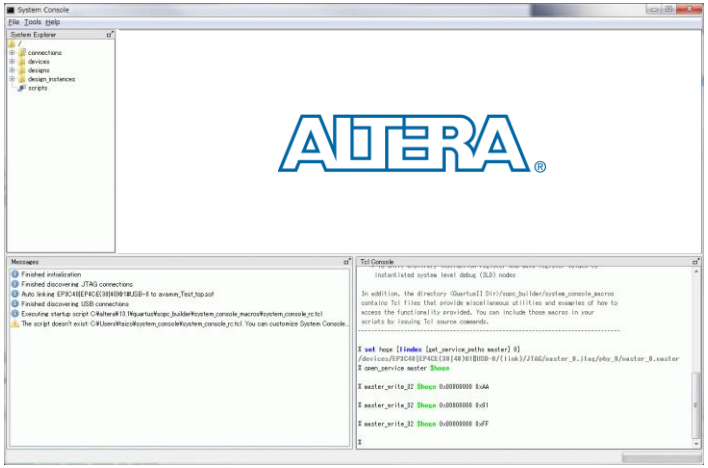
Solutions to debug visibility building up a system

- JTAG connections are essential to single-step a processor
- Ethernet connections are suitable for application debug
- But what about the debugging the FPGA?



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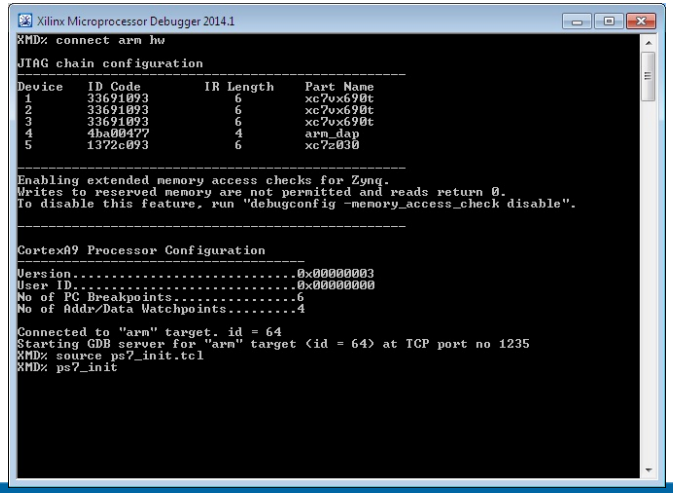

ChipScope Pro

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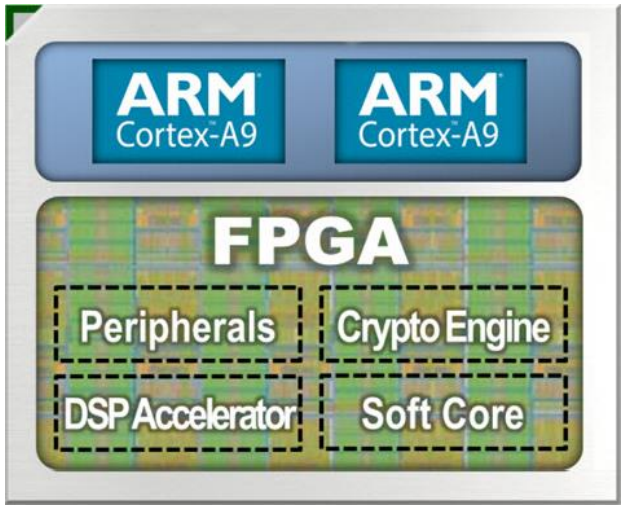
Debug and Deployment

- Debug in the lab can be bounded and straight forward
- Debug of a deployed system can be tricky
  - Chassis buildups can prevent JTAG access, this can also be by design
  - Debug may be needed in field trials when hardware is in final state

Can the processor aid board bring up?

- Integrated processors can bring benefits to board bring up
  - Processor is tightly coupled
  - Can reconfigure the FPGA
  - Processor system is “known good” (dependent on your PCB)
  - **Can act as a bridge to debugging tools**



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VPN

CPRI

Ethernet

OS

Server

Custom Applications

Configuration Control

Debug Hub

Logic

Logic

FPGA Programmable Logic

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Example demonstration

- Demonstration using Ethernet via an embedded FPGA processor for remote reconfiguration and in-system debug/test

Live Demo –

(What could possibly go wrong?)

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Can processors assist with board bring up?

[Military customer] – "We've used hard processors in FPGAs for years, and they have helped us bring the board up. They have always been a help and never a hindrance"

[Communications Customer] – "Without the processor, it would have taken much longer to prove out our board, especially as some of the IP has not been written yet"

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My conclusions

- Embedding a processor into an FPGA enables tighter integration
- A side effect of this is a tightly coupled **debug engine** available and at your disposal
- FPGAs by their nature are **RECONFIGURABLE.** Use this to your advantage during bring up and test.

What are your experiences?

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Thank You

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