A Package Fit for Purpose
NMI Roadmap Seminar April 2009

Changing the way the world connects

A Package Fit for Purpose

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Overview

- CSR Aim
- The ‘Connectivity Centre’
- CSR Markets and Packaging Requirements
  - Package Design Influences
  - Key Markets and Their Needs
- CSR Package Design
  - CSR Differentiation in Co-design
  - Driving out Cost
- Challenges for New Technology
- Future
- Summary

CSR's Aim

- **Lead the Supply of Short-range Wireless Solutions**
  - Lowest cost of ownership for its customers
  - Complete solutions
  - World-class supply chain
  - Excellent reliability

CSR's 'Connectivity Centre'

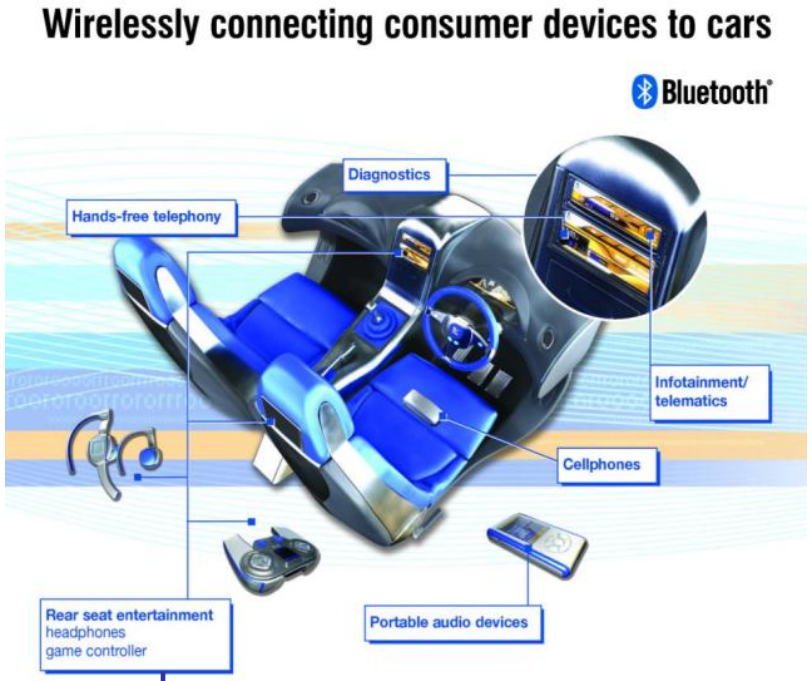
Package Design Influences

(2) CSR Markets and Packaging Requirements

- Automotive
- Headsets, PC’s, Consumer
- Cellular

Automotive

- **Automotive Applications**
  - Low-end PCB technology
  - Little RF design experience
  - Miniaturisation not critical
  - High Reliability



- **Package Considerations**
  - Coarse pitch
    - Array– 0.8mm or greater
    - Results in a larger, more expensive package
    - Emerging QFN – Peripheral pitch of 0.5mm is okay for many
  - CSR SiP reduces the customer's Bill of Materials, and RF design
  - System-in-Package Approach Makes Sense!

Headsets, PCs, and Consumer

- **Application**
  - Intermediate PCB, and PCB assembly, technology
  - Some RF design experience
  - Miniaturisation semi-critical
  - Programmability desirable
  - Price sensitive

- **Package Considerations**
  - Intermediate array pitch – 0.65mm, but can vary depending upon customer
  - Cost trade off is between package pitch/size and PCB technology
  - External or internally stacked Flash, some SiP
  - Example: New (lowest cost) BlueVox headset products use QFN

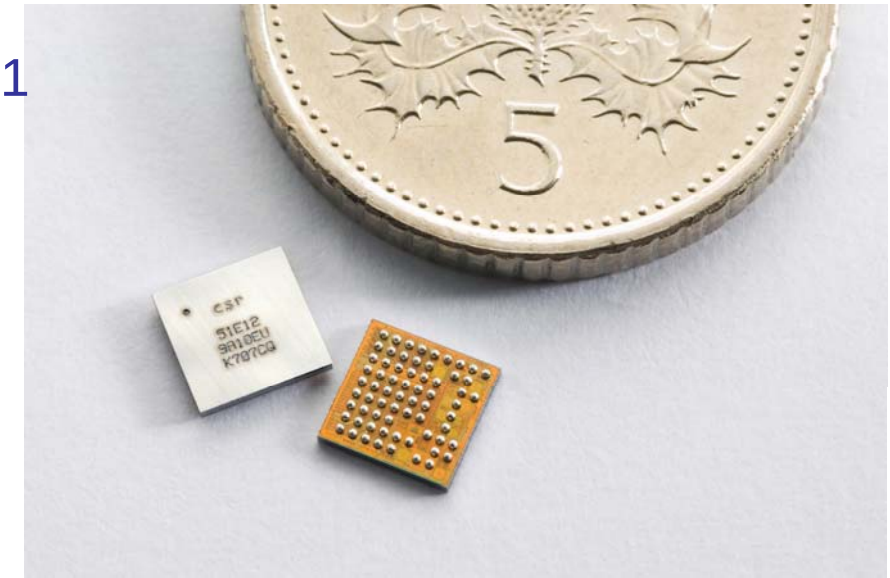
Cellular

- **Application**
  - High volume market 1B+ Phone Units / Year
  - High-end PCB technology and assembly
  - Good RF design experience
  - Miniaturisation critical
  - Cost critical

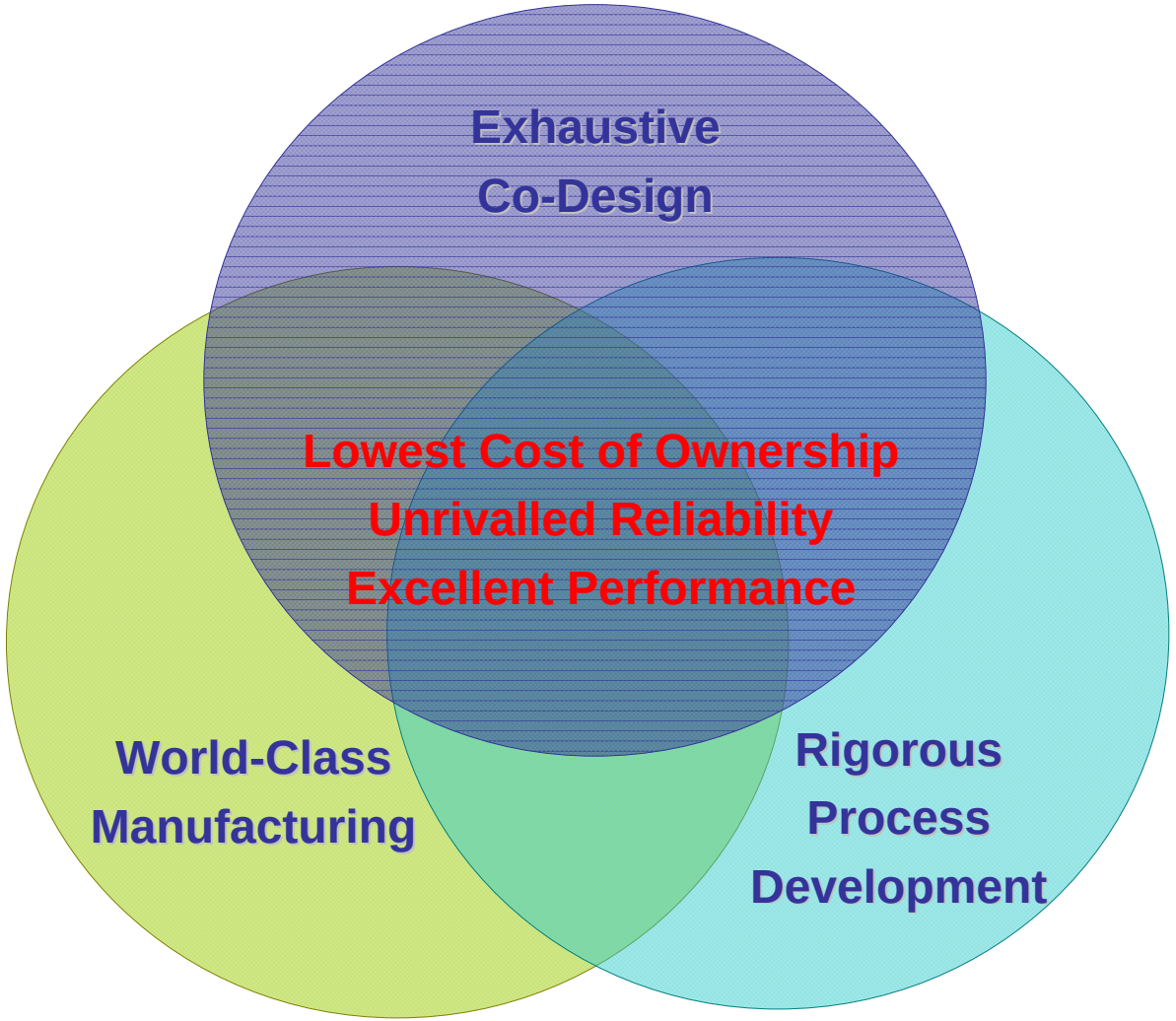
- **Package Considerations**
  - Fine ball pitch – 0.5mm or below
  - Smallest, lowest cost, package
  - ROM silicon/packages
  - Typically WLCSP

Current Handset Package of Choice

- **Wafer Level Chip Scale Packaging (WLCSP)**
  - Die-sized footprint, 0.6mm height
  - Proven board-level reliability – without underfill
  - More than 600Mu shipped by CSR
  - Regular array reduces surface mount alignment time
  - Pitch 0.5mm and 0.4mm
  - Moisture Sensitivity Level (MSL) 1

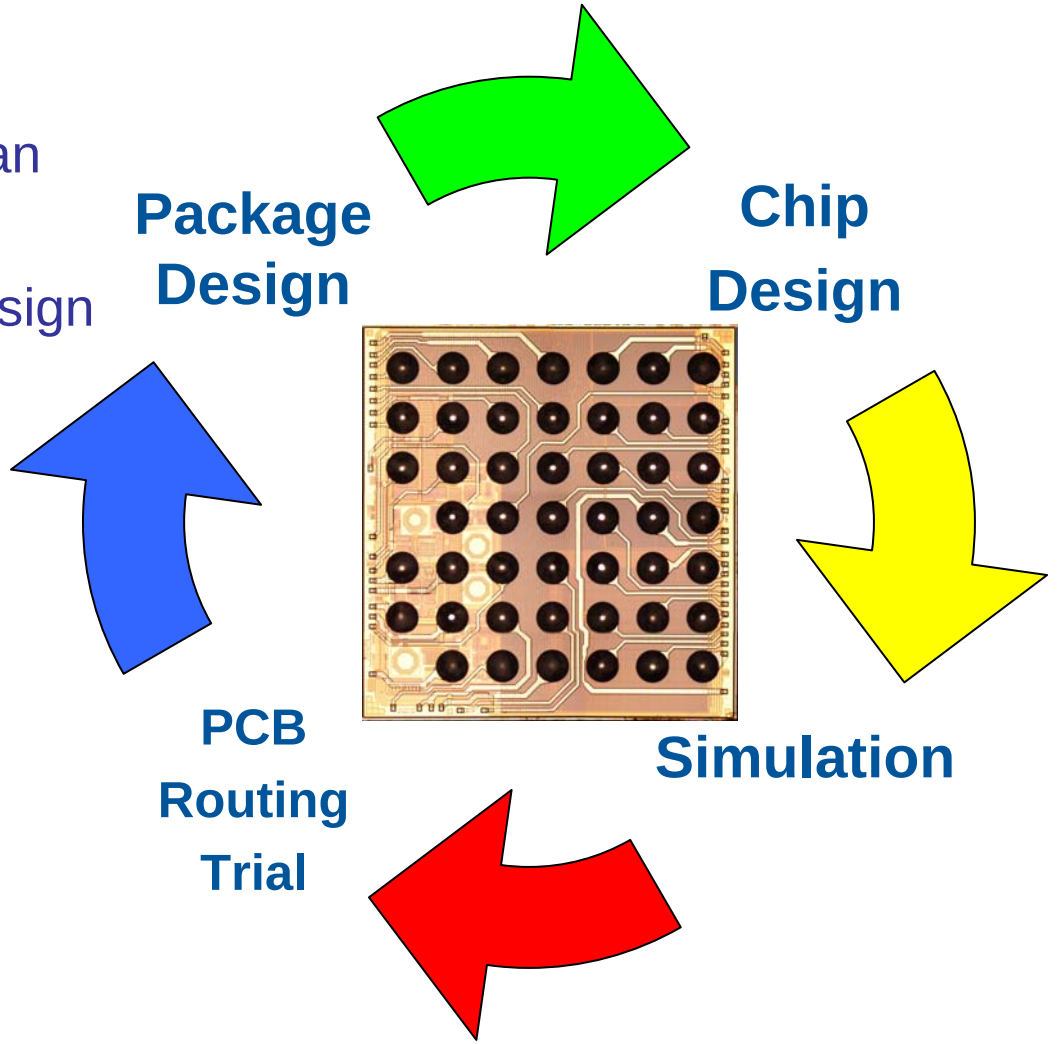


What Differentiates CSR's WLCSPs?

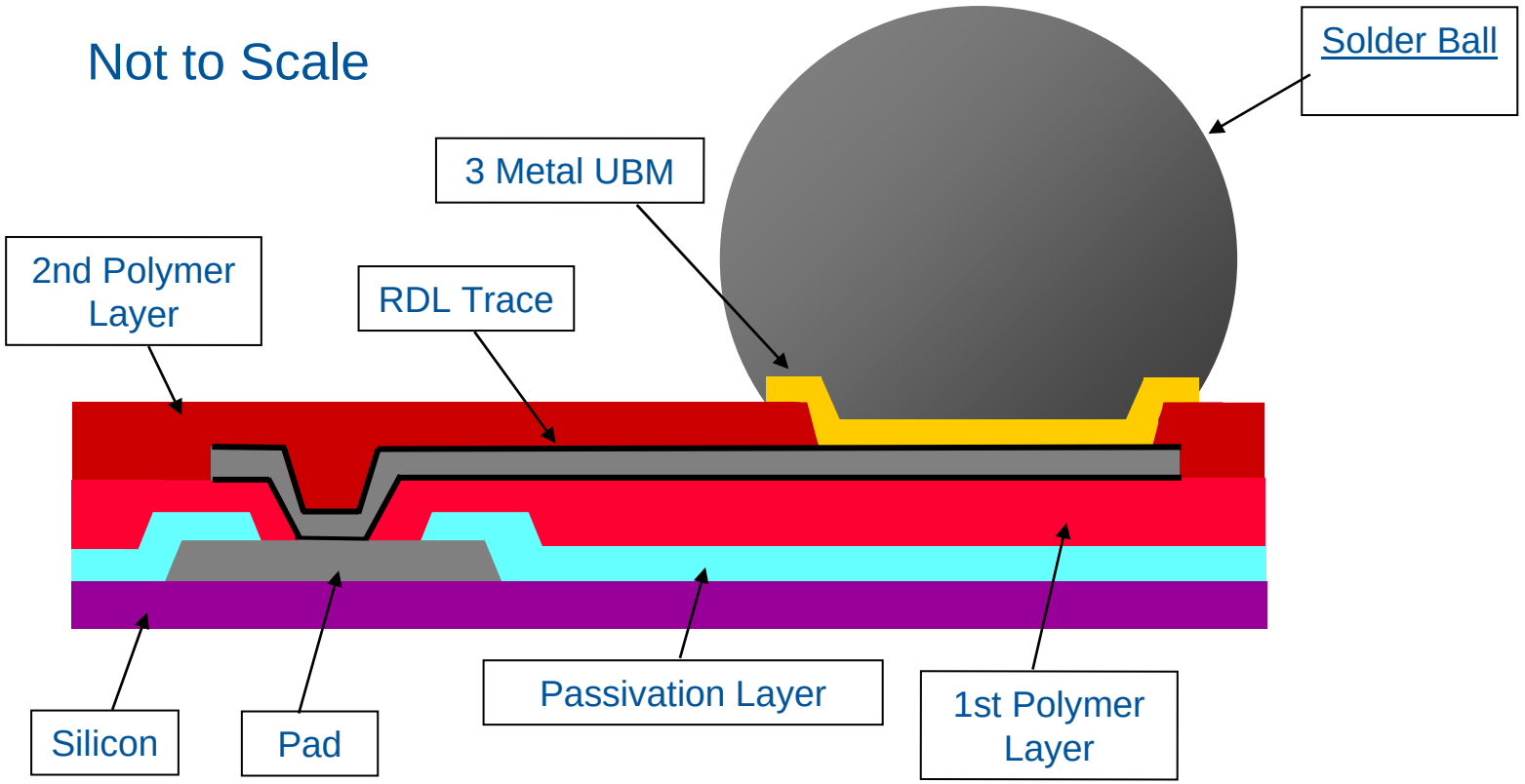


Silicon/ Package/ PCB Co-design

- **Process**
  - Co-design from first floor plan
  - IC cells robust by design
  - IC architecture robust by design
  - Iterative co-design process
  - Co-design for:
    - Application PCB routing
    - Different package styles
    - Test
    - Package process
    - IP Re-use
    - Support of SiP /Modules



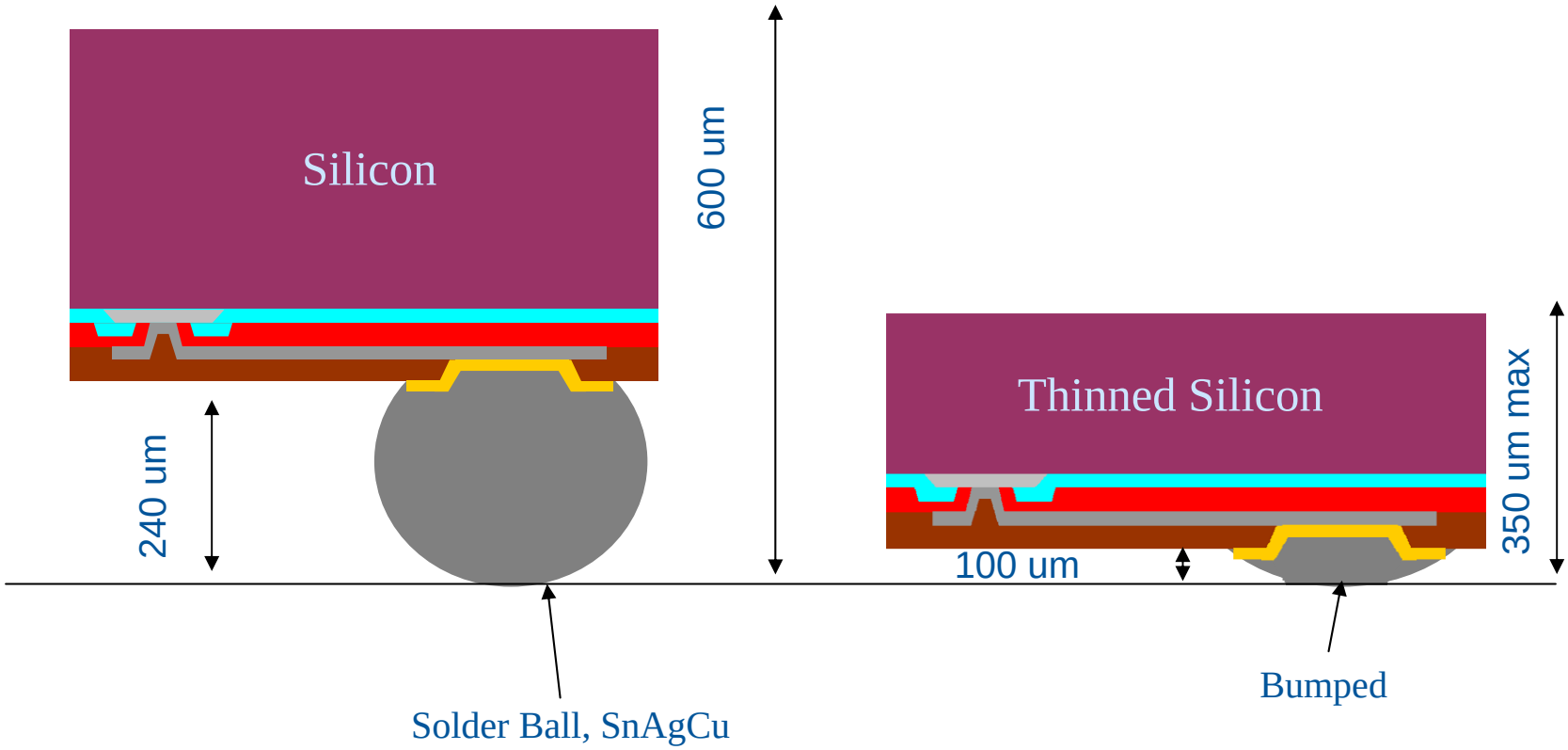
WLCSP Structure



WLCSP Evolution – Ultra-Thin WLCSP

WLCSP

Ultra-Thin WLCSP



BlueCore7™ – BT/ FM / GPS

World's smallest BT/ FM / GPS System-on-Chip

Co-Design at it's best

IMAGE WITHELD

0.4mm pitch

0.5mm pitch

UF6026 CSR's Co-design in WiFi

World's smallest WLAN 802.11 a/b/g SoC

Lowest cost of ownership

IMAGE WITHELD

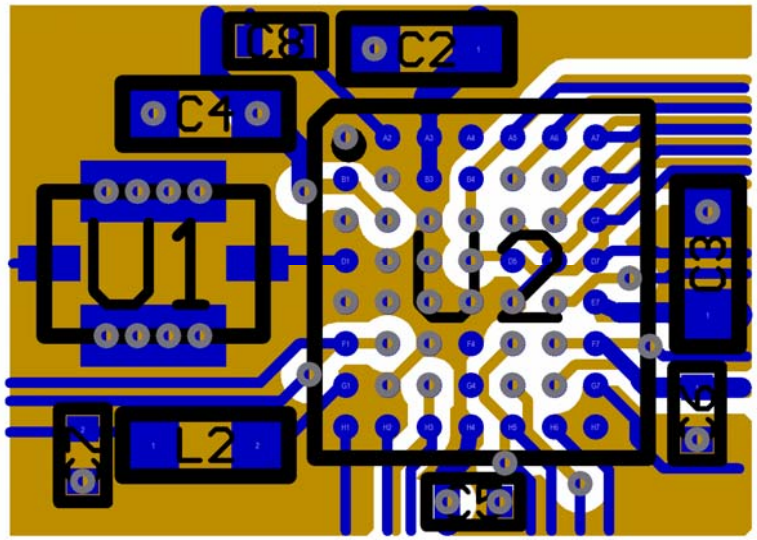
0.5mm pitch

CSR's Smallest Solution Size

IMAGE WITHELD

Co-design Benefits

- **Produces Simplified Packages**
  - Inherently reliable
  - Inherently high yield
  - Inherently low cost
- **Enables Regular-array WLCSP**
  - Faster SMT
  - Simplified PCB designs



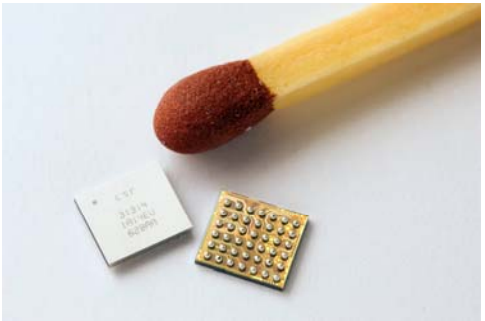
WLCSP Routing Trial On Low-End PCB Technology

- **System-level Simulation**
  - Improved Electrical, Thermal & Mechanical Performance
- **Products that Route Out on Low-end PCB and Modules**
  - Reduced PCB layer count
  - Lowest cost of ownership to CSR's customers

Driving Out Cost

- **Silicon**
  - Selection of the most cost-effective process node
  - Large (12”) wafer diameter for all new designs
    - Economy of scale for IC fabrication & packaging
  - Pin count minimised to facilitate WLCSP

- **Wafer Level Chip Scale Package**
  - Highly-efficient wafer-level process
  - Reliable on board – without costly underfill
  - Regular array aids customer SMT throughput



- **Final Test**
  - Extensive IC self test, for reduced test time
  - Most cost-effective test platform
  - Test strategy, for wafer sort and final test
  - Test “time is money”!

New Packaging Technologies

- Flip-chip BGA
- Wirebond Bare Die Stacking (2+)
- Thin-Die / UTCSP
- Integrated Passive Devices (IPD)
- Embedded Passives / Actives
- Fan-Out WLCSP
- 3D- Thru-Silicon Vias

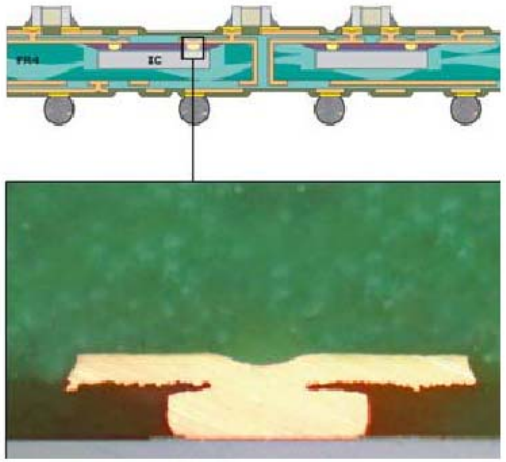
New Packaging Technologies – The Challenge

- **A compelling packaging technology will:**
  - Hit “the right” price point
  - Reduce total Bill of Materials
  - Be reliable
  - Grow revenue
  - …all whilst improving performance and size

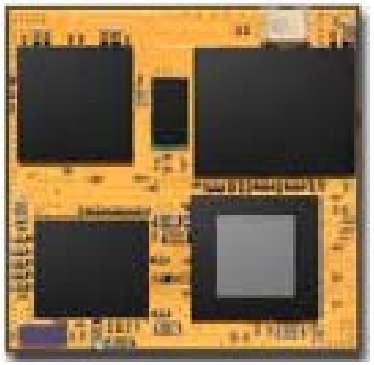
Example: Redistributed PCB with Embedded ICs

- **Pros**
  - Miniaturisation
  - Good thermal/ electrical performance
  - Greater integration

- **Cons**
  - Relatively immature technologies
  - Likely to be more costly than a SMD solution
  - Must be high yielding
  - Requires Known Good Die



Courtesy of Imbera



Courtesy of Freescale Semiconductor Inc

Future Trends

- Relentless Integration of subsystems / standards
- CSR Connectivity Centre

- CSR will extend standard WLCSP to maintain lowest cost of ownership
- CSR will continue to support Module customers

- New technologies expand options for package designers…but making the right technology choice is critical to product success

- Technology choice is not set to get any easier

Summary

- CSR's 'Connectivity Centre'
- CSR co-design to minimise cost of ownership
- Different Markets may need different packages
- CSR constantly reviews emerging technology options with its partners – to get the optimum solution
- Preferred approach is to maintain viability of WLCSP for future silicon nodes
- Co-Design of different products to meet market needs with a single piece of silicon is complex but this approach ensures a product "fit for purpose"

Thank-you for your Time

Any Questions?

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