"SiP & Passive Integration - options & directions"

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Astride the Packaging Roadmap
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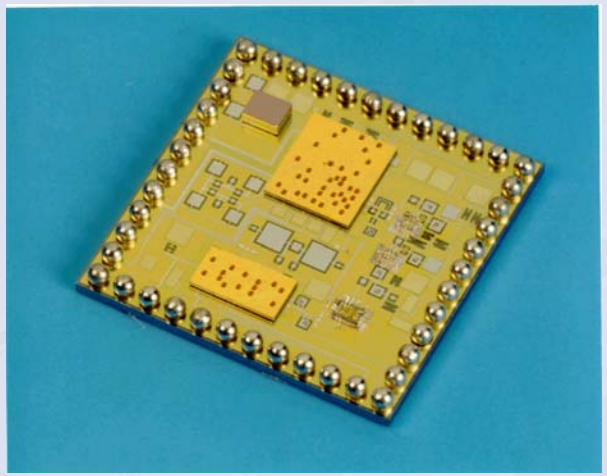
Outline

- *SiP concept & benefits*
- SiP categories and architectures
- SiP industry survey
- SiP application areas
- SiP options & future directions
- Summary & conclusions

Acknowledgement

- SiP: A Guide for Electronic Design Engineers
  - An EKTN funded TWI project
  - May 2008 – May 2009
  - Content
    - SiP Classes, benefits
    - Design routes, applications
    - SiP future trends, design guidance
  - Activities
    - Benchmark interviews with technology, design and applications leaders in Europe & USA
  - Deliverables
    - State-of-the-Art reports
    - SiP webinar series



Electronics Knowledge Transfer Network

ADEPT SiP

Photonics Knowledge Transfer Network

SiP definitions

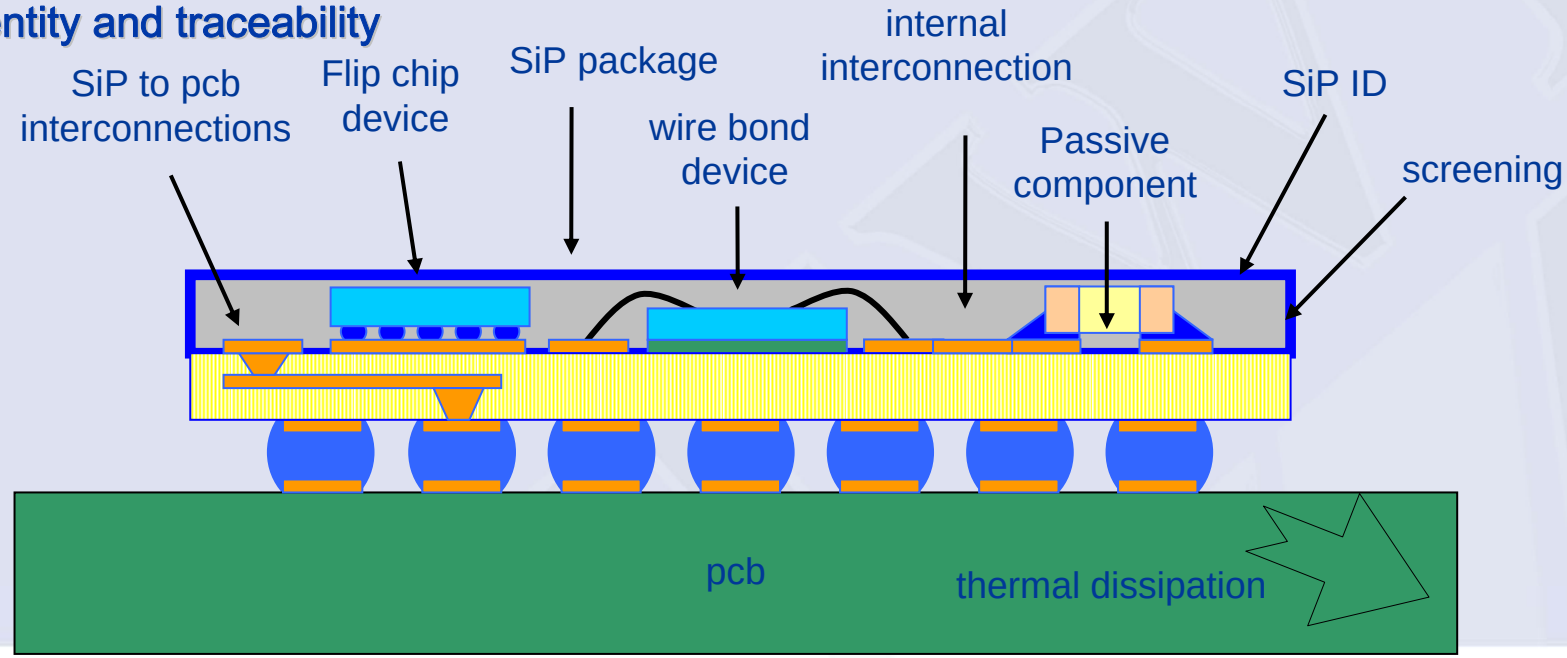
- *System-in-Package* is a functional system or sub-system assembled into a single package
- It contains *a single die or* two or more dissimilar die, *(typically) combined* with other components such as passive components (resistors, capacitors and inductors), passive networks (filters, baluns, antennas) and/or mechanical and/or optical components (MEMS, MOEMS, photonics devices)
- These components are mounted, embedded and/or integrated together on a substrate or package base to create a customised, highly integrated product for a given application

SiP definitions

- Precludes :
  - single die type stacked memory products
  - Stacked package structures (PoP, PiP)
- Aligned with heterogeneous integration trend
- Multichip Modules (MCM)
  - 1980s, processor modules, > 5 die, gated by cost, KGD issues
  - absorbed by SoC
- Multichip Packaging (MCP)
  - 1990s, used single chip infrastructure, < 5 die
  - SiP pre-cursor

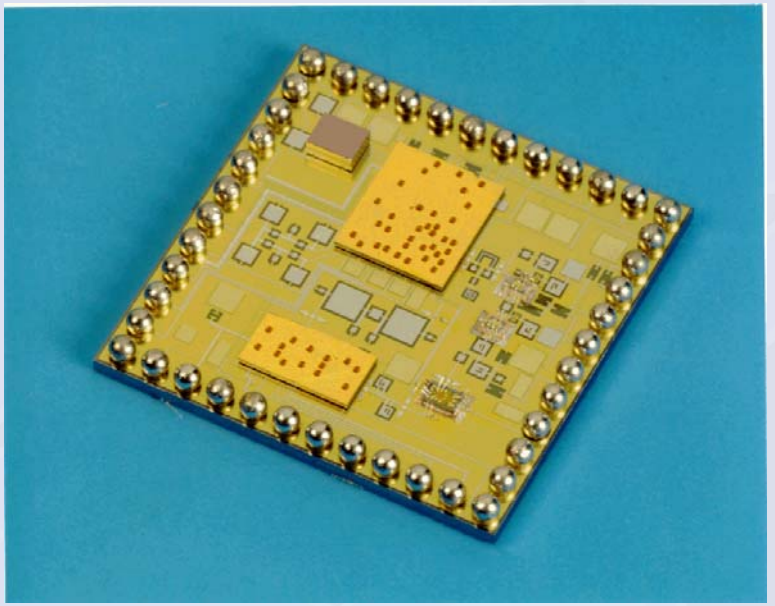
SiP packaging functionality

a) Internal electrical interconnections between SiP active, passive & mechanical devices
b) External electrical interconnections to the pcb at a supportable pitch
c) Environmental protection & encapsulation of the SiP integrated active, passive & other devices to allow test, handling, pcb assembly, mechanical & environmental reliability
d) Electrical screening between the SiP module and surrounding pcb–level components
e) A thermal dissipation path between the devices, components, module, pcb & system ambient
f) SiP identity and traceability



SiP benefits

- **System-in-Package (SiP)**
  - Smaller form factor
  - Flexibility
  - Faster time-to-market
  - Lower NRE
  - Mixing of technologies
  - Higher performance
    - signal propagation
    - power dissipation
    - noise & EMC performance
  - High added value
  - IPR protection



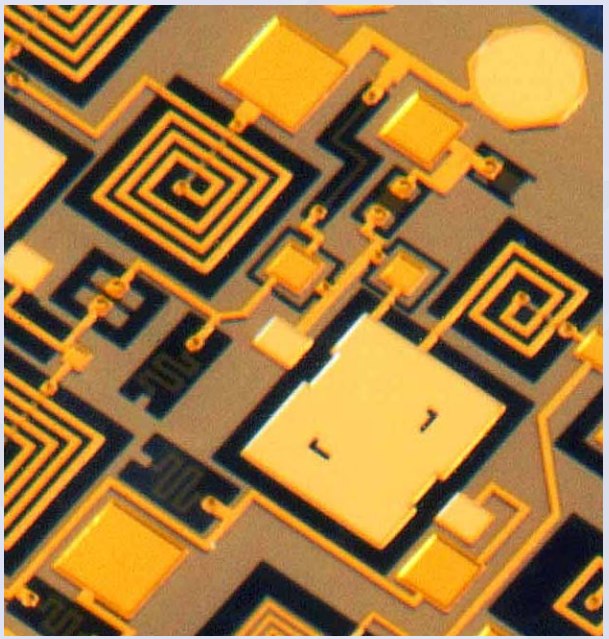
SMT passive components

On a typical PCB, SMT passives comprise:

- **91% of components**
- **29% of solder joints**
- **41% of board area**
- **per year, ~ 1 trillion passives surface-mounted**
- **~ 0.5 cents purchase + 1.3 cents “conversion”**
- **Passives numbers growing**

Integrated passives benefits

- Improved performance
- Reduced size & weight (2 to 10 fold)
- Higher functional density
- Reduced mounted component count
- Reduced costs per function
- Reduced wiring demand
- Greater SMT throughput
- Improved reliability & EMC emissions
- Continuous component values
- Lead-free technology
- High added value & IPR protection



Outline

- SiP concept & benefits
- *SiP categories and architectures*
- SiP industry survey
- SiP application areas
- SiP options & future directions
- Summary & conclusions

SiP categories, architectures

- Hierarchical structure

SiP category								
Active devices								
packaging	bare die			CSP			other	
Die placement	2D				3D			
Chip-to-chip	wire bond		flip chip		solder ball		TSV	
Chip-to-next-level	wire bond		flip chip		solder ball		TSV	
Passive devices	SMT				IPD			
Other devices	tbd							
Packaging platform	leadframe	LTCC			laminate		thin-film	
					mounted	embedded	substrate	interposer
		integrated passives			integrated passives		integrated passives	

SiP categories, architectures

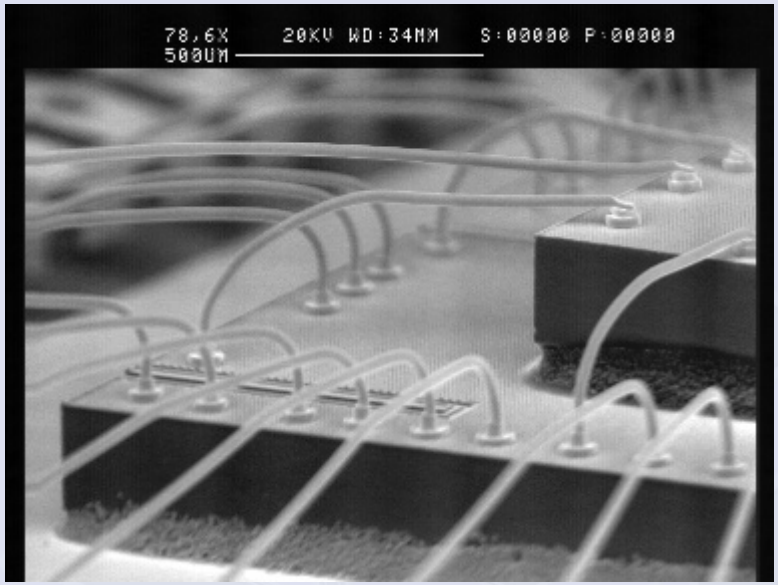
- The first class of SiP categorisation
- Active devices
  - *Technologies: CMOS, BiCMOS, bipolar, GaAs ..*
  - *active device packaging (if any)*
  - *die placement architectures*
  - *chip-to-chip and chip-to-next-level interconnection technology*

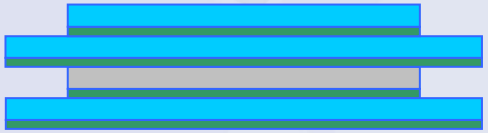
SiP categories, architectures

- *Device packaging categories*
  - Bare die
    - important to use Known Good Die (KGD)
    - ensures high SiP manufacturing yield
  - Chip Scale Packaged (CSP) die
    - inherently high KGD level
  - *Conventionally packaged devices*
    - *occasionally*
    - *area and headroom overhead*

SiP categories, architectures

- *Die placement architectures*
  - 2-dimensional arrays
  - 3-dimensional, stacked die structures
    - die thinning to minimise stack headroom
    - spacers to allow wire bond access

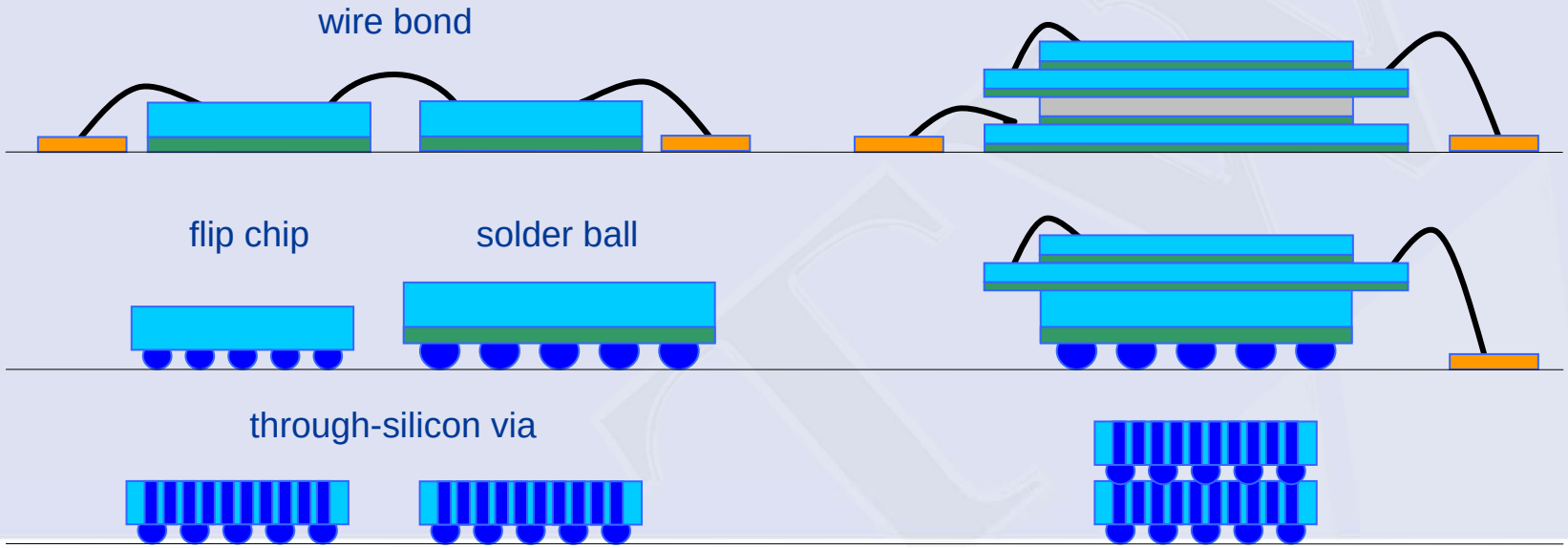




Source: Unisem

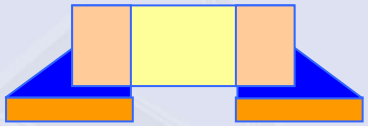
SiP categories, architectures

- *Chip-to-chip, chip-to-next-level interconnect*
  - wire bonding
  - flip chip and solder ball bonding
  - Through-Silicon-Vias (TSVs)



SiP categories, architectures

- The second class of SiP categorisation
  - *Passive components*
    - SMT passives
      - standard footprints
      - issues at 0201, 01005
      - E-series value steps
    - IPDs
      - thin-film on glass, silicon
      - networks, arrays
      - solder ball, CSP format
      - quasi continuous values



SiP categories, architectures

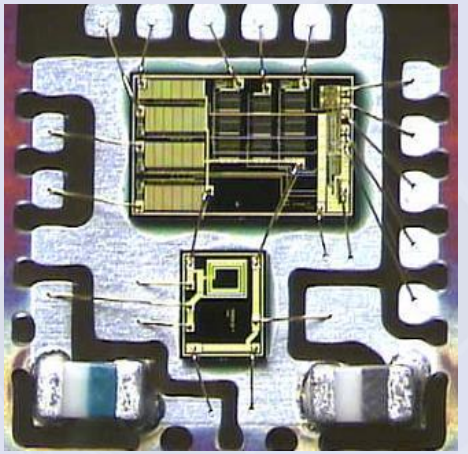
- The third class of SiP categorisation
  - *Mechanical and optical device structures*
    - MEMS, MOEMS
      - Special packaging needs
      - Hermetic sealing
    - Optical devices
      - Sources, detector devices
      - Precision alignment needs
      - Wave-guide, fibre, lens interfacing

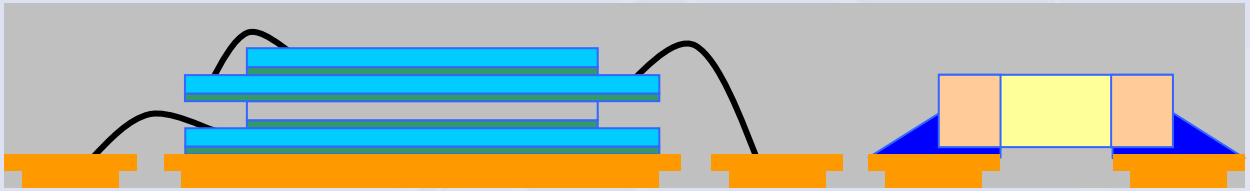
SiP categories, architectures

- The fourth class of SiP categorisation
  - *SiP packaging platform categories*
    - *leadframe*
    - *LTCC*
    - *laminate*
    - *thin film substrate*

SiP categories, architectures

- leadframe packaging platform
  - DFP, QFP, QFN
  - metallic leadframe
  - lower pin-count
  - high thermal dissipation SiPs

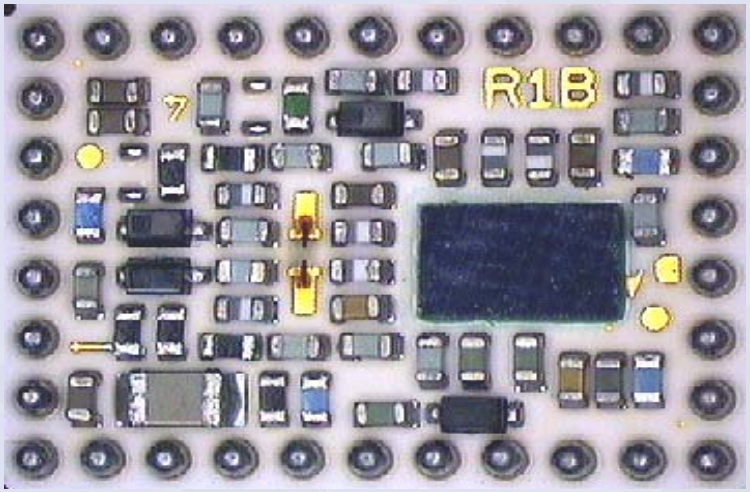


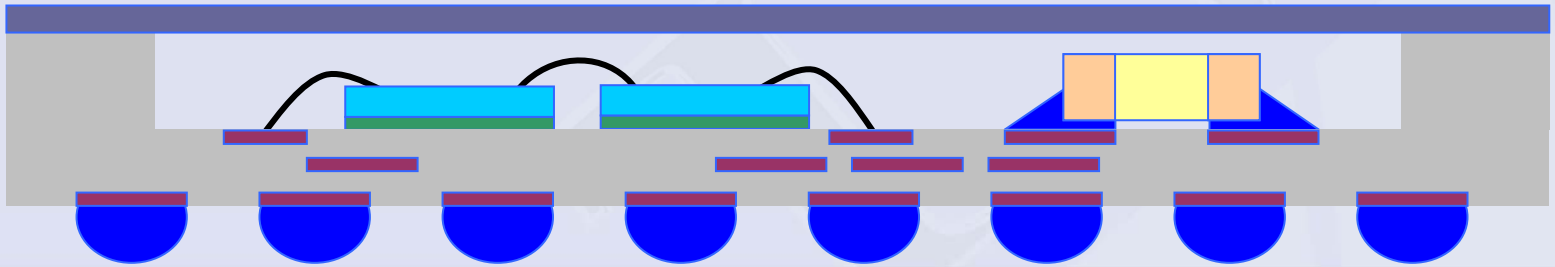


Source: Unisem

SiP categories, architectures

- LTCC packaging platform
  - glass-ceramic, laser vias, printed conductors
  - laminated & fired
  - print resolution, shrinkage limitations
  - cavity package option
  - integrated passives capability

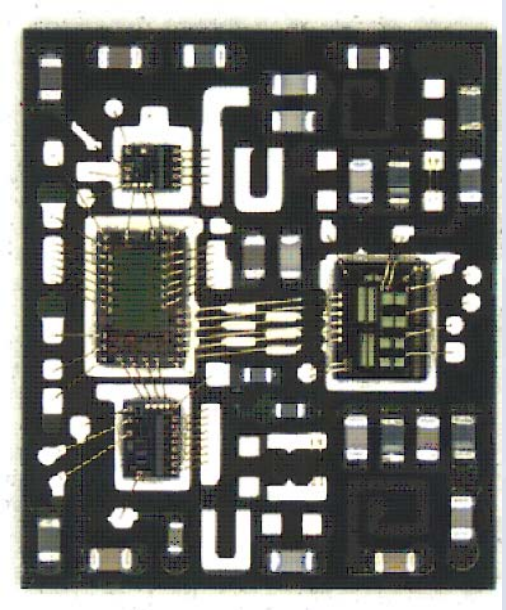


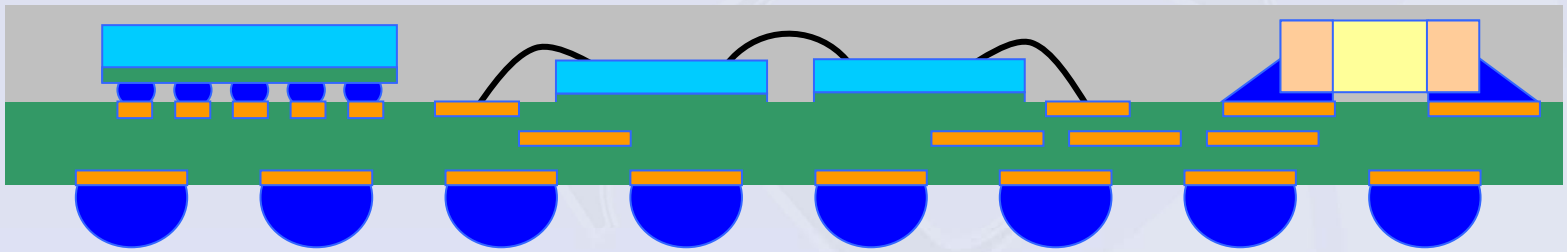


Source: Carsem

SiP categories, architectures

- laminate packaging platform
  - surface mounted or embedded components
  - integrated passives capability

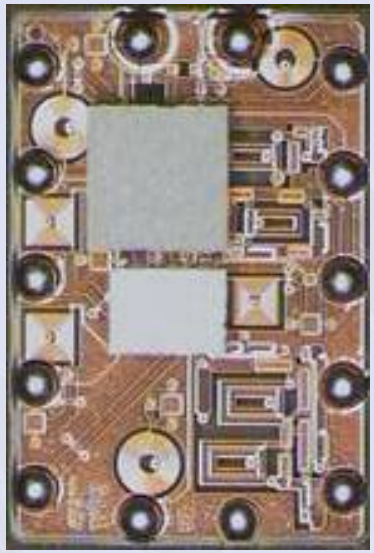


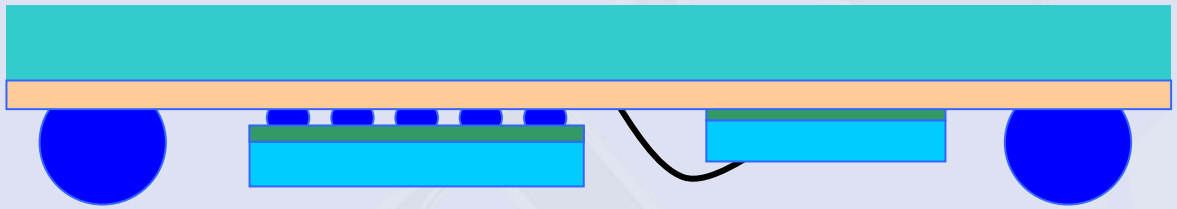


Source: RFMD

SiP categories, architectures

- thin-film substrate packaging platform
  - SiP package platform
  - thin-film interposer
  - high density integrated passives capability





Source: STMicroelectronics

SiP packaging platform comparison

Platform class	*leadframe*	*LTCC*	*laminate*	*Thin-film*
Key attributes				
I/O count	low-medium	high	high	low-medium
Interconnection density	low	medium	medium	high
Patterning accuracy	low	medium	medium	high
Integrated passives	no	full range	part/full range	full range
Thermal dissipation	high	medium	low-medium	medium-high
Reliability	high	high	high	high
Cost per unit area	low	medium	low	high
Primary difficulty	Interconnection density	shrinkage and accuracy	materials, interconnection density	cost
Primary advantage	Thermal dissipation	maturity	cost	Functional density, performance
Optimum size, cm^2	< 5	< 10	< 25	< 2

Integrated passives comparison

Platform class	***LTCC***	***laminate***	***Thin-film***
substrate type and manufacture	printed and fired multi-layer glass-ceramic	FR4 panel, HDI build-up	silicon/glass wafer
Inductor materials	~10 μm Ag alloys	~ 12 - 35 μm Cu	2 - 5 μm Al or Cu
Inductance density	medium	medium	high
Inductor quality factor	medium	Medium-high	high
Capacitor materials	Glass-ceramic dielectric or ferroelectric based	Thin laminate, polymer thick-film or ceramic thick-film	SiN, anodised Al, Ta in 2D or 3D formats
Capacitance density range	1 - 100 nF/cm^2	0.3 - 150 nF/cm^2	1 - 80 nF/mm^2
Resistor materials	Conducting oxide-dielectric mixtures	Ni(P), polymer thick-film, ceramic thick-film	NiCr, TaN, SiCr
Resistivity	10Ω - 10MΩ/square	100Ω - 10KΩ/square	10Ω - 1KΩ/square
Component accuracy	medium	low-medium	high
Component density	50/cm^2	25/cm^2	200/cm^2

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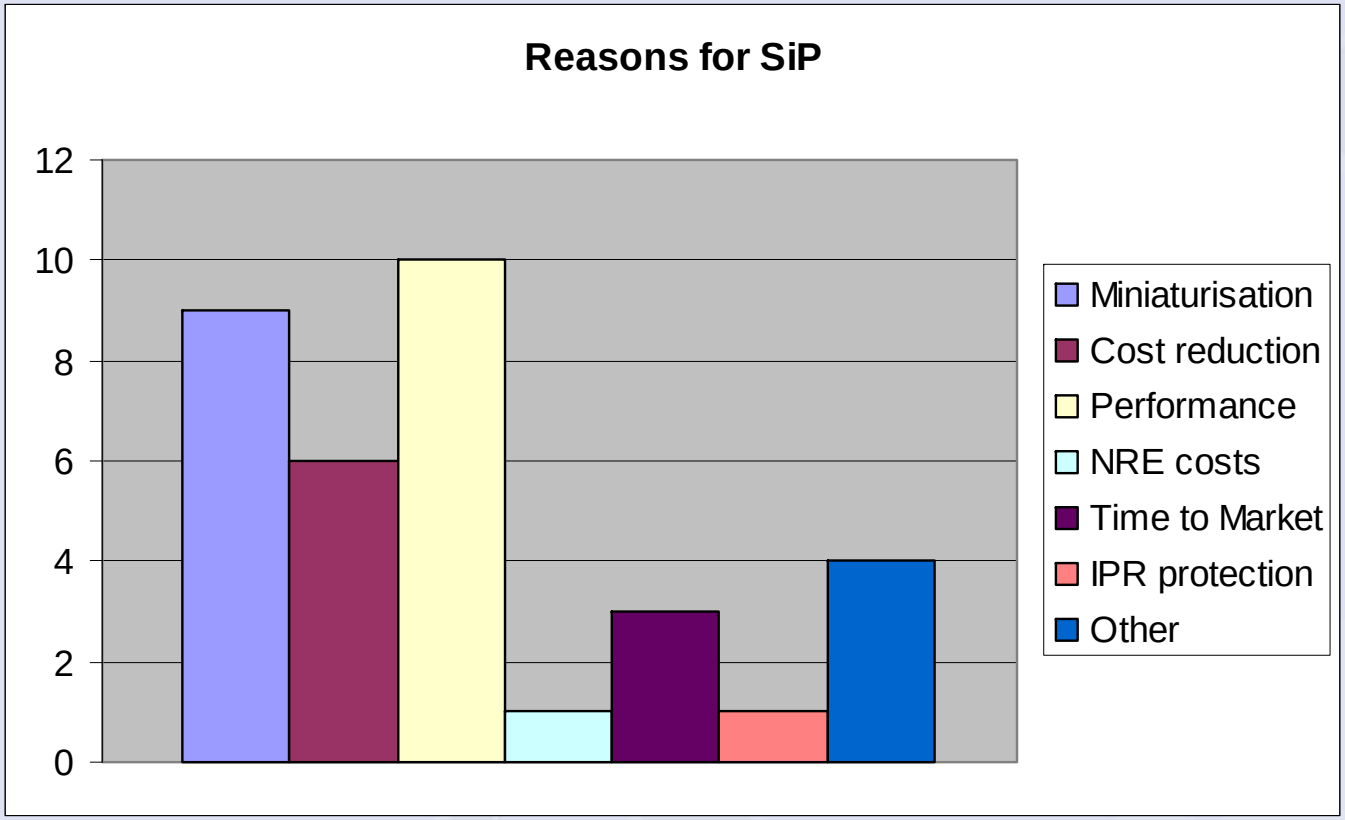
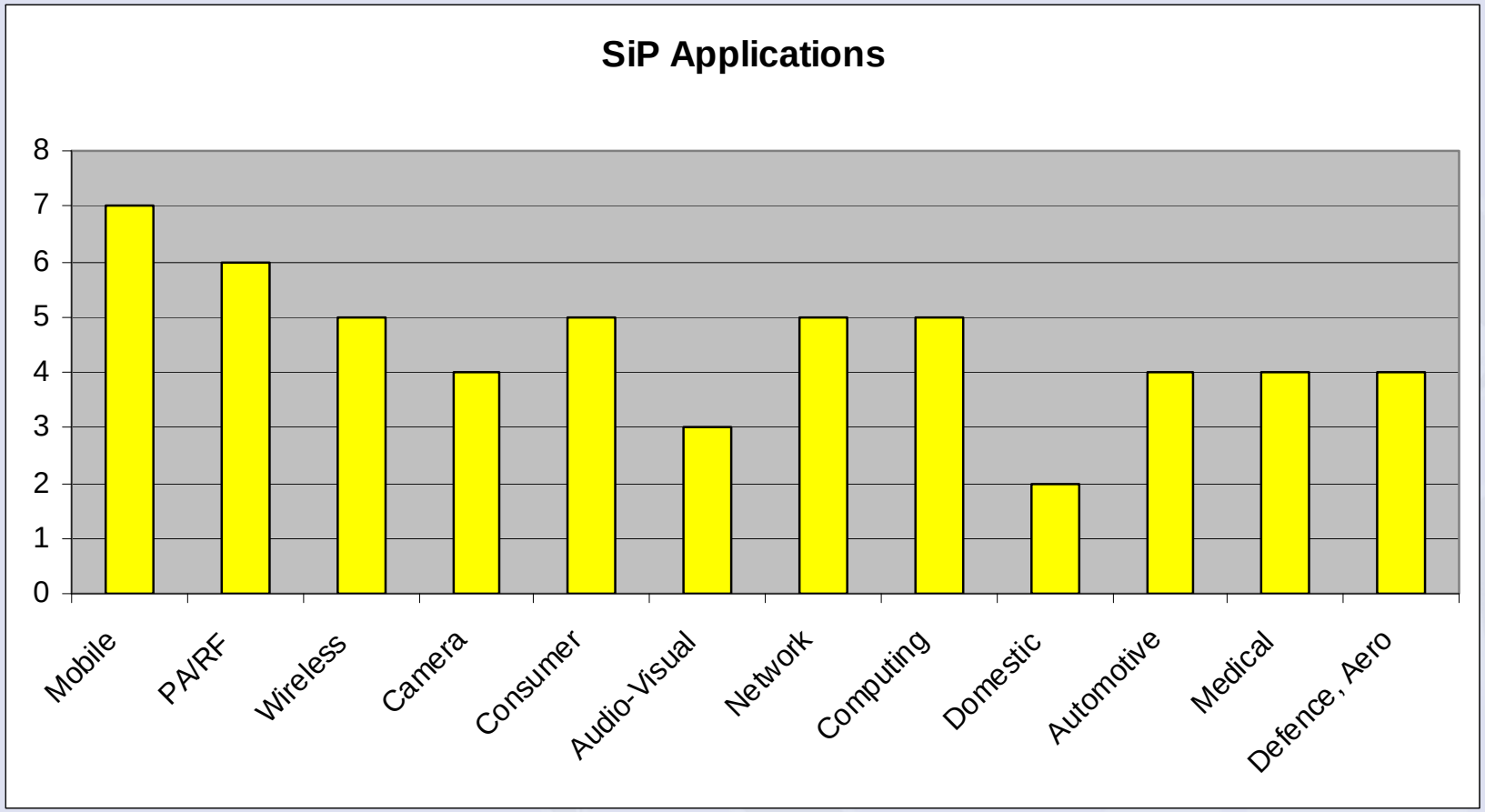
SiP industry survey

- Company name, address, contact details
- Your reasons for adopting SiP
- Your position in the SiP supply chain
- SiP application example data collection
- SiP technologies employed in the application example
- SiP design tools, design route employed in the application example
- Willingness to supply SiP technology example image(s)

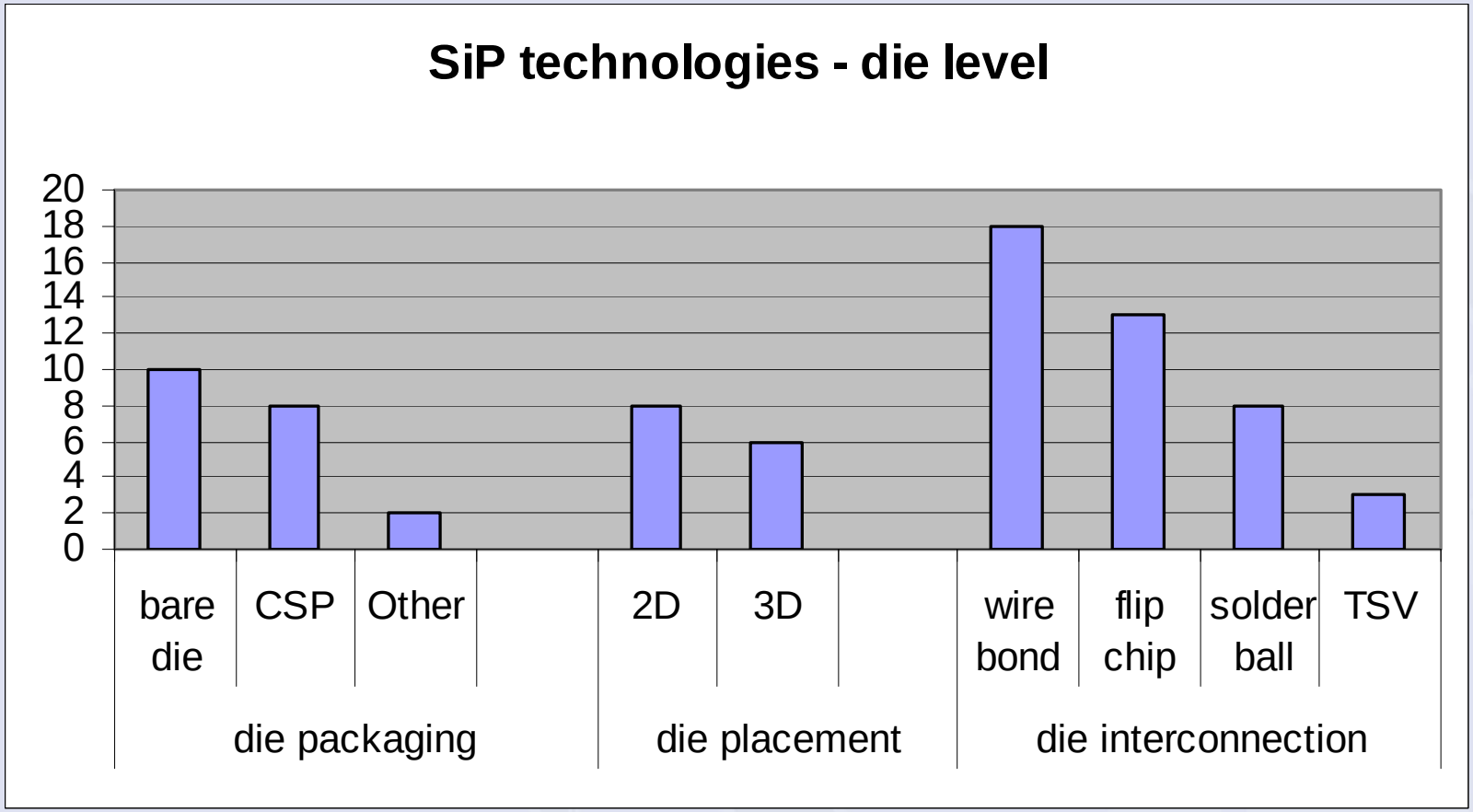
Reasons for adopting SiP



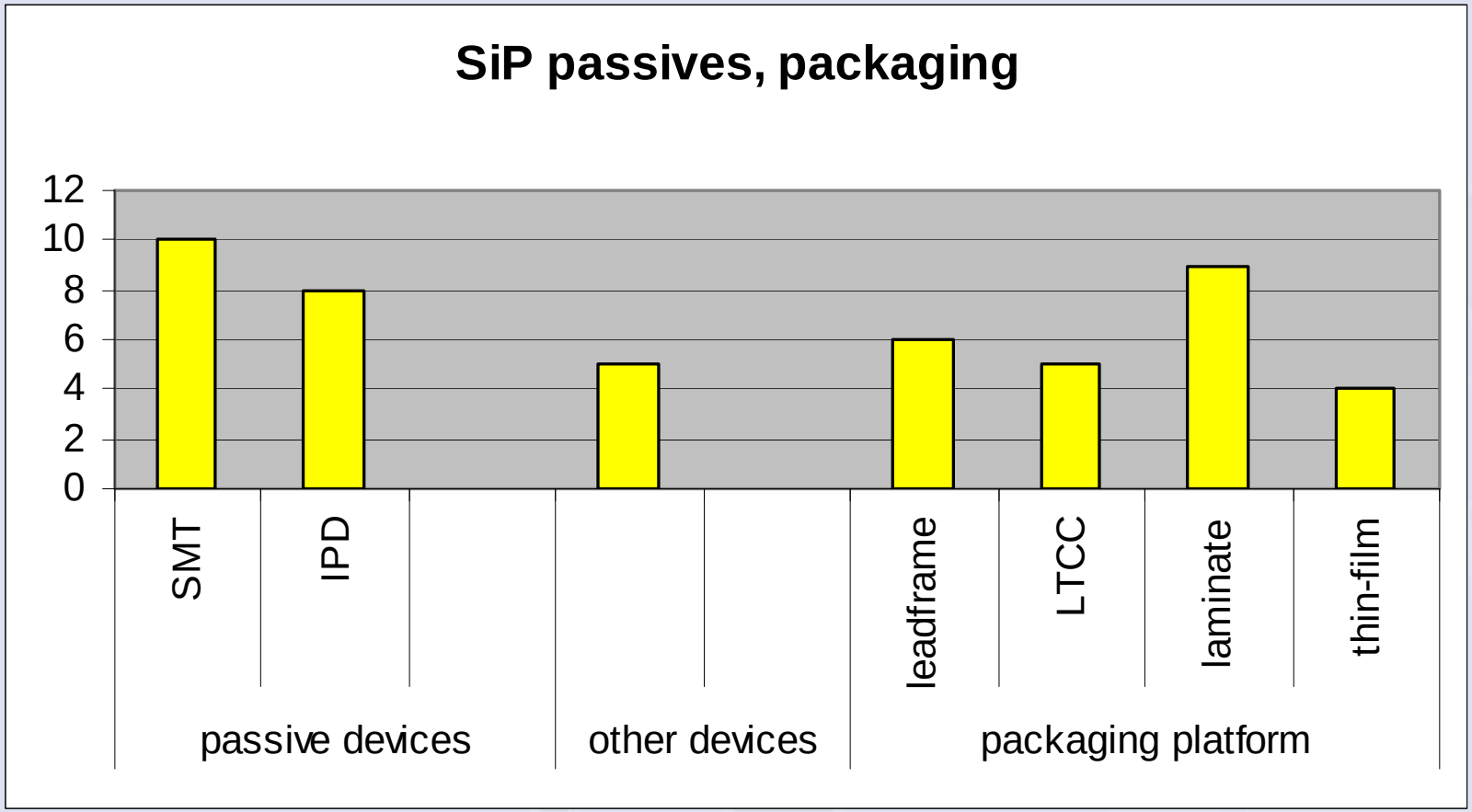
SiP Applications



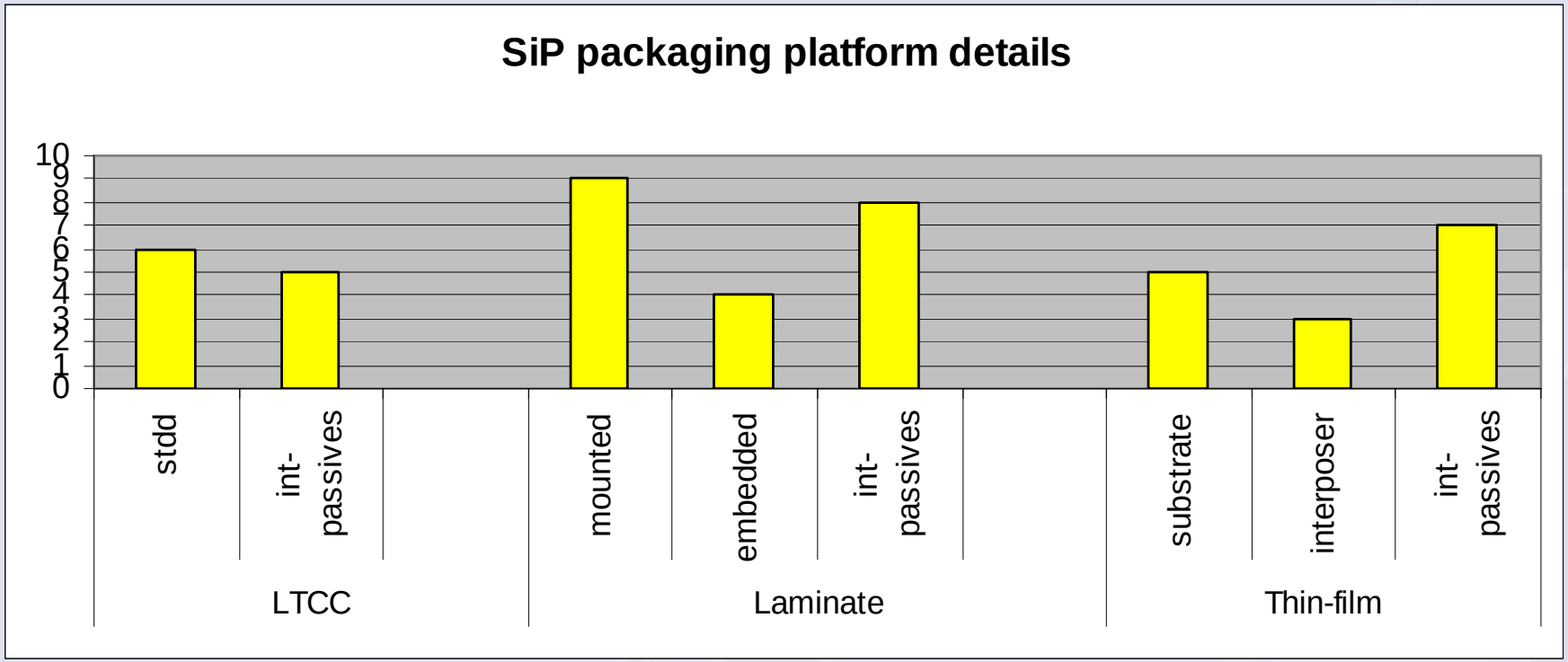
SiP technologies



SiP technologies



SiP technologies



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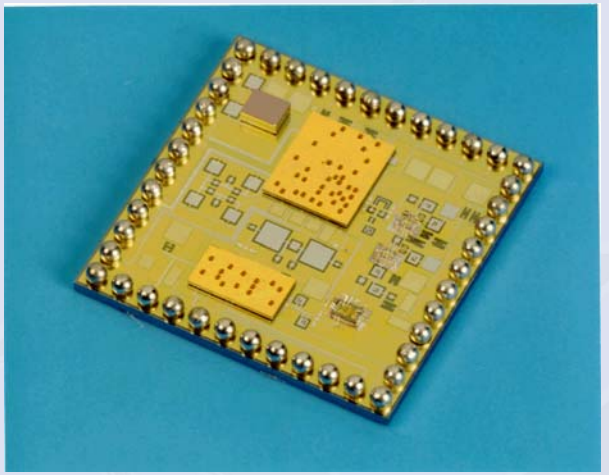
SiP options

- Many partitioning options
  - SoC, SiP
  - pcb, LTCC, laminate, thin film
  - hierarchical design helpful
  - easy interface transfer helpful



- Partitioning key to size, cost, performance
- Opportunities for chip-package co-design
- Performance & cost-per-function Figures-of-Merit

SiP directions

- Time-to-market is key
  - Improved design routes
  - Adoption of packaging platform & IPD PDKs
  - SiP co-design
  - SiP/SoC iterations
- Functional density is key
  - Growing adoption of flip chip, IPDs, TSVs
- Cost-performance is key
  - Early design partitioning
  - Larger substrate processing formats

Summary & Conclusions

- SiP & passive integration
  - Concepts & benefits outlined
  - Categories & architectures defined
  - Industry survey results presented
  - Application areas reviewed
  - Technology options & directions indicated

Thank you for your attention

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