Design for Variability efforts in Europe – The REALITY project

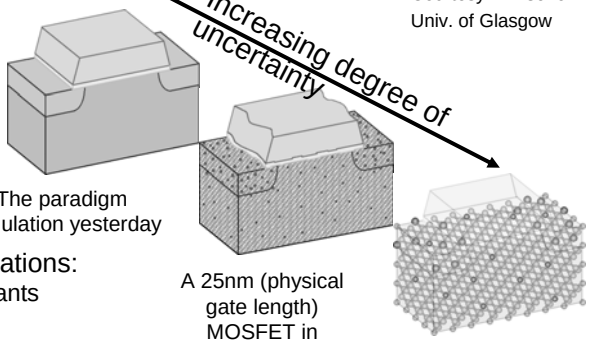
REALITY: Reliable and Variability tolerant System-on-a-chip Design in More-Moore Technologies

Presenter: Miguel Miranda, IMEC, Belgium

NMI 2nd International Conference on CMOS Variability – London May 12-13

The next generation MOSFETs are atomic scale devices

Courtesy A. Asenov
Univ. of Glasgow



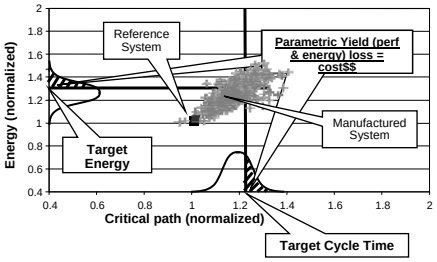
The paradigm simulation yesterday

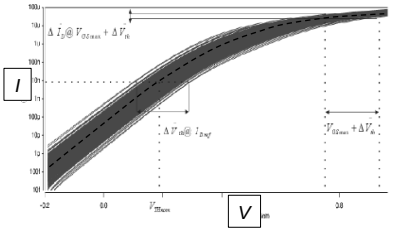
A 25nm (physical gate length) MOSFET in production today

A 4.2nm MOSFET in production in 2023

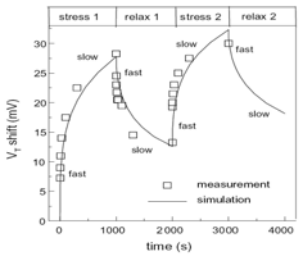
- Intrinsic Process Fluctuations:
  - Random discrete dopants
  - Line edge roughness
  - Interface roughness
  - Poly silicon gate
  - Strain
  - High-k structure
  - Gate tunnelling
  - ….

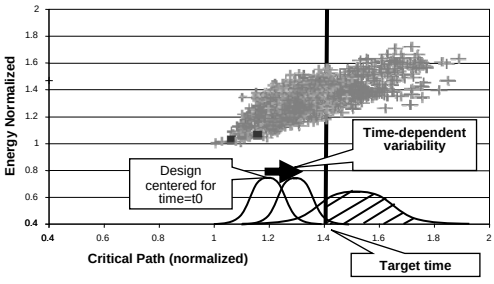
Focus is intrinsic device variability and its impact on design





With some outlook on the impact of degradation effects due to ageing





Overview

- Motivation for the project
- General project objectives and innovation
- Overview of research activities and current status
- Conclusions

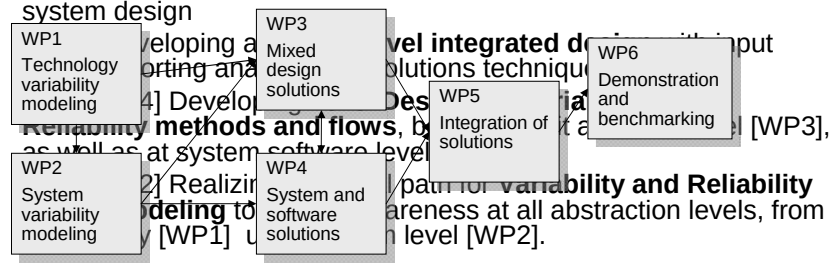
General project objectives

- (a) Analysis of the system in terms of performance, power and yield/reliability of manufactured instances across a wide spectrum of operating conditions.
- (b) Solution techniques to mitigate impact of yield/reliability issues of integrated circuits, at component, circuit, and architecture and system design.

Overall project approach

Six technical work packages conceived for a final goal: "**build reliable system using unreliable components**":

- [WP6] Demonstrating the feasibility of the project goal for sub-32nm system design
- [WP3] Developing a **…vel integrated d…** …put …orting ana… …olutions techniqu…
- [WP4] Develop… **Des…ia…** **Reliability methods and flows**, b… …t a… …l [WP3], as well as at system software level
- [WP2] Realizi… …l path for **Variability and Reliability Modeling** to… …areness at all abstraction levels, from … [WP1] u… …n level [WP2].
- From January 2008 till June 2010



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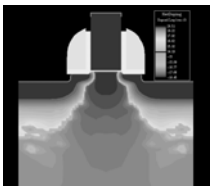
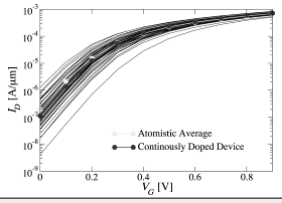
  - Modeling:
    - Technology
    - Circuit to System
  - Solutions:
    - Circuit level
    - System level
  - Project Integration & Benchmarking
- Conclusions

Technology Modeling (1): Model the statistical variability at 45nm and 32nm

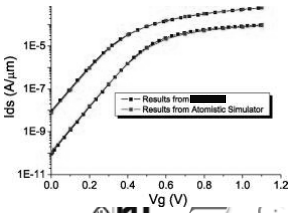
Receive device description



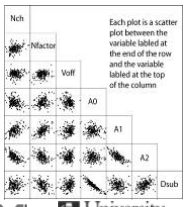
Introduce IPF sources



Calibrate our simulator



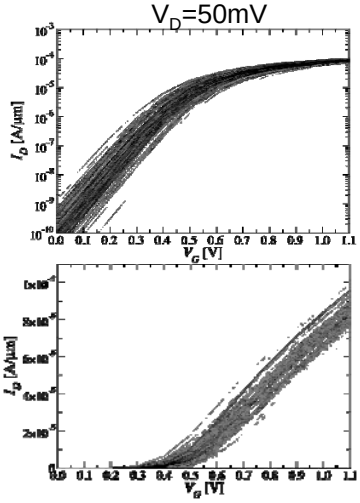
Extract compact model param.



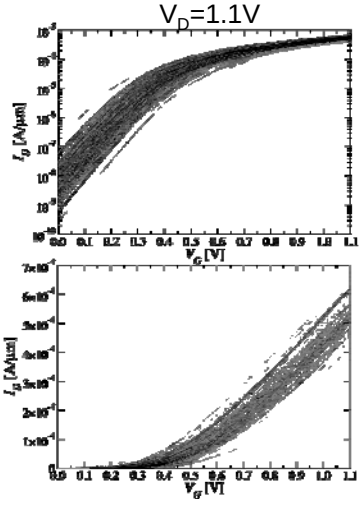
Technology Modeling (1): Status

devices: Simulated set of I-V characteristics of n-channel

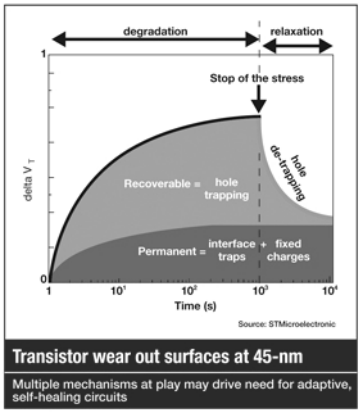
V_D=50mV

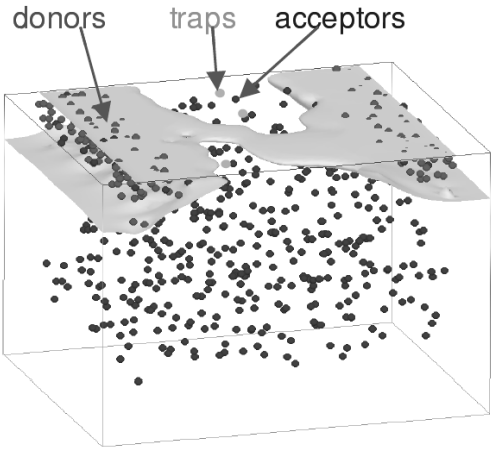


V_D=1.1V

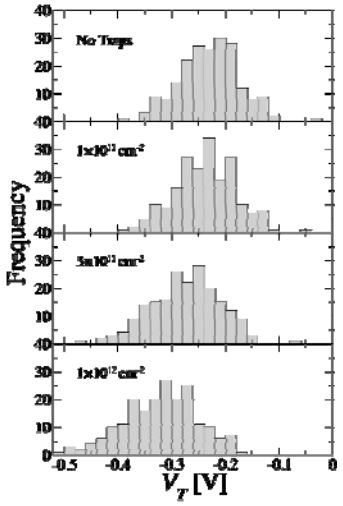


Technology Modeling (2): Model the statistical reliability at 45nm and 32nm

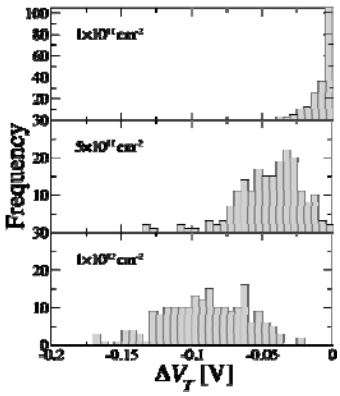




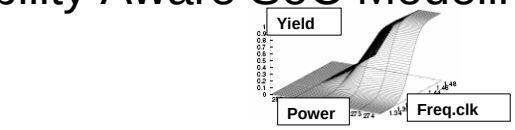
Technology Modeling (2): Status



V_D=-1.1V



Device to System Modeling: Holistic Variability Aware SoC Modeling



Start: Architecture level description (RTL) and simulation bench (WP5)

END: SoC Level Yield Model (WP6)

Word level activity

Statistical Analysis of Architectures (T2.4)

SoC netlist

Statistical Analysis of Digital Components (T2.3)

Statistical Analysis of macro-blocks (SRAMs, Register Files, etc, T2.2))

Bit level activity

Standard Cell netlist

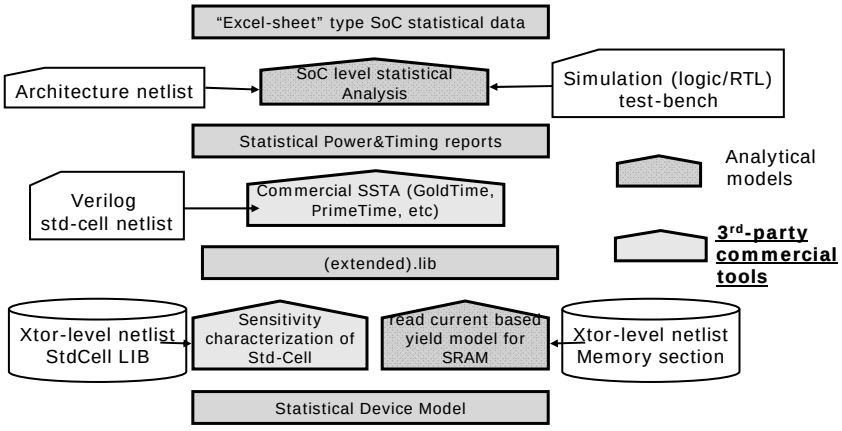
Statistical Characterisation of Library Cells (T2.1)

Transistor netlist

START: Variability aware Compact Device Models (WP1)

Variation Aware Information Format (T2.5)

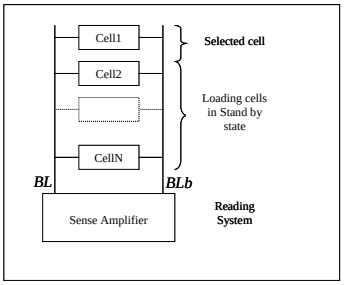
Device to System Modeling: flow

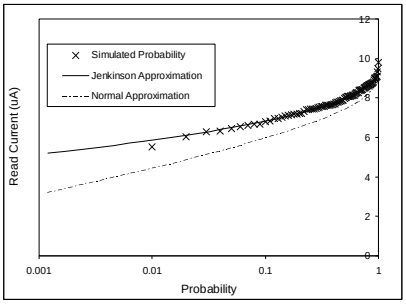


Statistical Analysis Flow from device to SoC level

Device to System Modeling: Results for Memories

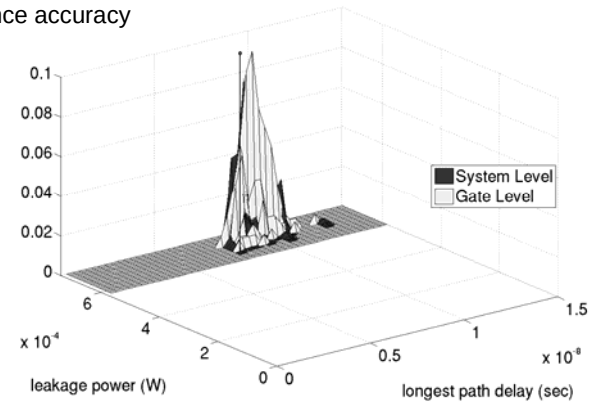
- Example: Creation of a memory column of a 32nm SRAM array from ARM's Memory statistical characterization
  - READ margining is accurate using Generalized Extreme Value Theory.





Device to System Modeling: Results at SoC level

- Test outcome, using a processor pipeline
  - System Level: combined individual statistics of all 5 pipeline stages
  - Gate Level: reference accuracy
- Results show:
  - Correlations are preserved
  - Good accuracy



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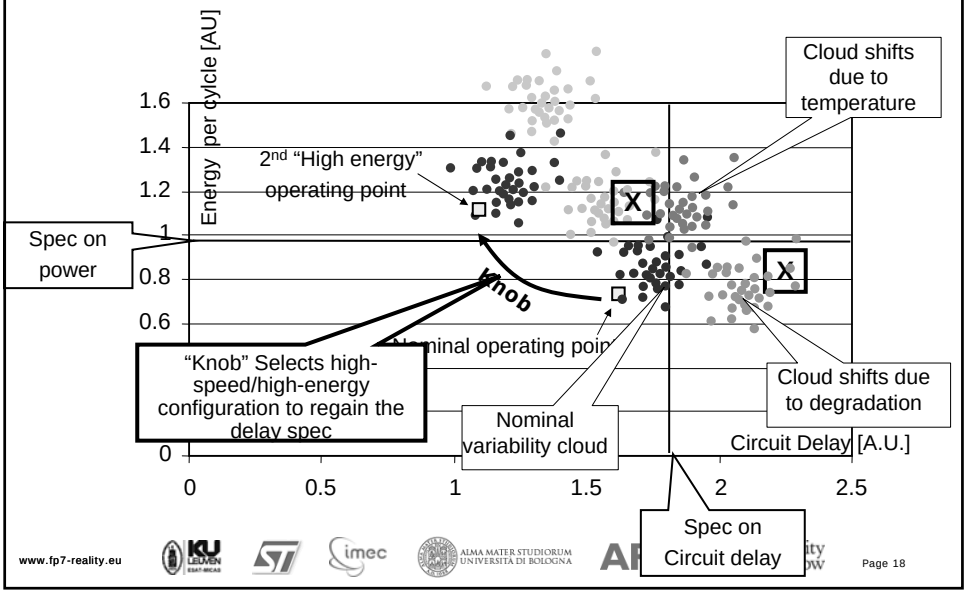
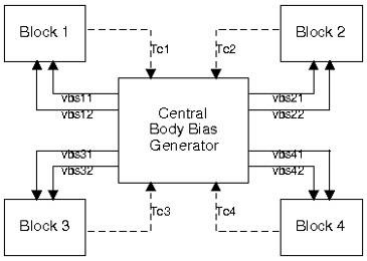
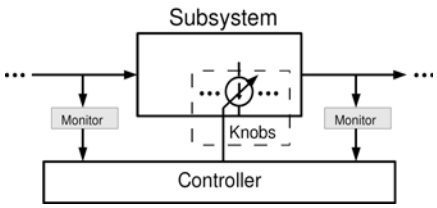
Circuit Counter-Measures: The concept



Circuit Counter-Measures: Examples

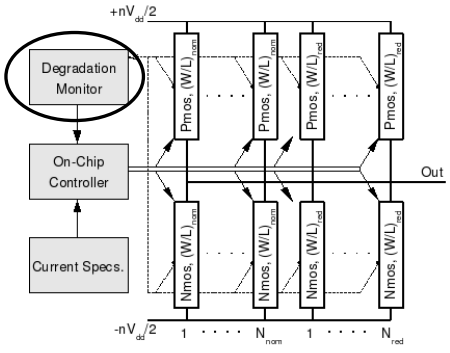
- Reliable+Variation tolerant dpath
  - Controller examines signature and decides (based on policy) how to set V_{dd}, V_B to layout rows, with constraints on power/speed
- Reliable+Variation mixed signal circuit
  - Controller monitors current and additional output drive sections are enable if required to keep ~constant drive





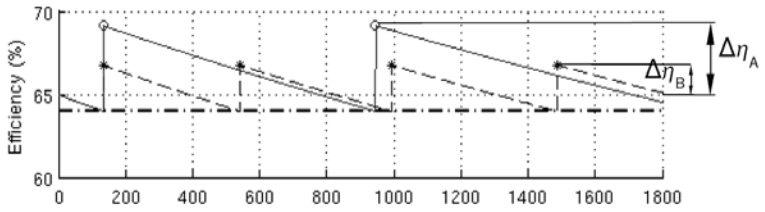
Degradation-Tolerant Mixed Signal Design

- Example circuit: high-voltage output driver (validation of simulation methodology)
  - Spec: power efficiency
  - Low R_{on} needed to preserve efficiency
  - Reliability simulation needed
  - Trade-offs at system-level
  - Circuit solutions using reconfigurable & self-healing techniques
    - ongoing



Degradation-Tolerant Mixed Signal Design: Results

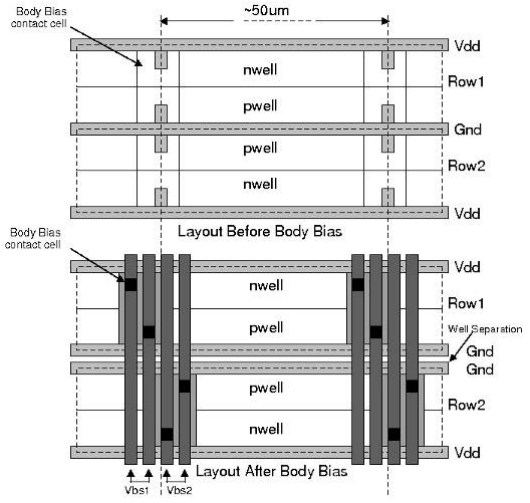
- Example circuit: high-voltage output driver
  - Trade-offs at system-level possible:
    - Reconfigurability / Healability level vs area/power overhead



[KUL- DRVW 2008]

Variability Tolerant Data-Path Design

- Novel physical layout design
  - Support very fine grained tuning
  - Low routing and area overhead
- Only 6% increase in utilization on each row



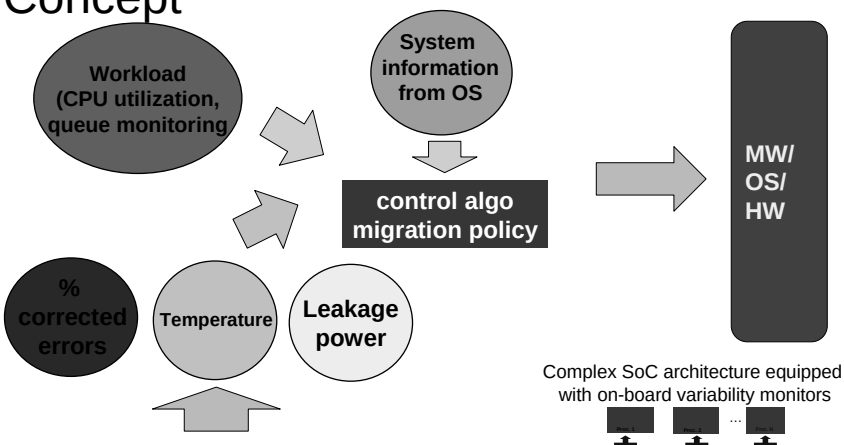
Variability Tolerant Data-Path Design: Results

	Benchmark	#gates	Energy savings (Optimal)	Energy savings (Heuristic)
ISCA 85 and ISCA89	C1355	439	11.76	11.76
	C3540	842	23.08	11.54
	C5315	1308	21.43	16.67
	C7552	1666	19.05	17.46
	Adder_128bits	2026	26.57	23.08
	C6288	2740	4.6	3.45
ST SoC	industrial	23898	-	15.67

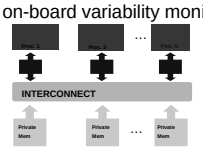
45nm ST technology library

Energy savings are w.r.t. single Body Bias technique

System-level Counter-Measures: The Concept



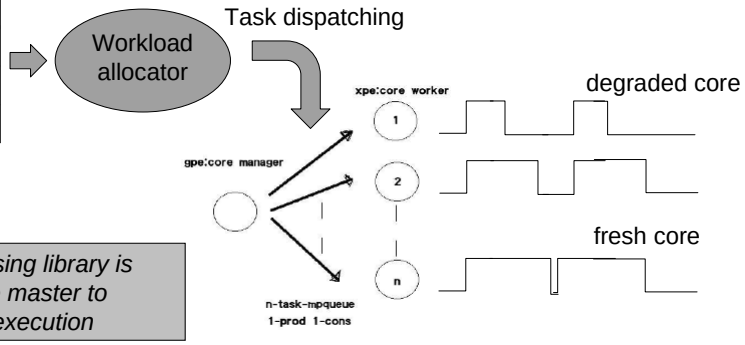
Complex SoC architecture equipped with on-board variability monitors



System-level Counter-Measures: Reliability Aware Workload Support

Trivial example: allocate less workload to "BAD" cores

Core #	Monitor
1	0.5
2	0.3
N	0.7



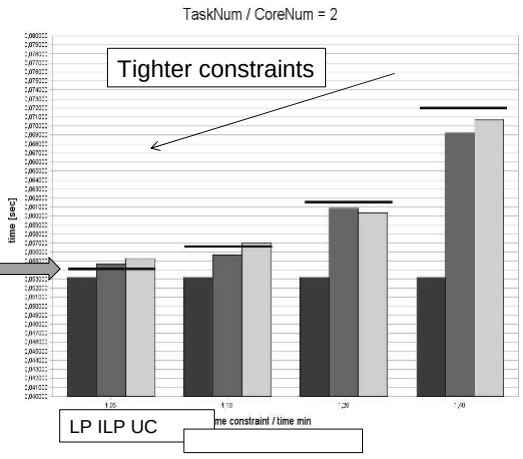
Message passing library is used to by the master to control slave execution

Reliability Aware Workload Support: Results

Control Algorithms for Variability Management:

- Deadline missed for tighter constraints
- Linear Programming (LP) always better (cycle granularity)
- Heuristic Solution (ILP, task granularity) better than Uncompensated Case (UC)

Timing constraint



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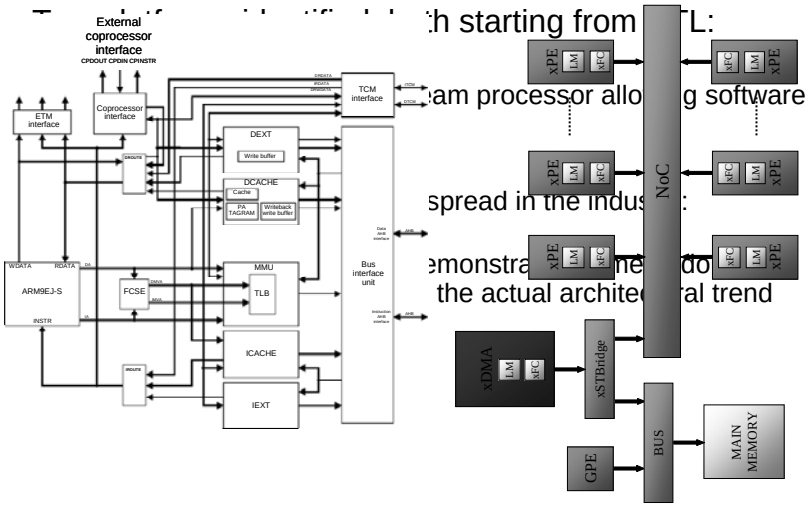
Integration and Demonstration



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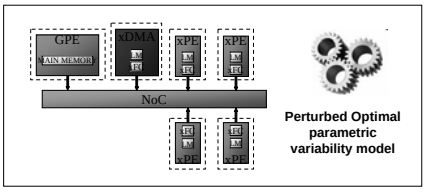
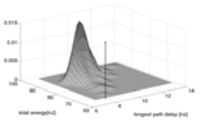
Assessment and Benchmarking

- Requirements on:
  - Application
  - Programming model
  - System specs
- Integration of simulation platform and models



REALITY system simulation platform (wp5)

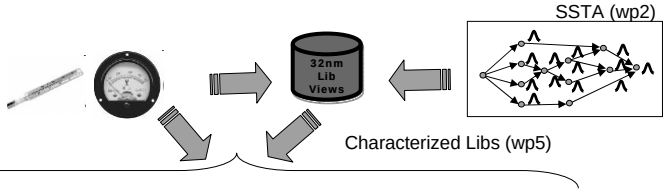
- Validation and benchmarking <u>against uncompensated situation</u>



System level analysis: Energy vs. Freq, Yield Functional Yield based on application requirements, comparative analysis with uncompensated case

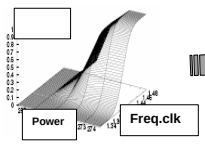
Validation strategy and scenarios: device to RTL

Wp6: Vdd/T Corners
(max,nom,min):
T: 70C,25C,-30C
Vdd: 1.2V,1.0V,0.9V

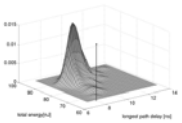


Characterized Libs (wp5)

ARM9 core & memories



IMEC VAM flow

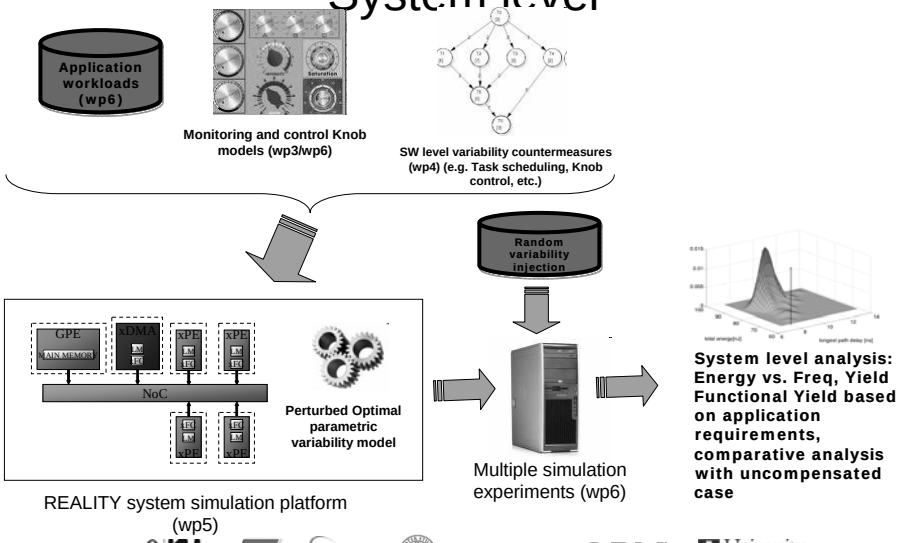


ARM9 Energy vs. Freq, Yield, etc.

Circuit level countermeasures (e.g. Memory, data-paths)

Analytical model parameters to system level validation

Validation strategy and scenarios: System level



Conclusions

- Under technology challenges:
  - Increased variability and static fault rates
  - Increased time-dependent variability and dynamic fault rates
- To address new design challenges:
  - To build reliable systems out of unreliable technology
  - Allowing technology scalable, energy efficient SoC systems
- Holistic Effort (from device to system) along two main axes:
  - Analysis and Modeling
  - Mitigating solutions at different abstraction levels: circuit, system
- Focus during first year on setting up flows and techniques
- Focus this year focus on implementation, demonstration and benchmarking

REALITY

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Thank you!

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