Variability beyond 45nm
Design Impact & Countermeasures

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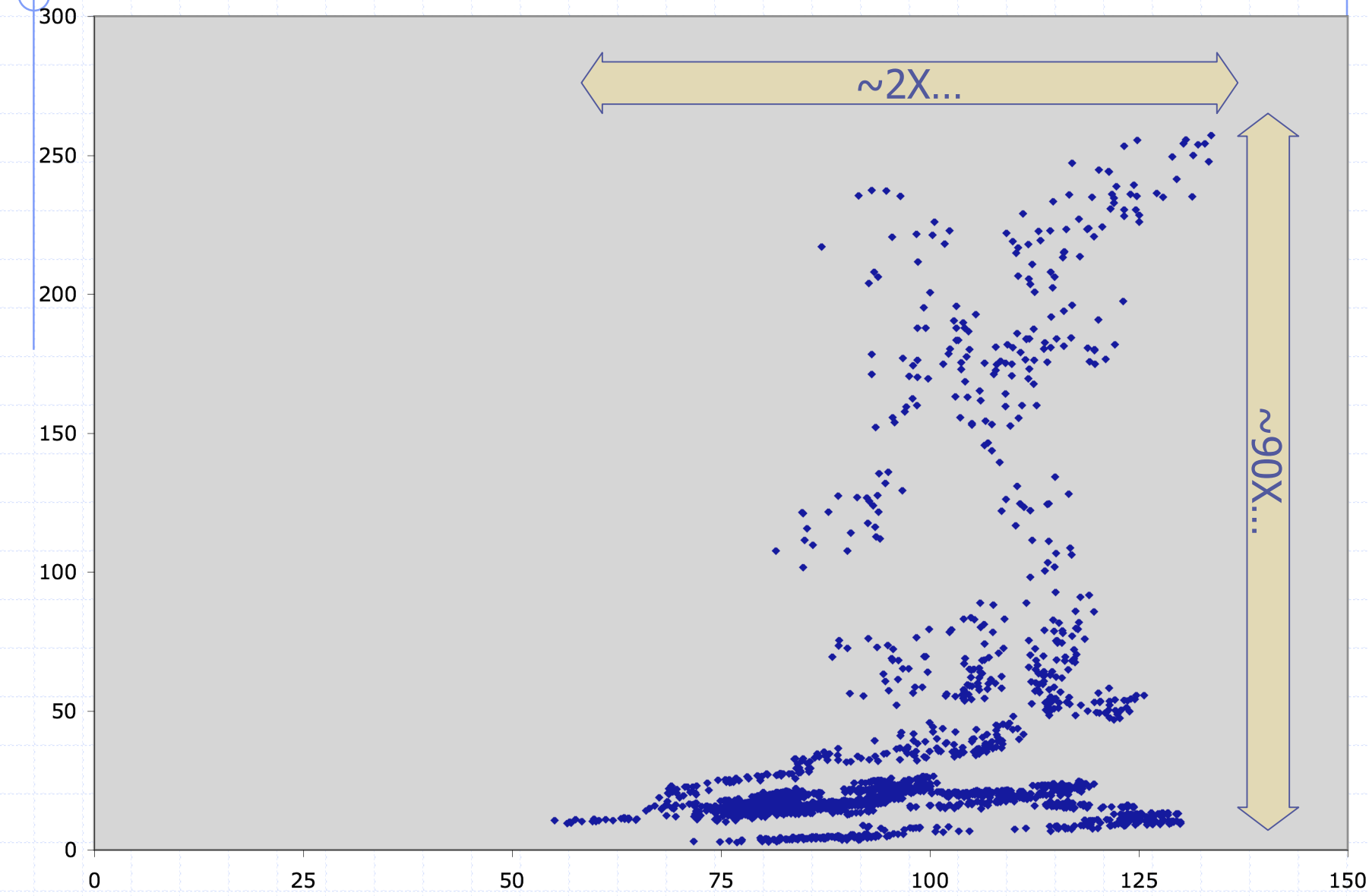
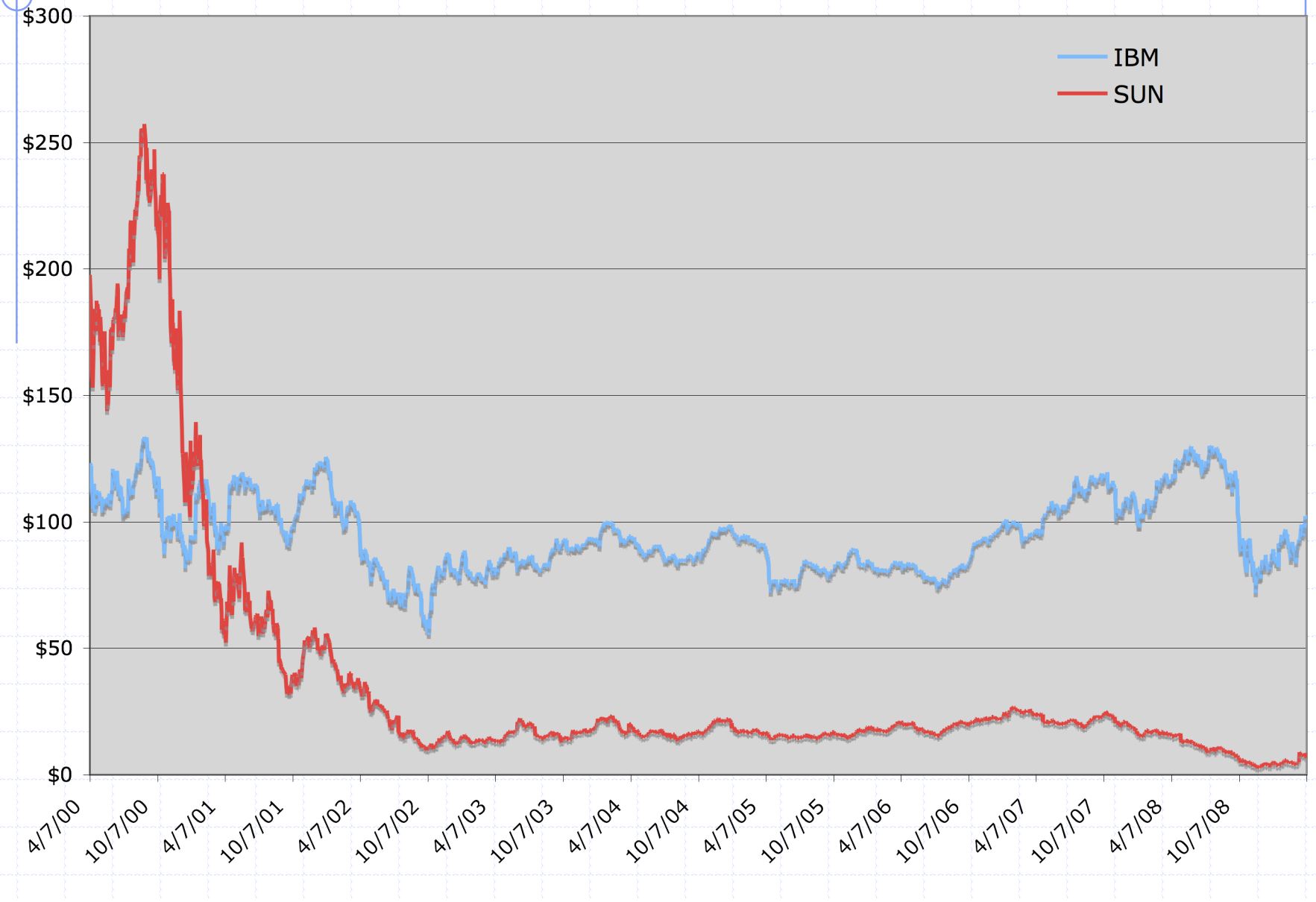
Variability: Things Changing!

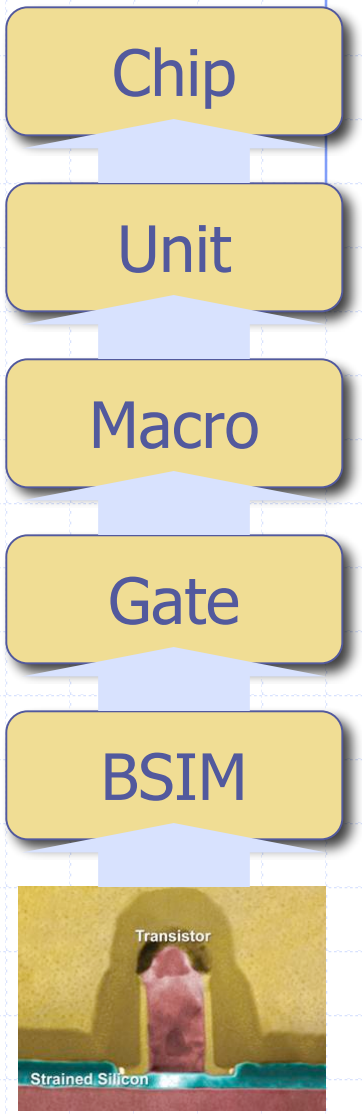


Things Really Really Change!



Realities

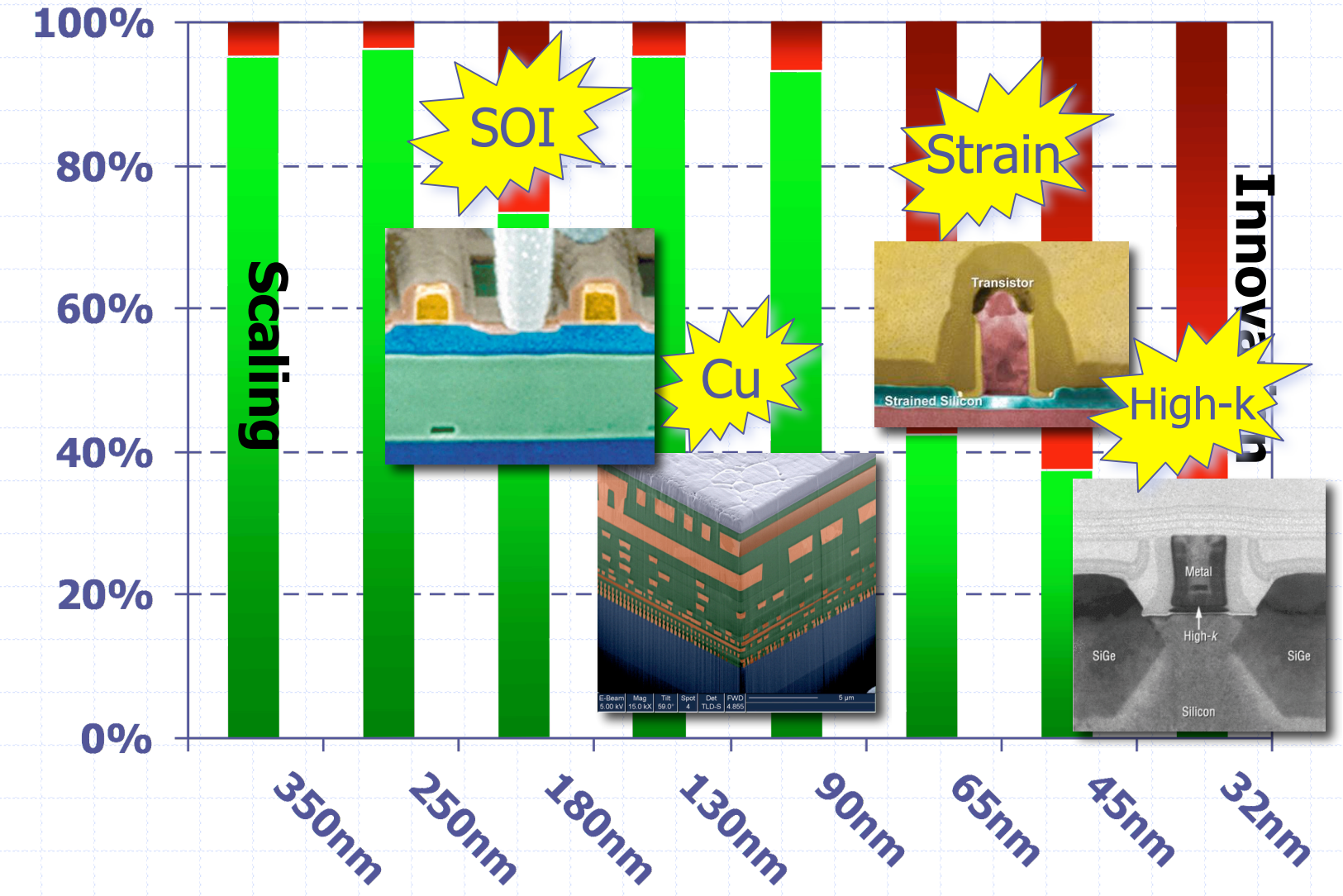
- The IC industry is built on a foundation of simulation and prediction.
  - We use models for frequency, power, yield.
- Models are derived from "characterization" which is done at multiple nested levels.
  - Manufacturing, Devices, Gates, Units, Chips.
- Technology complexity beyond the 90nm node is making this increasingly difficult!
- Variability, or lack of predictability, has emerged as major problem in current (45nm) and near term technologies.



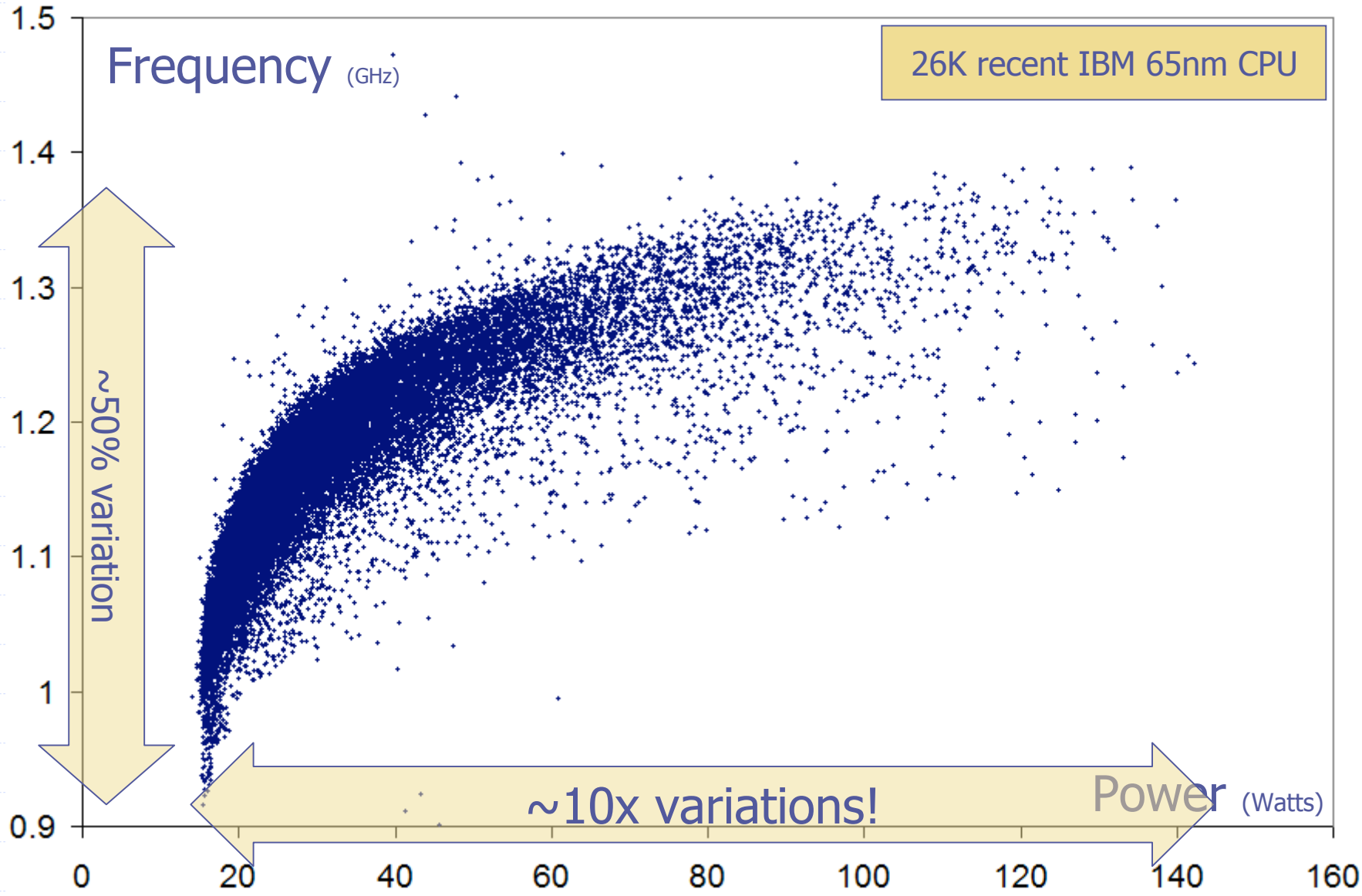
Why Added Complexity?

- Semiconductor manufacturing is getting harder as scaling fails to deliver performance.
  - Performance gain per technology generation is reducing.
- Gain coming from non-scaling innovations, Cu, SOI, Stress, Hi-κ, etc…
- Technology R&D has become so expensive that few companies can afford to do it alone.
  - Thus the consolidation we see in our industry.

Scaling vs. Innovation



Result: Massive Variability



Introduction to Variability

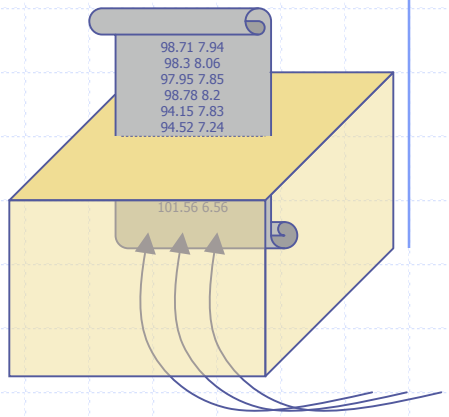
- Variability means lack of uniformity.
  - Individual devices on a chip are NOT identical.
  - Individual chips are NOT identical.
- Fluctuations imply unpredictability, which ultimately leads to un-profitability.
  - Sales team cannot reliable predict product!
- Important variability concepts:
  - Systematic vs. Random.
  - Time and space dependence.
  - Future trends.

Variability vs. Knowledge

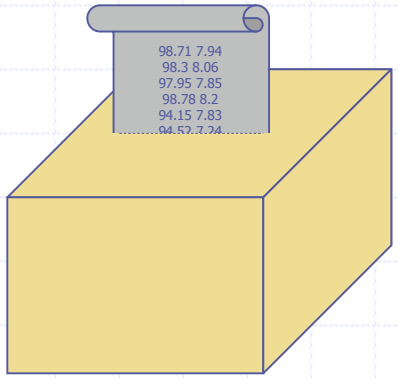
- Often, variability is simply "lack of knowledge".
- This lack of knowledge can come about due to different factors:
  - I do not know where on the wafer this die will be.
  - I do not know how this wafer or lot will get processed.
  - I do not know what type of wiring will pass over this cell.
  - I do not know the exact load I am driving.
  - I do not know the exact value of V_{DD}.
  - I do not know how long this chip will need to operate.
  - …
- Often (always?), knowledge requires effort!

Random vs. Systematic?

- Systematic variability occurs when variation is caused by a known phenomena.
  - Wafer edge behaves differently from center!



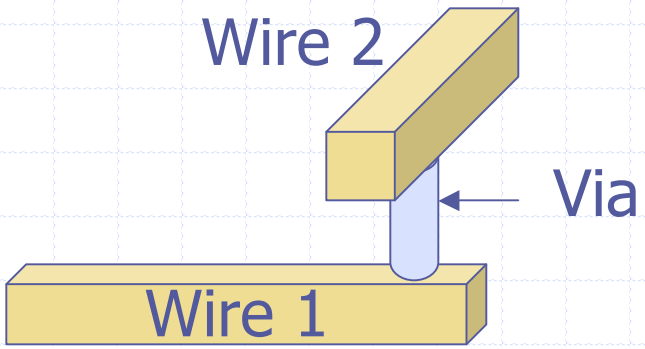
- Random variability occurs when the law of large numbers fails, i.e. for atomistic phenomena driven by scaling.
  - Random dopant fluctuations, line edge roughness.
  - Exacerbated for smaller devices.

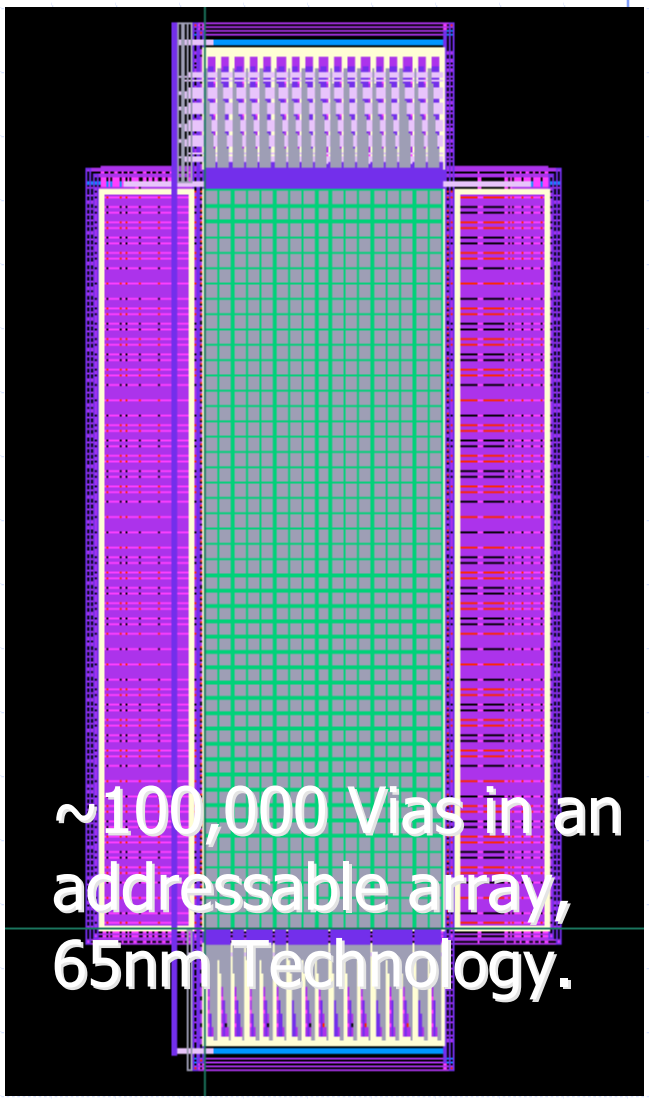


- For die-to-die variability, the random vs. systematic breakdown is immaterial since it does not change how the phenomena is dealt with.

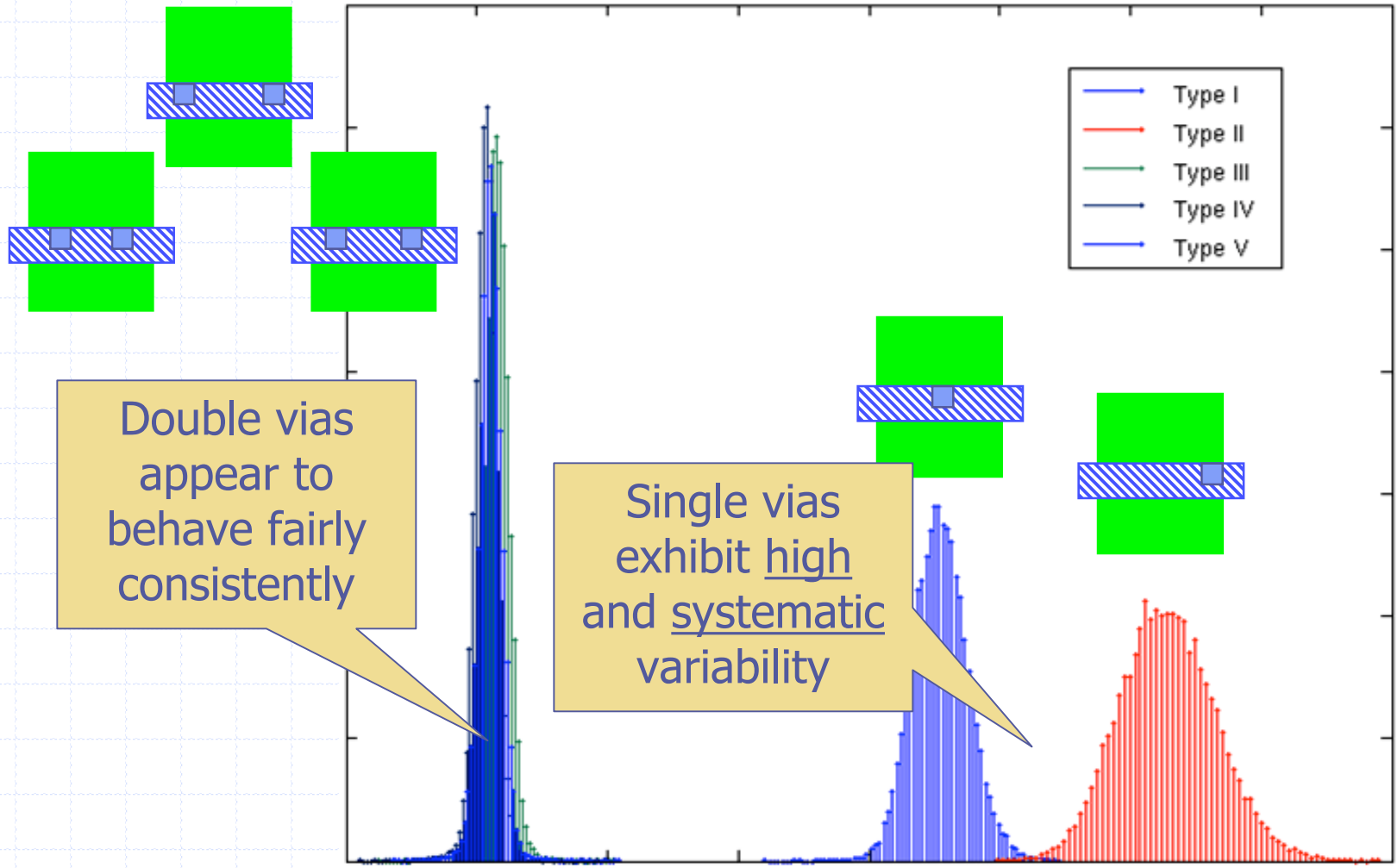
Systematic Variability: Characterization

- Vias are the connections between different metal levels, and between metal and Si.
- Via resistance is a very important technology characteristic.
- We created a special structure to measure resistance of individual vias for various configurations.

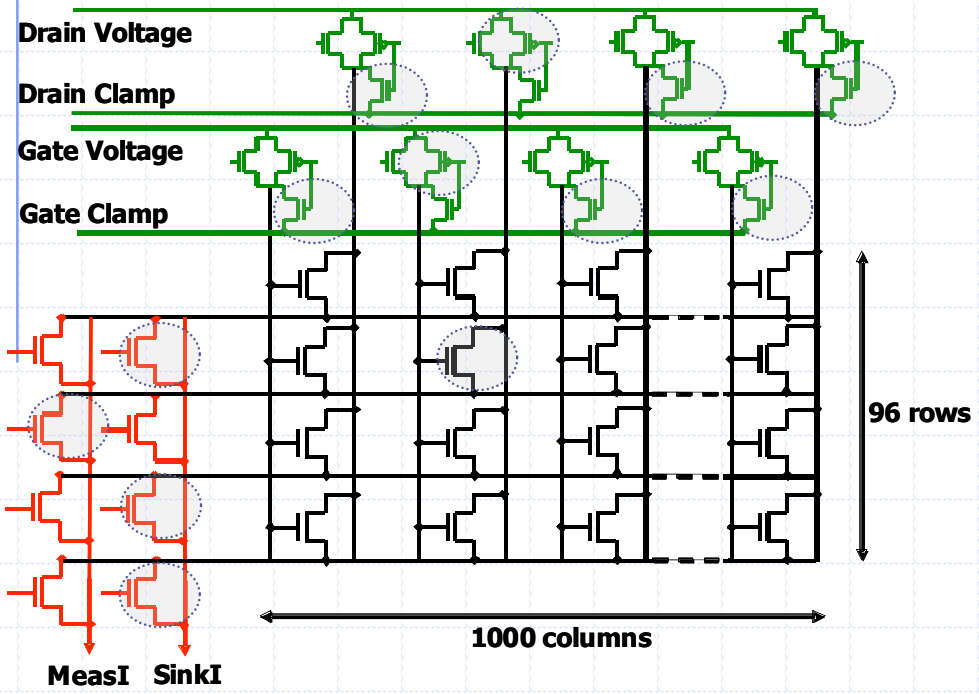


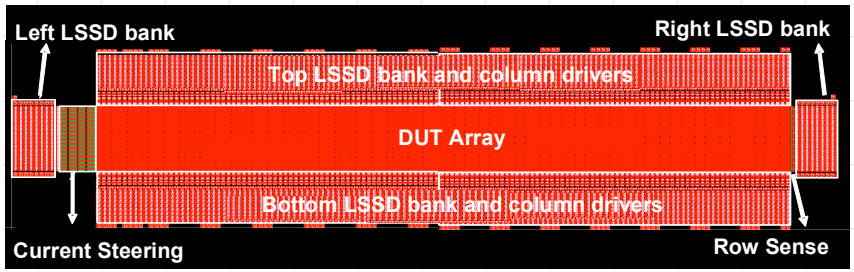


Systematic Variability: Observation



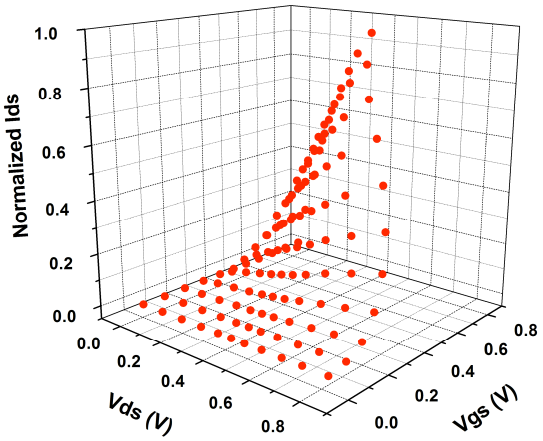
Random Variability: Characterization

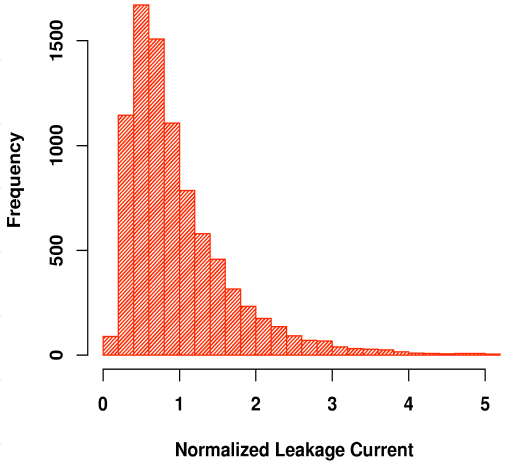


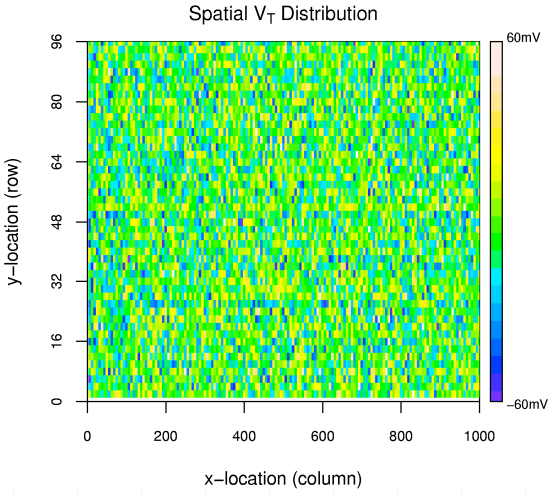


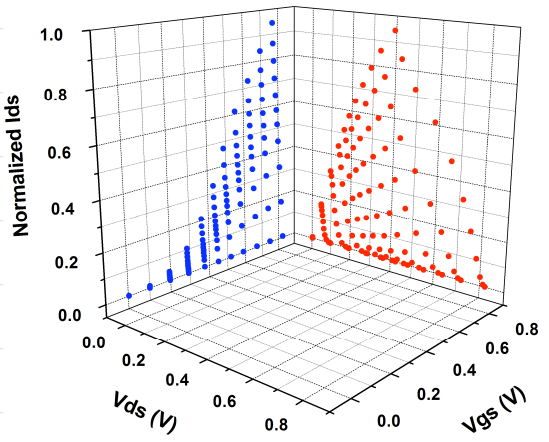
- Test structure to explore the limits of device variability.
- Small sized devices arranged in an addressable array.
- Current is "steered" in array to allow the measurement of individual devices.
- 96 rows, 1000 columns – 96,000 total devices.

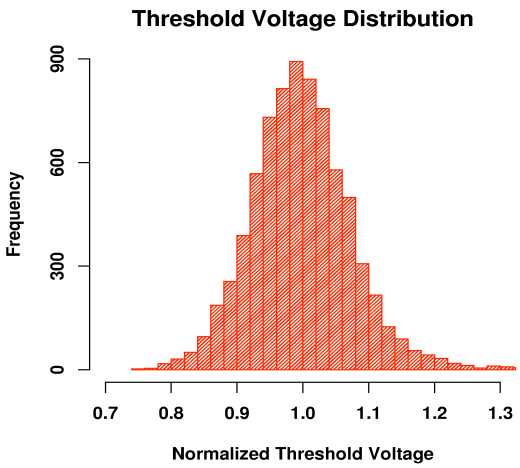
Random Variability: Observation

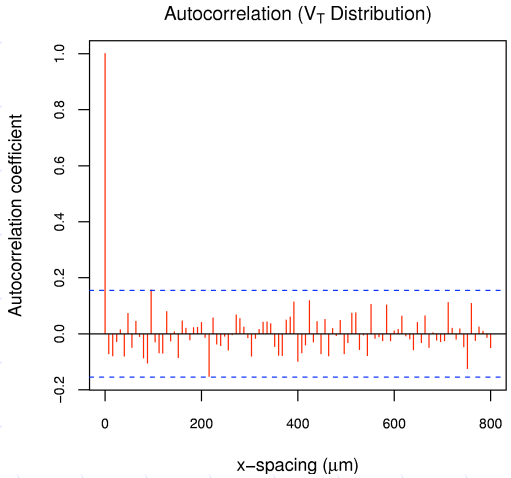












Sample I-V curves

Parameter Distributions

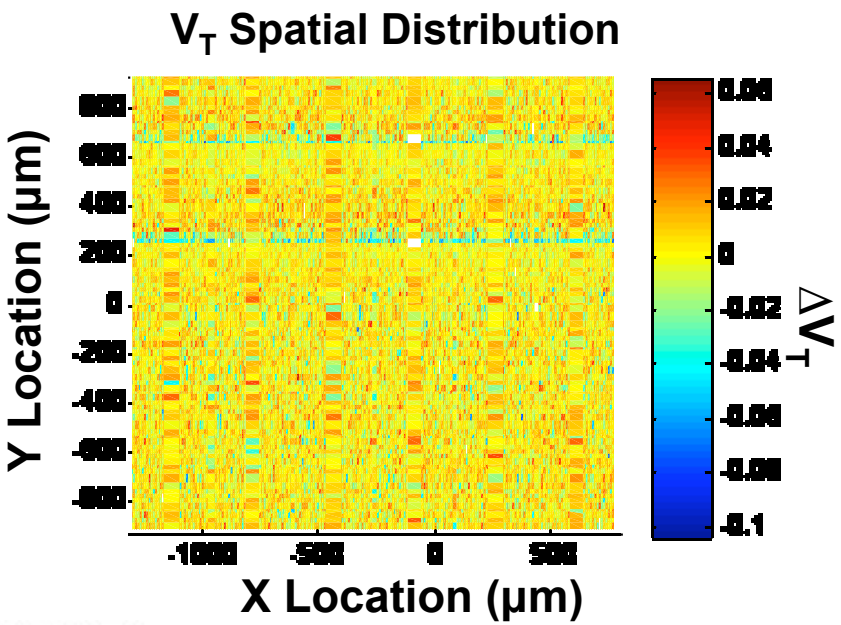
Spatial Correlation

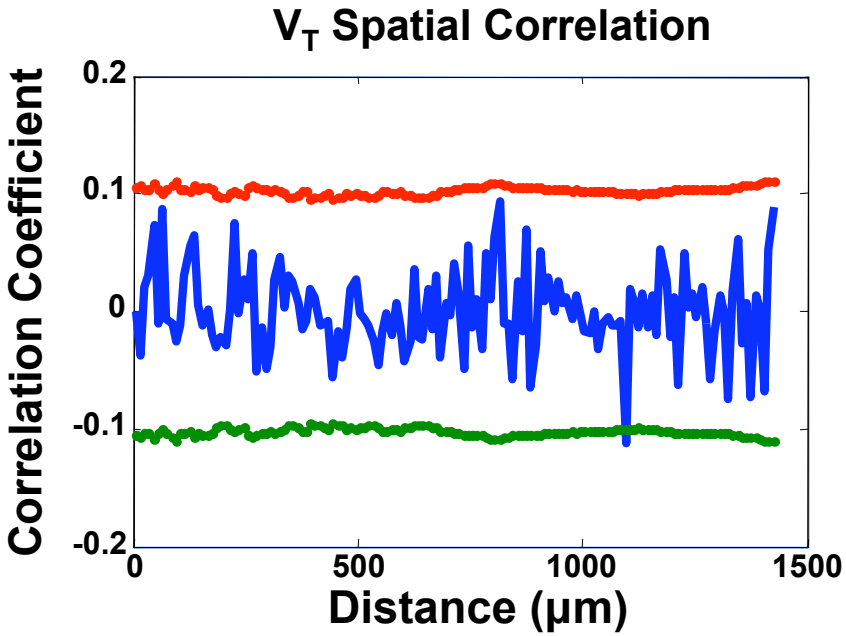
K. Agarwal, et. al. DAC 2007

V_T: Within-Die Spatial Variation

- V_T variation follows Pelgrom Model
  - Proportional to square root of device area
  - Variance not distance dependent
- No statistically significant correlation
  - Correlation coefficients centered around 0
  - No dependence on distance

$$\sigma(V_{T_o}) = \frac{A^2_{V_{To}}}{WL} + S^2_{V_{T_o}} D^2$$





Courtesy Duane Boning (ICCAD '08) *cf.*

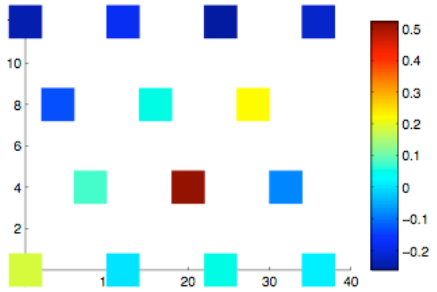
Systematic vs. Random

- Systematic: known quantitative relationship to a source (readily modeled and simulated).
  - Designer has option to *null* out impact.
  - Example: power grid noise.
- Random: sources unknown, or model too difficult/costly to generate or simulate.
  - Treated using worst-case analysis, increasing design margin.
  - Example: ΔL within die variation.

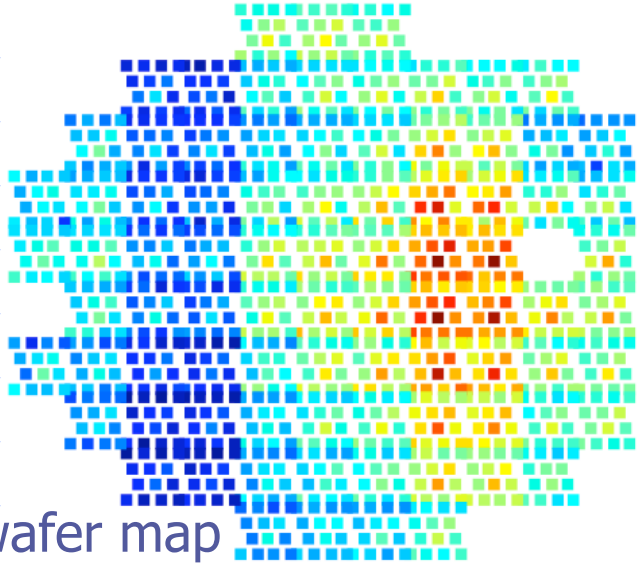
- Lack of modeling resources often transforms systematic phenomena to a random one.
  - Therefore leading to excessive design margins!

Spatial Variability Characterization

- Requires a "deep" sample of performance over all important levels of the chip manufacturing hierarchy.
- In IBM, performance-sensitive ring oscillators are embedded in each chip.
  - In this example, chip had 14 process rings.
  - Each ring is independently testable.
- Collected 348 wafers from 23 lots.
  - Each wafer contained 117 die.
  - Around 6% of the measurements are missing.
- Work done in partnership with Prof. Sherief Reda, Brown Univ.



Rings within die

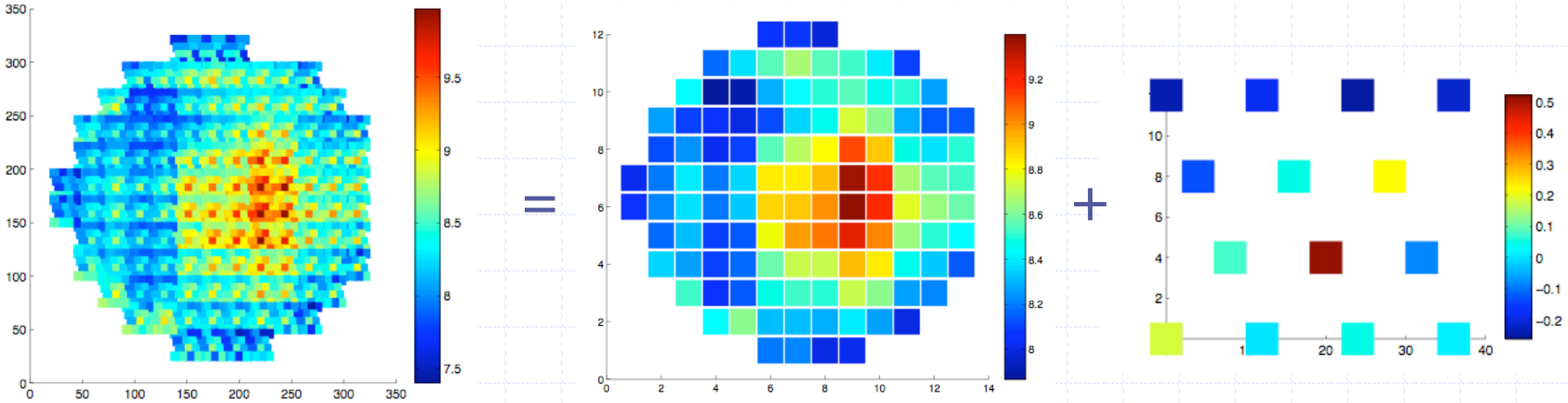


Typical wafer map

Courtesy S. Reda (DATE '09)

Systematic Spatial Variations

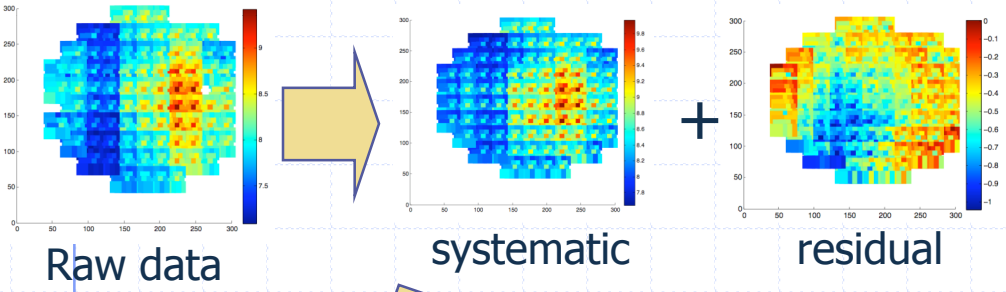
- Extract out "common" pattern across dies and wafers.
- Take the mean of the data, and separate out the wafer and die components.
  - Upcoming paper on algorithms used, accepted to DATE 2009.

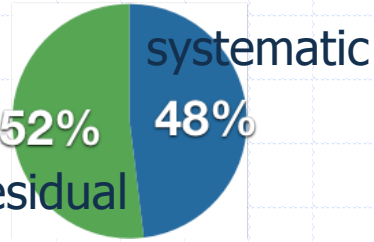


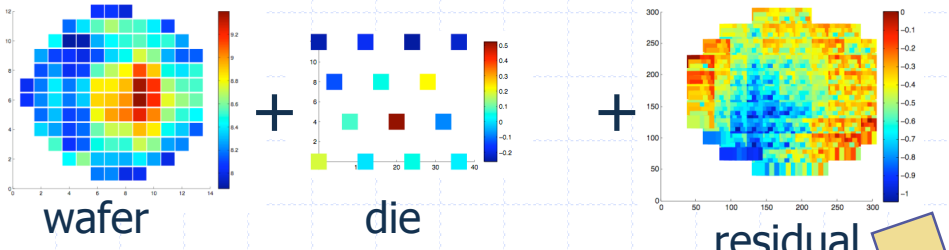
average wafer | systematic within-wafer | systematic within-die

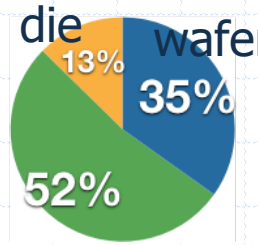
Courtesy S. Reda (DATE '09)

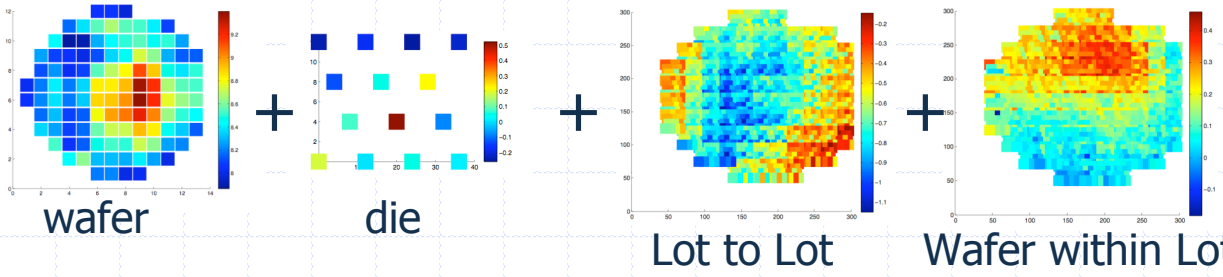
Overall Variability Breakdown

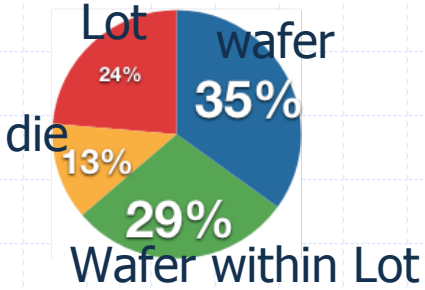












Courtesy S. Reda (DATE '09)

Spatial Systematic vs. Random

- There are a number of systematic phenomena at various length scales:
  - Wafer-level phenomena ~3000μ.
  - Chemical Mechanical Polishing ~300μ.
  - Rapid Thermal Annealing ~30μ.
  - Resist Etch Loading ~3μ.
  - Lithography ~0.3μ.
- From a design-level modeling point of view, these systematic phenomena have been a problem.

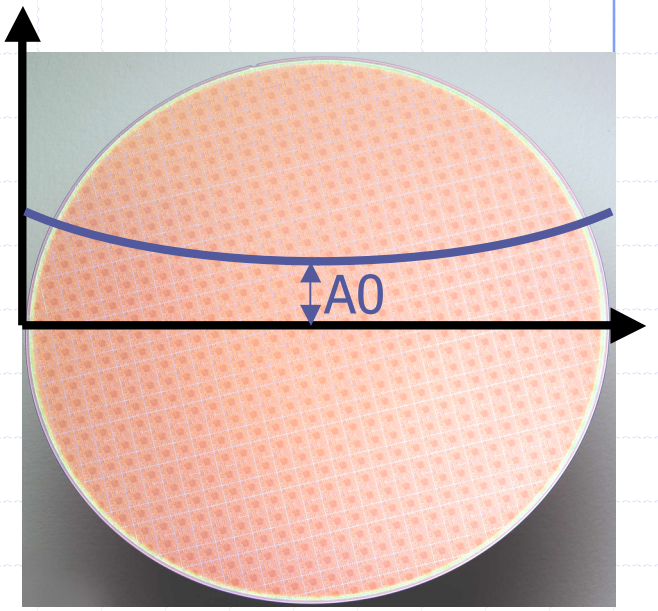
Spatial Systematic Variability

Two types:

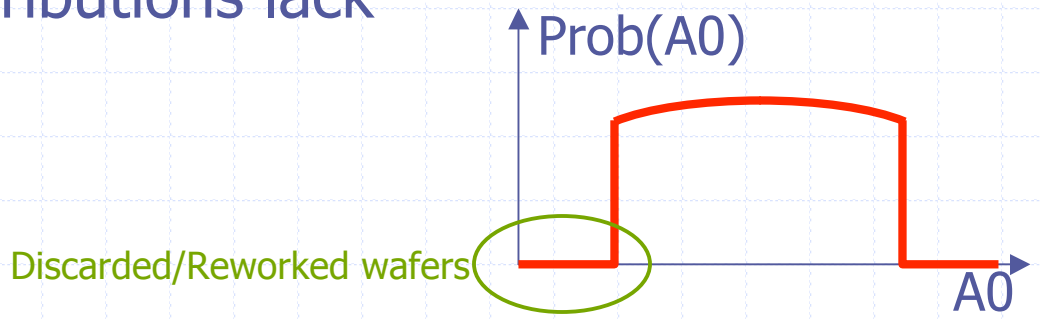
- Position dependent
  - These phenomena are usually due to specific wafer or reticle level processing steps.
  - Example: "salad bowl" shape for T_{OX} across wafer.
- Local (layout) dependent
  - These phenomena are dependent on neighborhood issues like layout density.
  - Example: wire thickness variation due to CMP.

Modeling Spatial Systematics

- For pure position dependent variability, we must rely on characterization.



- It is important to recall that statistical process control is in effect, which means that "out of spec" wafers are typically missing.
  - Implication: distributions lack the "tails".



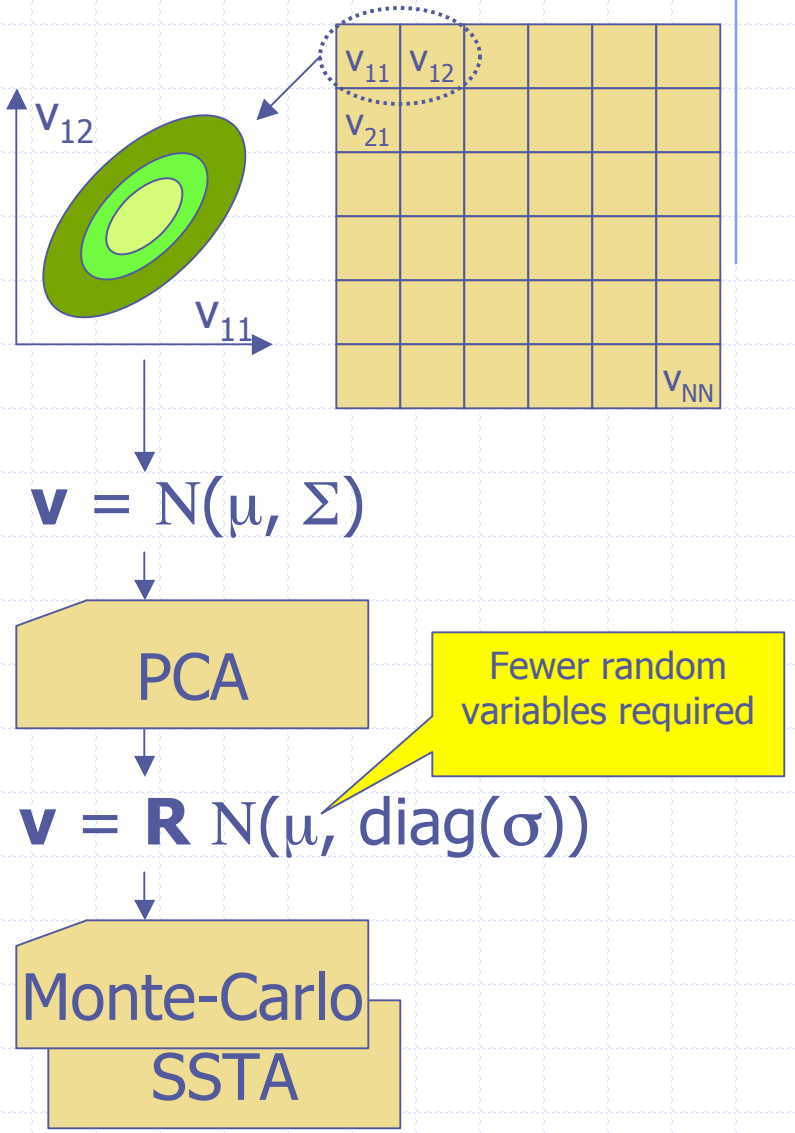
Modeling Design Systematics

- Impact of design dependent variability on a design depends on… the design!!!
- When a design is complete, models (e.g. CMP) can be applied to determine impact.

- Before a design is finalized, however, it is only possible to make estimates.
  - Current research is focused on a purely stochastic description of the variability.
  - Key assumption: spatial correlation.
    - Things close by are correlated…

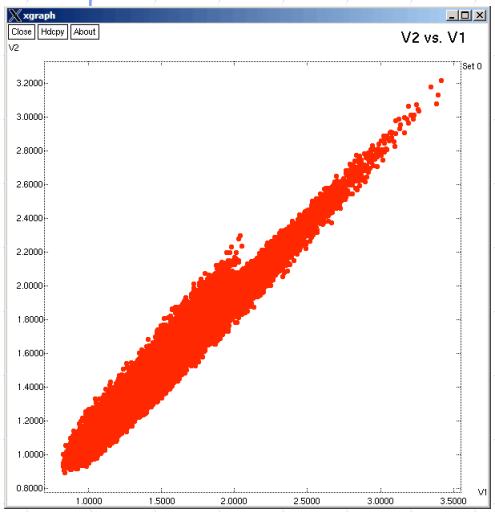
Stochastic Spatial Variability

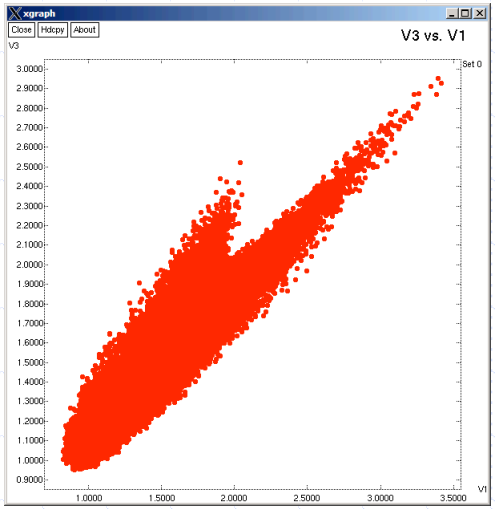
- Assumes correlated random variables, with correlation dependent on distance.
- The overall chip is divided into a number of spatial bins.
  - Each bin has a unique value.
  - The values are correlated.
- To make analysis easier, the design space is reduced using PCA (or similar techniques).
- Such a stochastic model allows analysis via MC or SSTA.

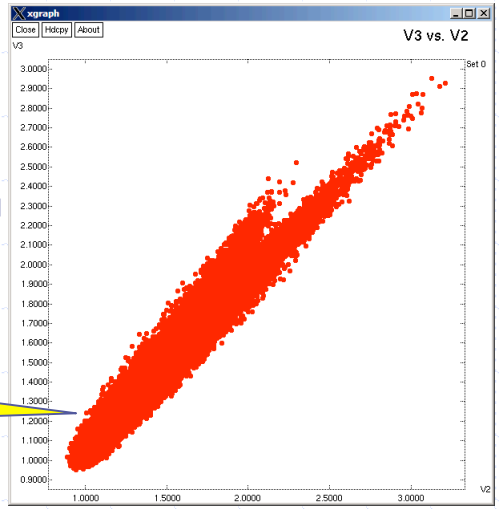


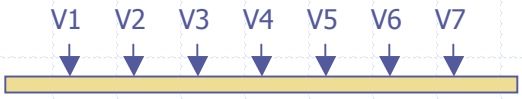
Simple Example

- "1D" chip with 7 measurement points...





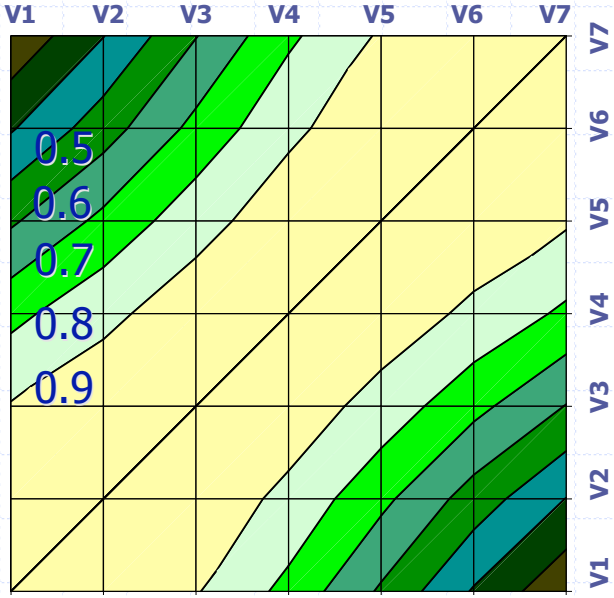




20K chips

Correlation Matrix:

V1	V2	V3	V4	V5	V6	V7
1.00000	0.97678	0.90700	0.77102	0.58551	0.39022	0.21902
0.97678	1.00000	0.96645	0.87440	0.72531	0.55462	0.39719
0.90700	0.96645	1.00000	0.95866	0.86156	0.72917	0.59604
0.77102	0.87440	0.95866	1.00000	0.95943	0.87848	0.78106
0.58551	0.72531	0.86156	0.95943	1.00000	0.96783	0.91242
0.39022	0.55462	0.72917	0.87848	0.96783	1.00000	0.97830
0.21902	0.39719	0.59604	0.78106	0.91242	0.97830	1.00000



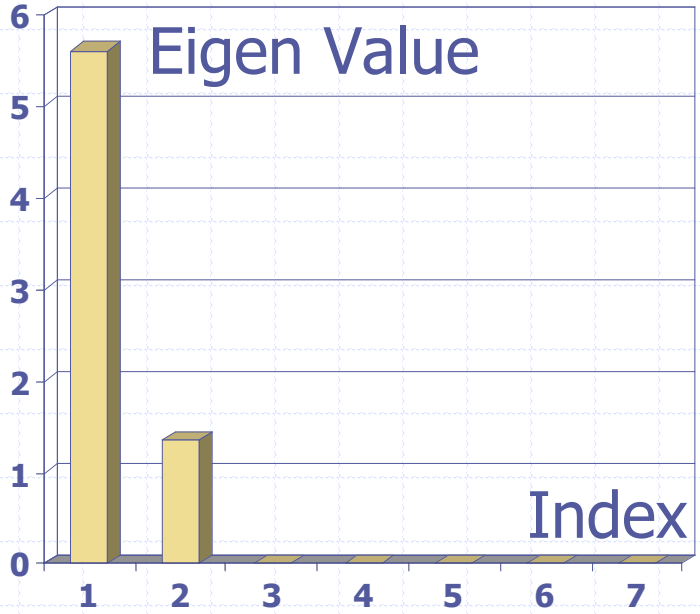
PCA on Simple Example

- PCA analysis reveals that only 2 factors are needed to model the statistics!

- Two independent random variables are sufficient to model the correlated spatial variation observed.

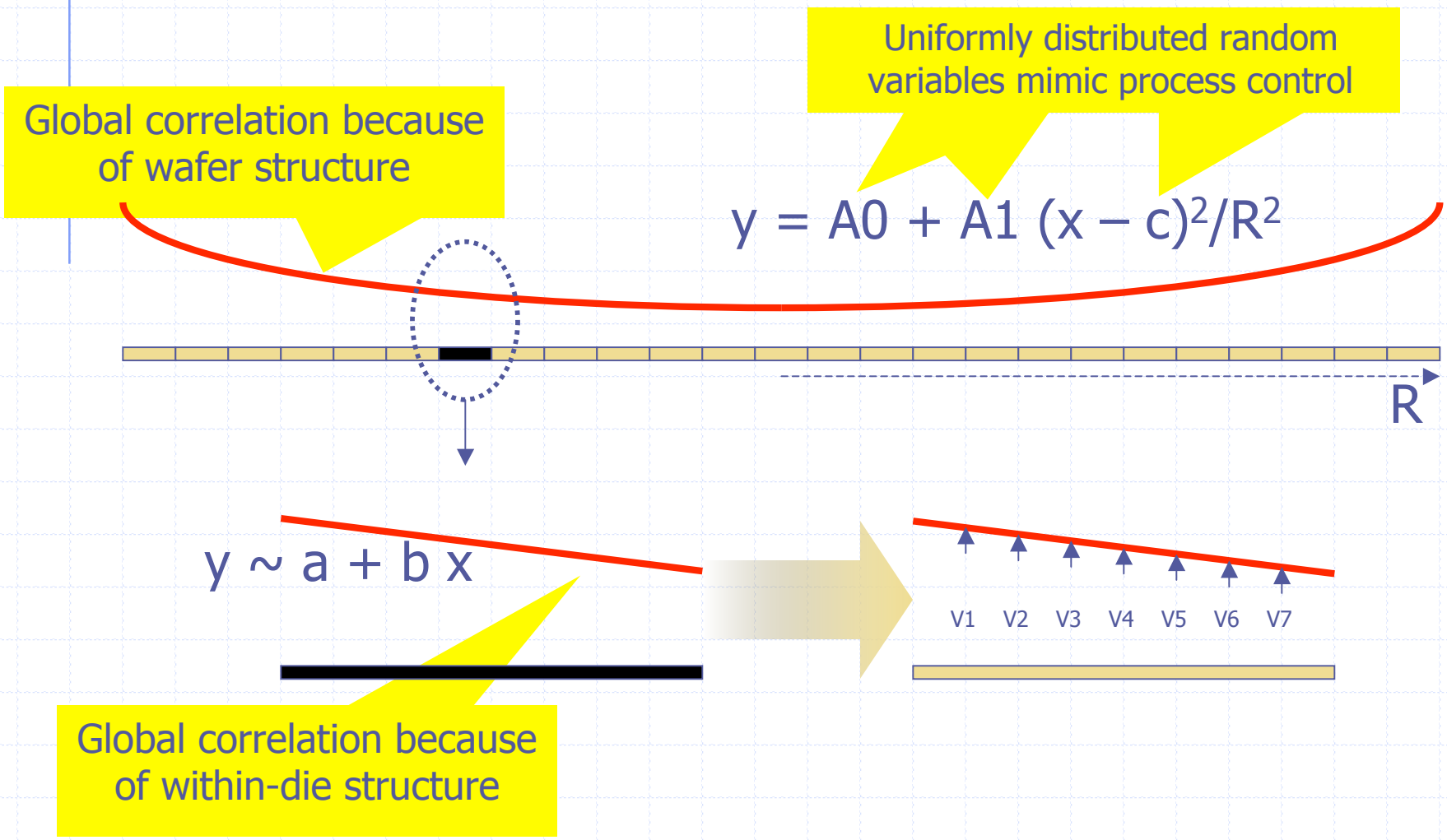
-0.32742	0.54032
-0.37114	0.40538
-0.40672	0.22004
-0.42067	-0.00217
-0.40651	-0.22179
-0.37186	-0.40271
-0.33036	-0.53285

$$\mathbf{v} \sim 1.6 + 0.4\,\mathbf{R}\,N(0, \mathrm{diag}(1))$$



Actual Source of Data…

- A "1D" wafer with systematic variations.



Comparison…

"True" Random Variables

Systematic Model

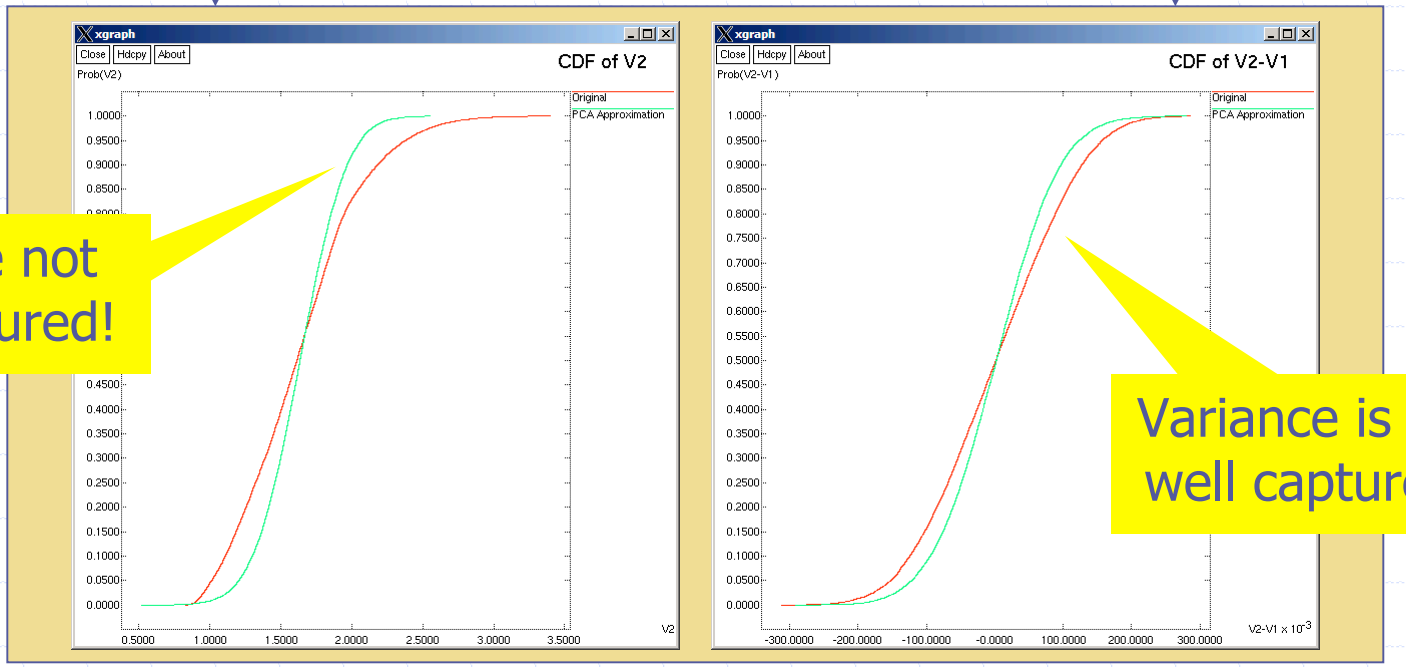
Variability Sample

PCA Analysis

"Discovered" Random Vars

Sampling

Variability Sample



Tails are not well captured!

Variance is not well captured!

Reasons, and Results

- A true stochastic model assumes variables have infinite tails.

But…

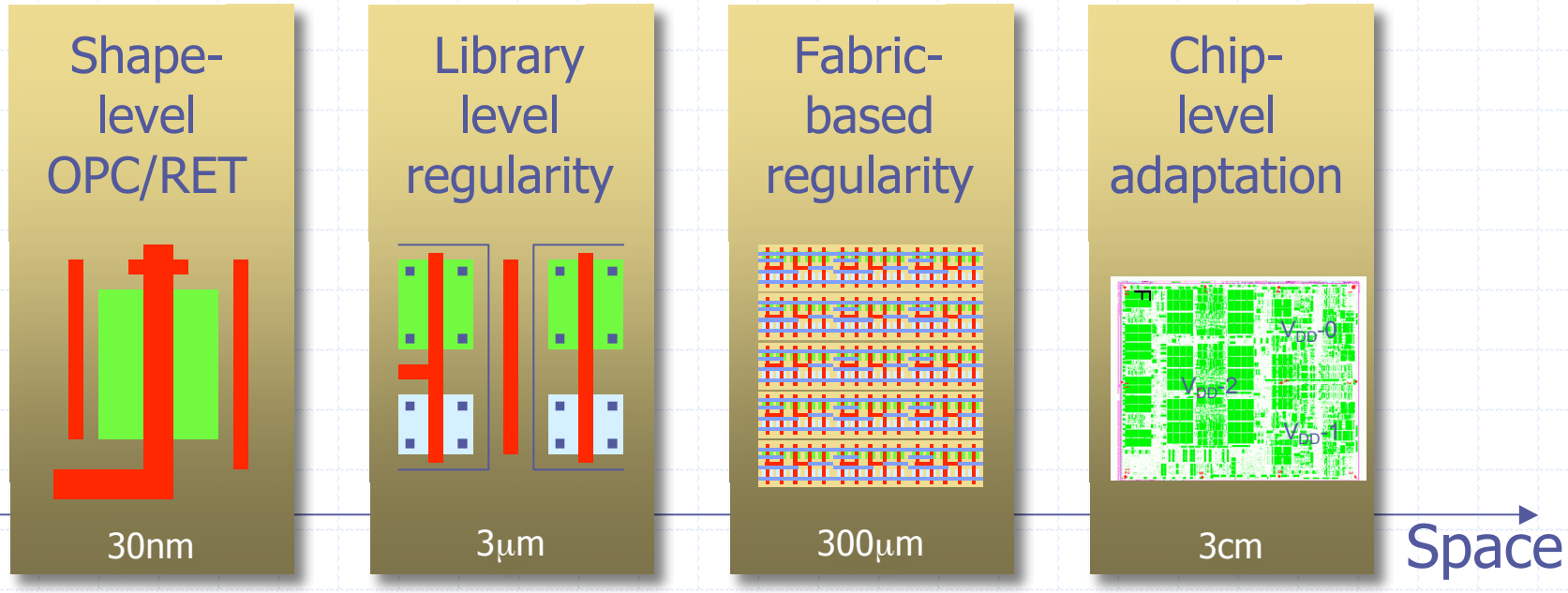
  - Position-related variables are bounded!
  - And… process control leads to truncated and bounded distributions.

Therefore…

- One must be careful in how systematic spatial variability is modeled. Naïve models will lead to inaccuracy. (More research is needed).
  - Adoption of SSTA is gated by accurate models.

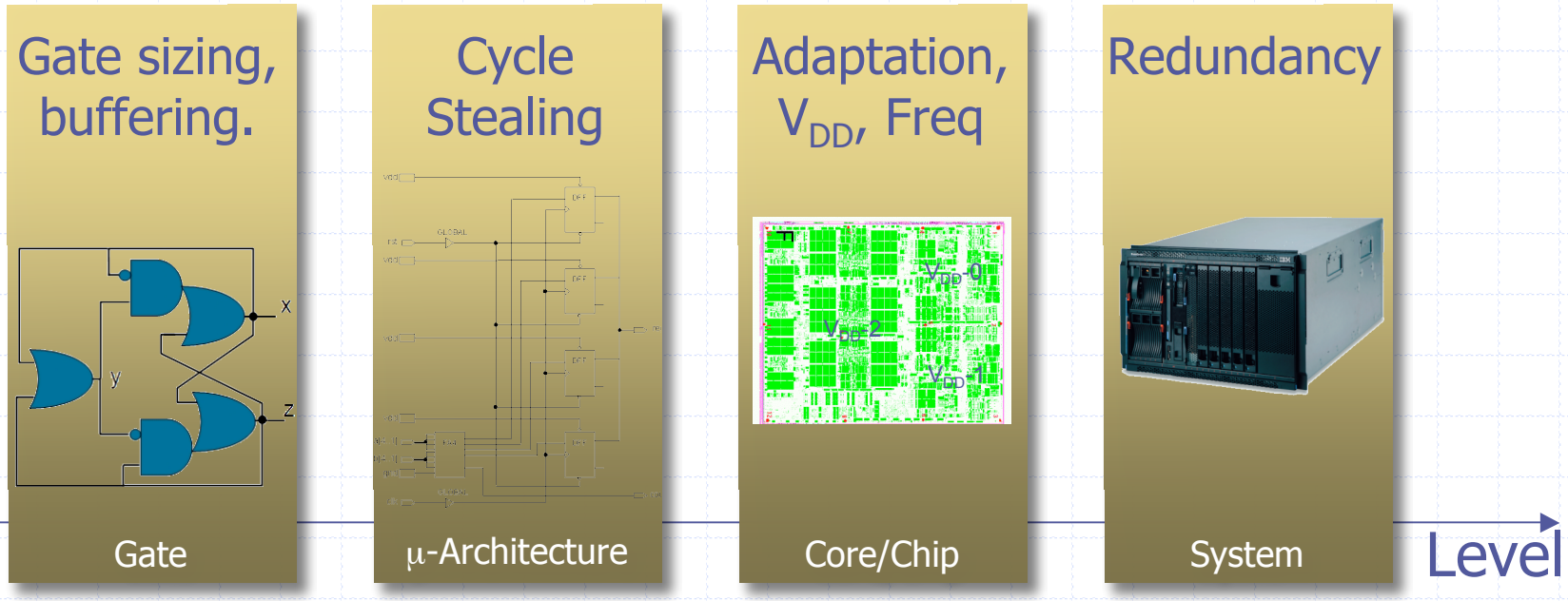
Response: Manufacturing

- Responses to manufacturing variability target different levels of granularity.
  - Message: no one response is sufficient to tackle the full impact, + higher leverage exists at the higher levels (e.g. adaptation)!



Response: Design

- Responses to variability as lack of knowledge.
  - Designers are smart, but are caught between increasing variability and decreasing performance!
  - Require knobs that change σ/μ, not just μ!



Lithography Trends (ITRS)

- ITRS document now has a DFM component.
  - Focuses on the relationship between technology specifications and circuit performance.
- One of the major sources of circuit variation is Critical Dimension (CD) control.
  - CD control is lithography's goal!
- ITRS makes predictions on future CD control.
  - Such predictions drive research in this area.
  - They should also drive "prevention" research!

CD Tolerance Components

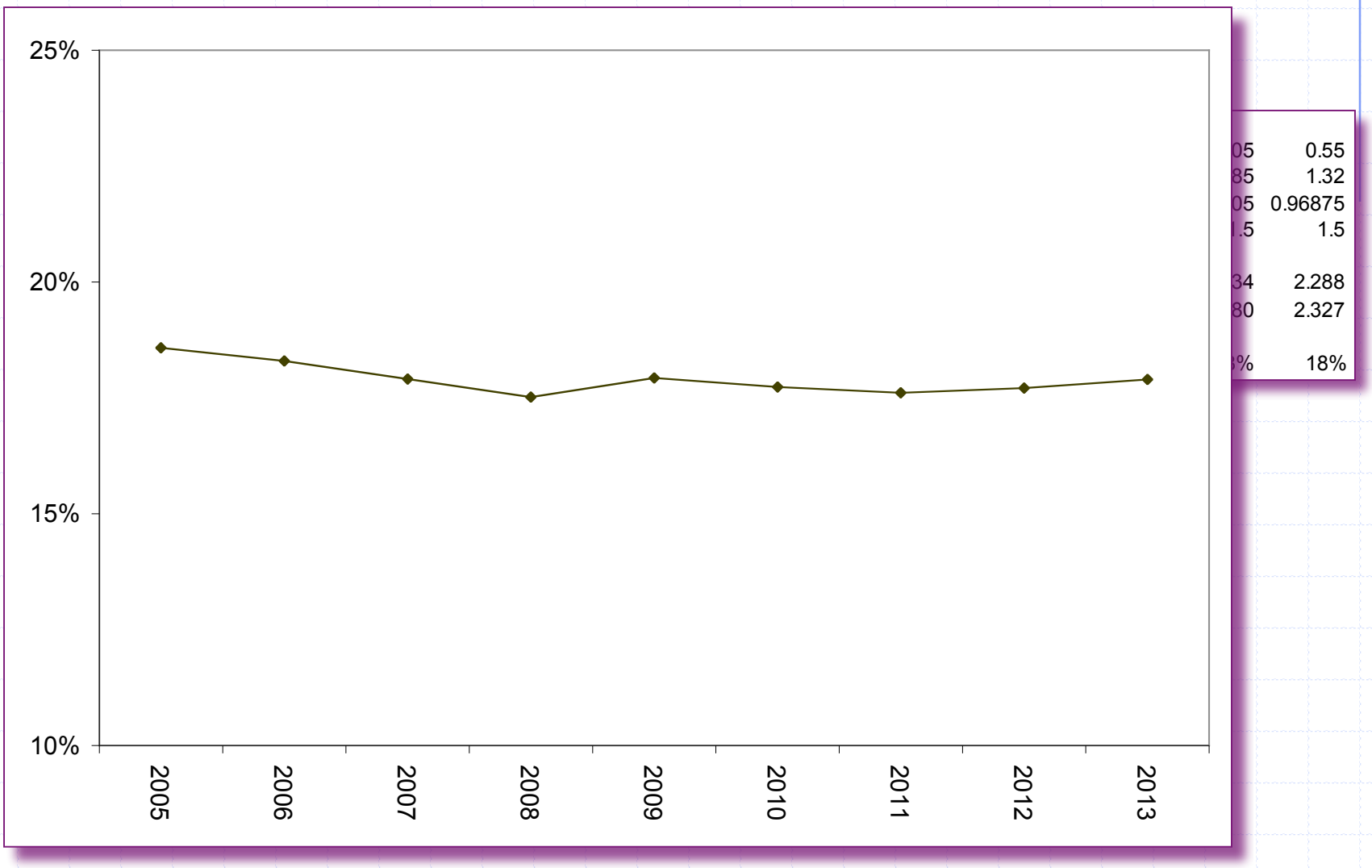
- Taken from 2005 Litho chapter:

	2005	2006	2007	2008	2009	2010	2011	2012	2013
Table 69a									
MPU physical gate length (nm)	32	28	25	23	20	18	16	14	13
Table 77a									
Low frequency line width roughness (3 sigma) (nm)	4.2	3.8	3.4	3	2.7	2.4	2.1	1.9	1.7
Table 78a									
Gate CD control (3 sigma) (nm)	3.3	2.9	2.6	2.3	2.1	1.9	1.7	1.5	1.3
Overlay (3 sigma) (nm)	15	13	11	10	9	8	7	6	6
Mask magnification	4	4	4	4	4	4	4	4	4
MEEF - isolated lines	1.4	1.4	1.6	1.8	2	2.2	2.2	2.2	2.2
CD uniformity - isolated lines (3 sigma) (nm)	3.8	3.4	2.6	2.1	1.7	1.3	1.2	1.1	1
MEEF - dense lines	2	2	2.2	2.2	2.2	2.2	2.2	2.2	2.2
CD uniformity - dense lines (3 sigma) (nm)	7.1	6	4.8	4.3	3.8	3.4	3	2.7	2.4
Linearity (nm)	13	11	10	9	8	7.2	6.4	5.6	5.1
CD mean to target (nm)	6.4	5.6	5.2	4.6	4	3.6	3.2	2.8	2.6

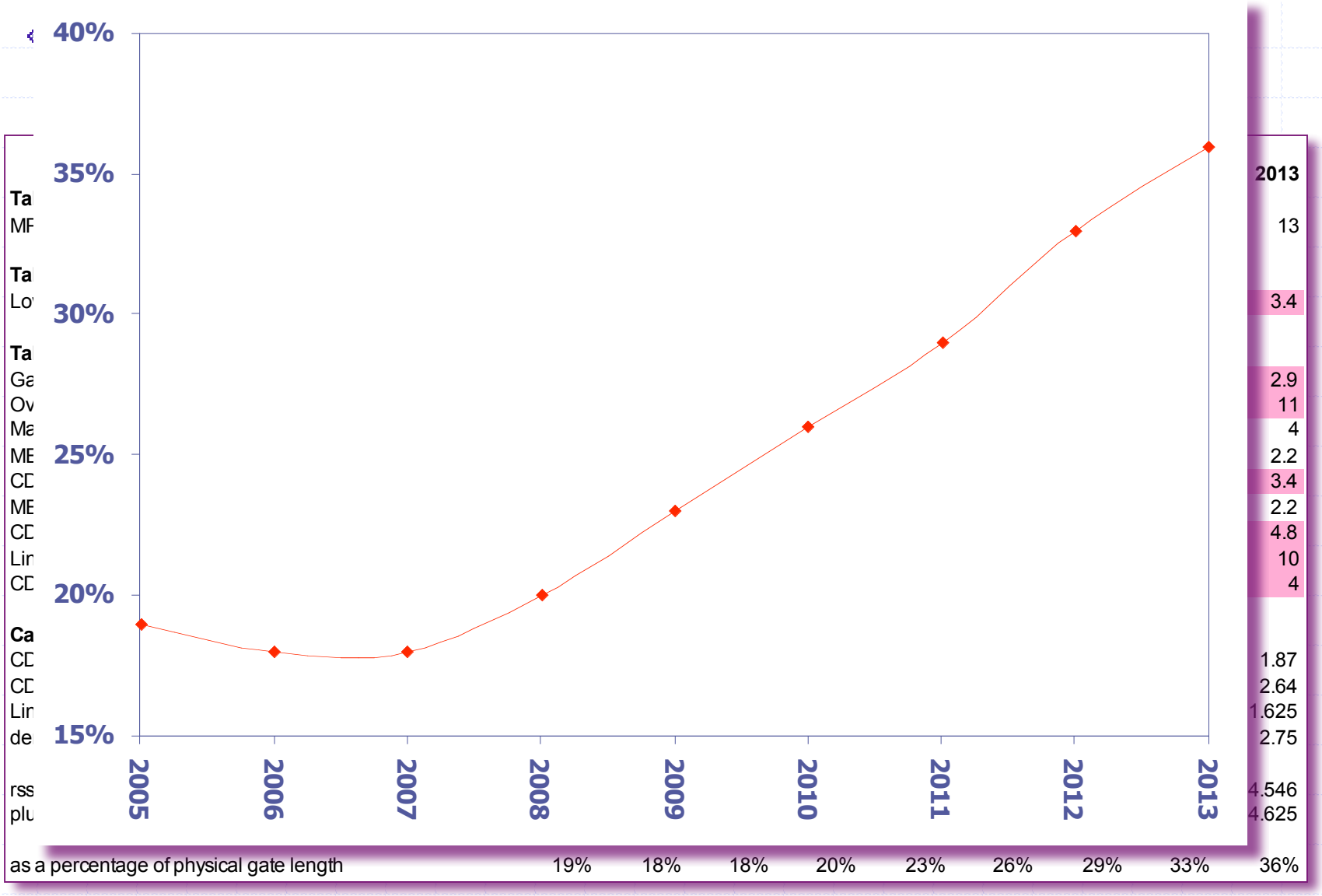
Trend estimation methodology:

- Combine random components, Nested/Isolated CD uniformity and LER, to systematic components like linearity and overlay.

Result (best case scenario)



Alternate Realities?



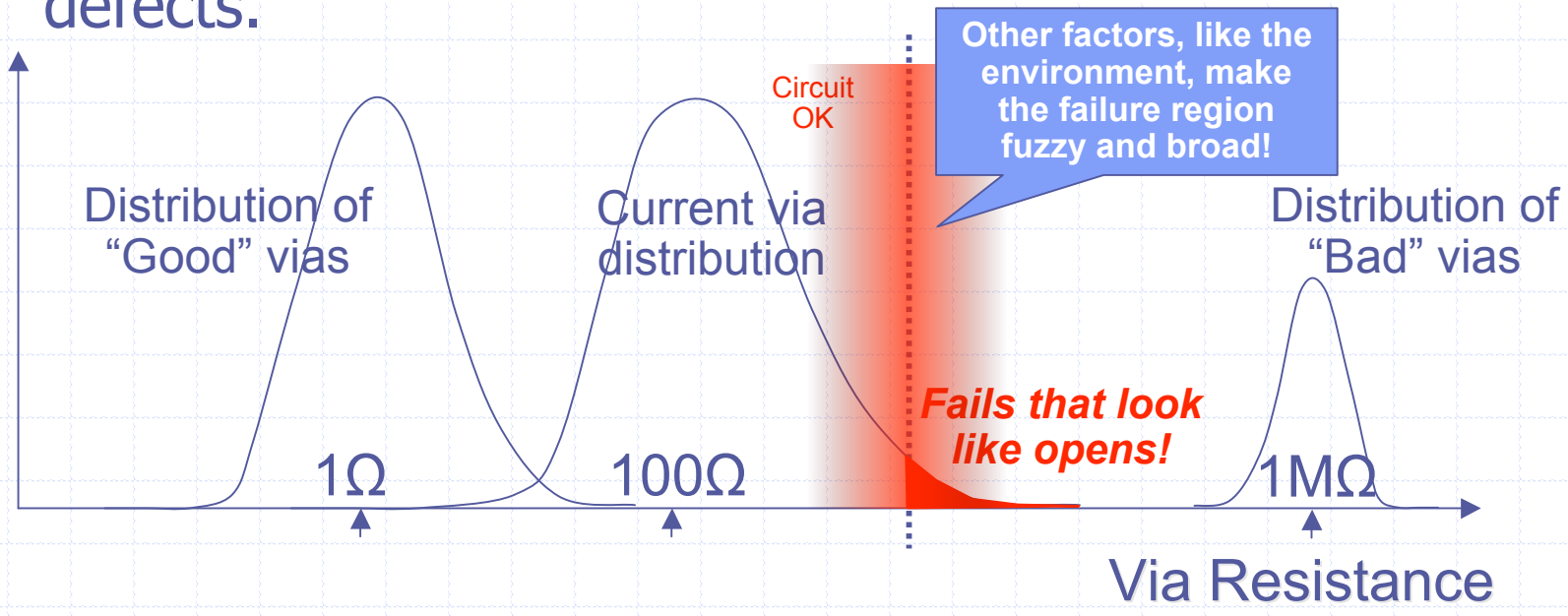
Can we Tolerate 40% variability?

- Not without fundamentally different circuit structures.
  - Rely on variation-tolerant techniques at the system or at the circuit levels?

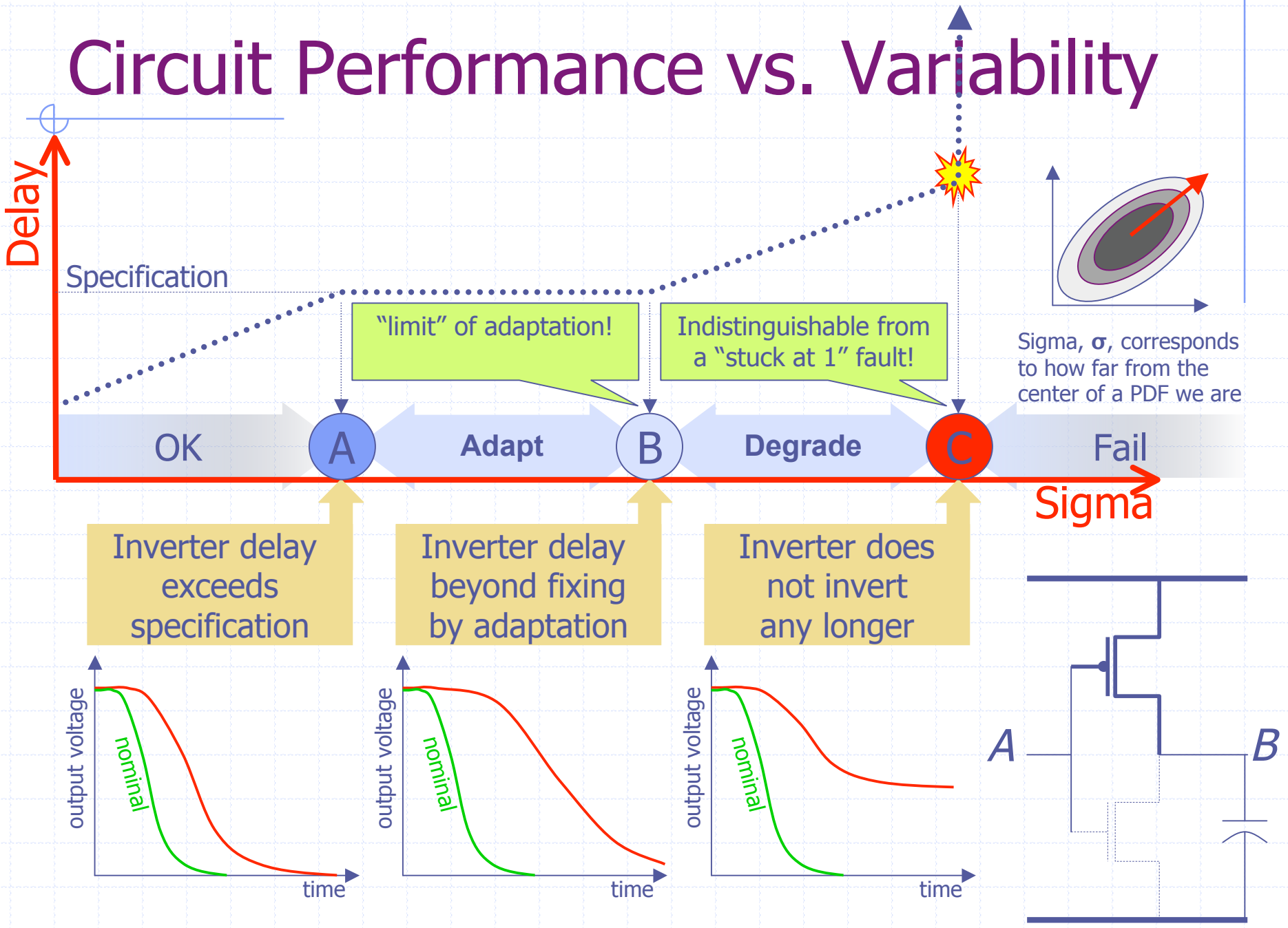
- But... much of the variability is due to diversity.
  - So "uniformity" or "regularity" knobs can be quite important, and nm scale technologies enforce fairly rigid regularity at the layout level..
- Open questions: are there architectures which are "naturally" more regular?

What changes with increased variability?

- Circuits can become permanently or intermittently defective.
- Failure dependence on operating environment makes test coverage very difficult to achieve.
- This can be viewed as the merger of failure modes due to structural (topological), and parametric (variability) defects.

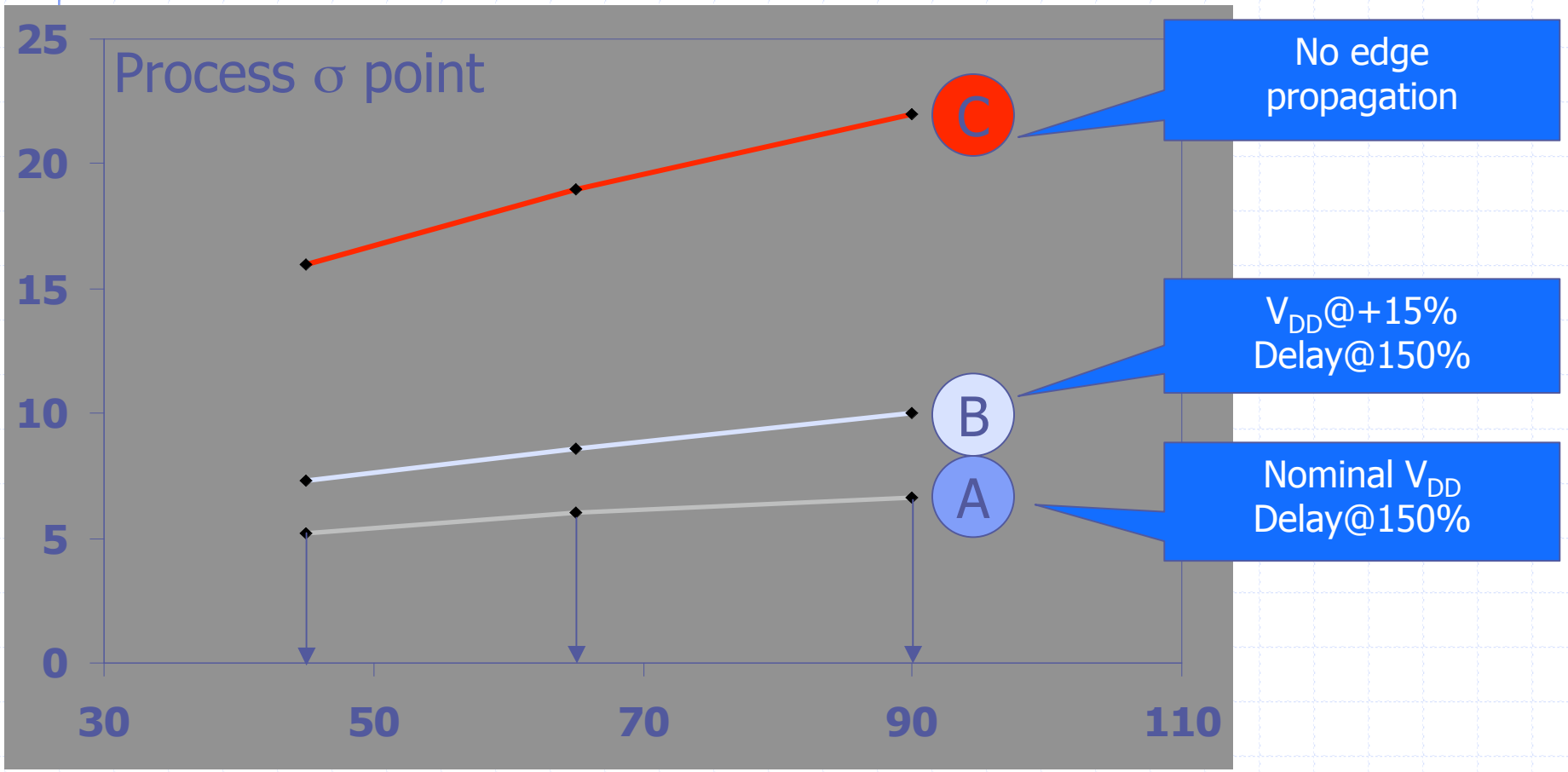


Circuit Performance vs. Variability



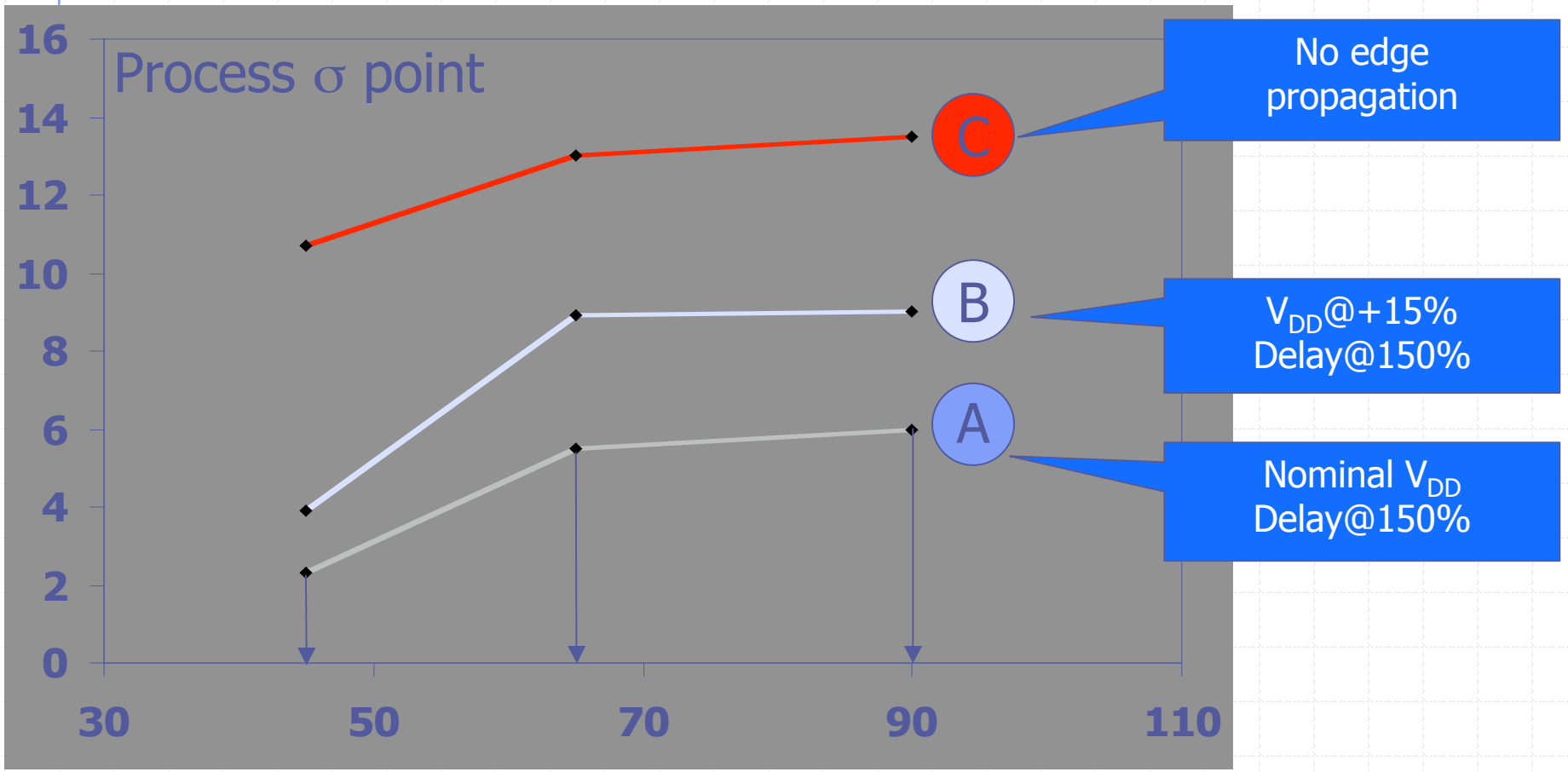
Trend For a Simple Buffer

- Simplest possible circuit (if this fails, everything else will).
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



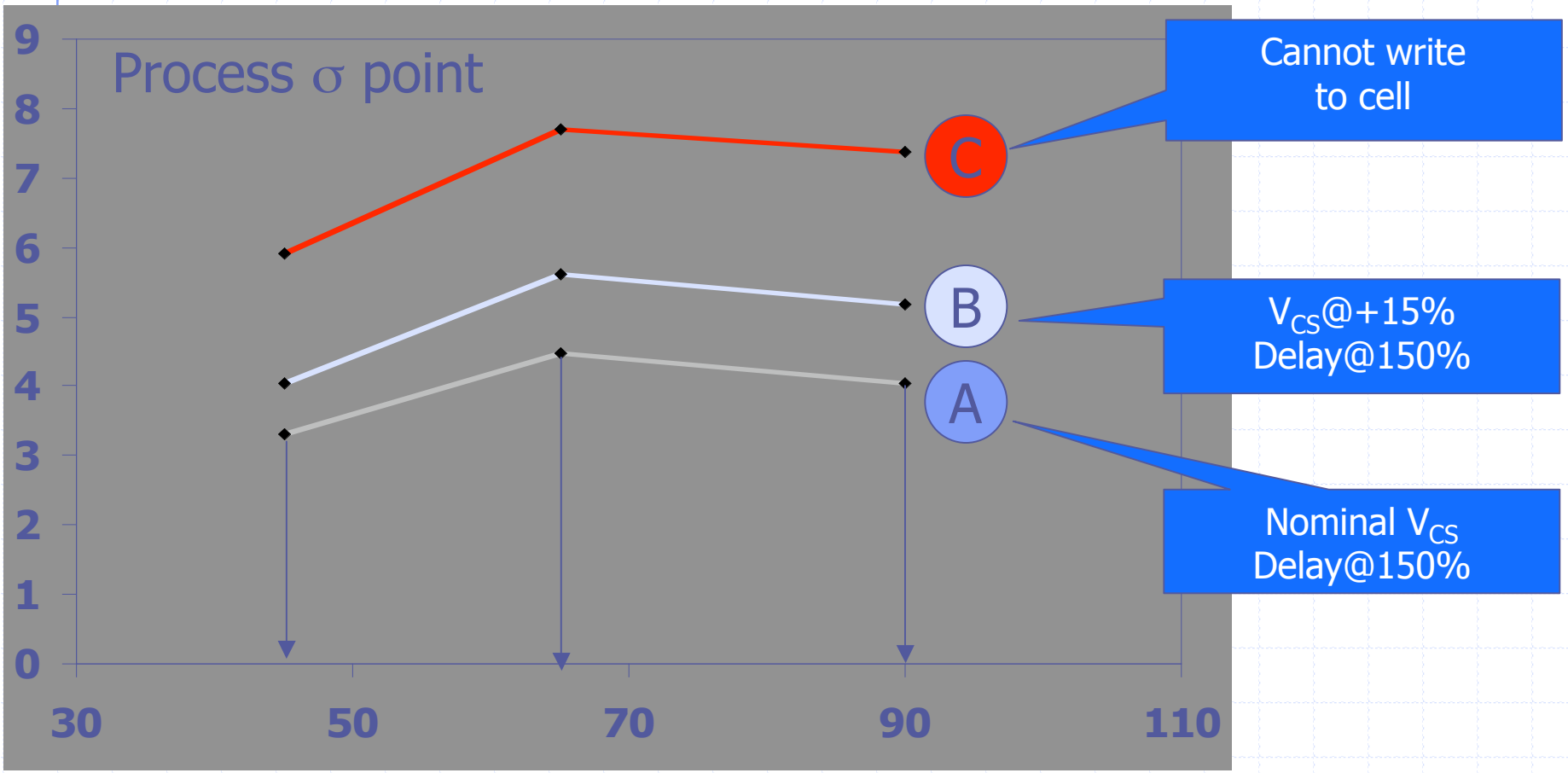
Technology Trend For a Simple Latch

- Pervasive circuit crucial for correct logic operation.
- Performed analysis for 90nm, 65nm and 45nm.
- Clear trend in sigma!



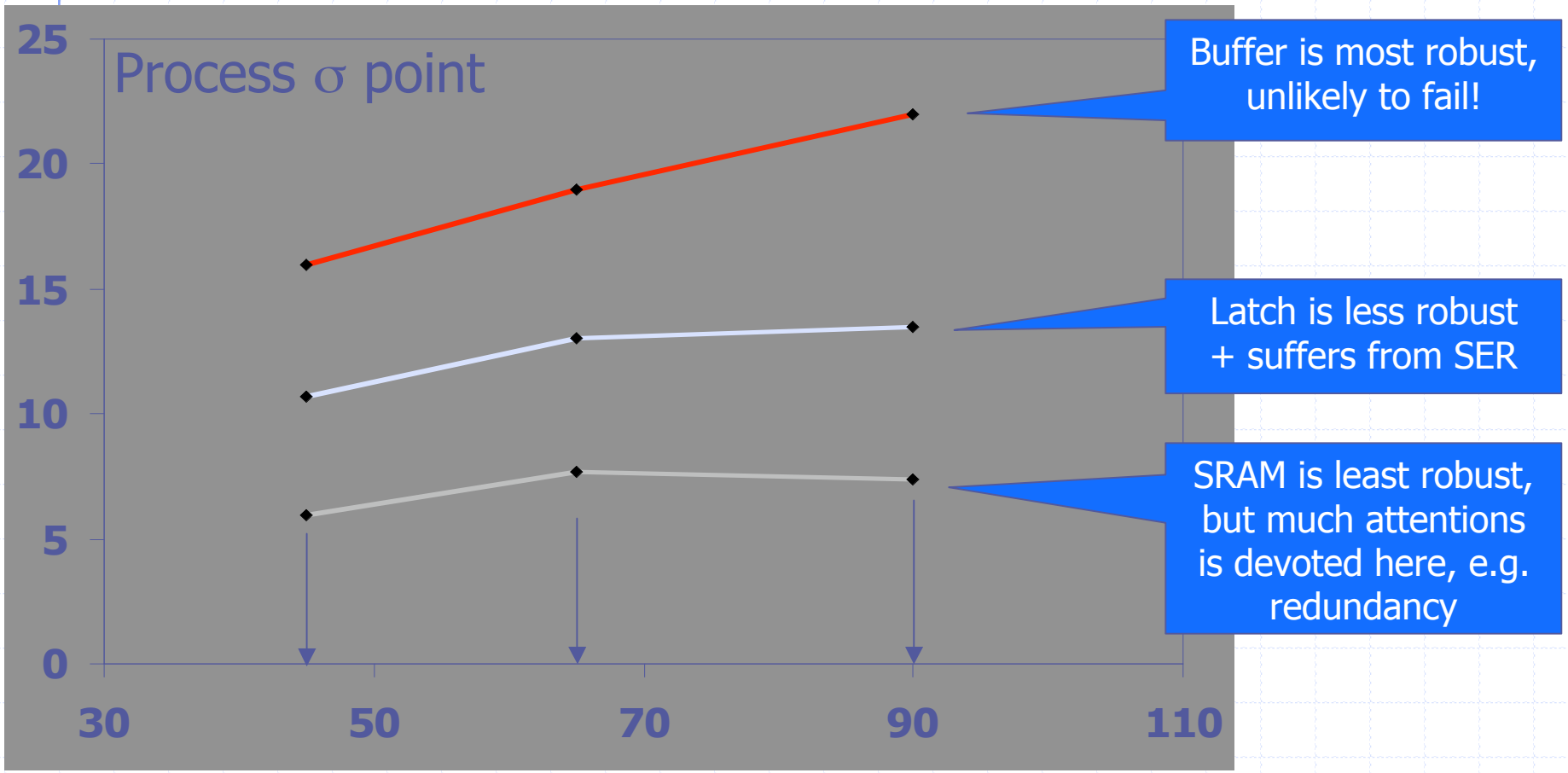
Technology Trend for an SRAM

- SRAM is known to be a more sensitive circuit… (lower σ).
- But, circuit heavily optimized for each technology.
- Much lower σ values + similar trend in sigma!



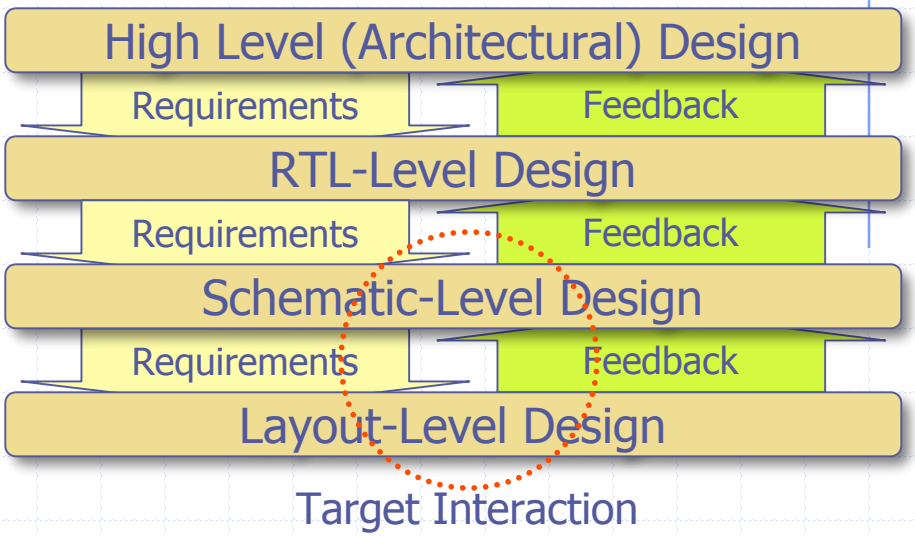
Comparison of Circuits (@Point C)

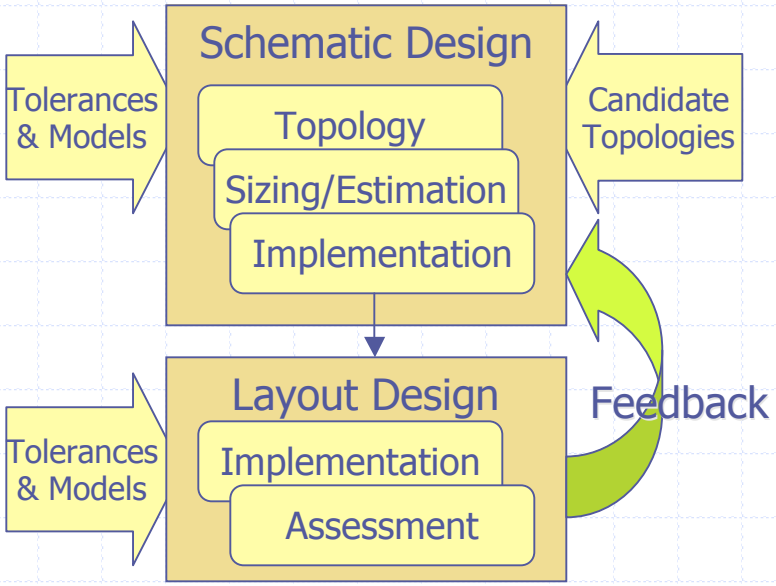
- Global trend remains clear, few generations left?
- Technology trend is modulated by circuit innovation and investment in analysis and optimization tools.



Progress Thus Far

- Manufacturing awareness has clearly entered the "lower" levels of design.
- Current physical implementation highly influenced by OPC/RET at the front-end, and by CMP at the back-end levels.
- Many of these problems are already well solved in current EDA flows.
- But is this enough?





Take Away Message

- Variability, Reliability and Manufacturability are real problems. Solutions require technology-aware design.
- One of the most effective ways to improve design/technology coupling is to reduce implementation diversity.
  - Uniformity at all levels improves predictability, reduces variability, and increases yield.
- Architectures that foster uniformity are likely to fare better in future technologies.

Summary

- Technology is slowing down and getting more expensive.
- The design/manufacturing interface is becoming ever more complex.
- Predictability is suffering!
  - Profitability follows predictability.
- Differentiation will require new innovation.
  - Fewer technology / design-fabric providers.
  - Architectures which foster regularity and are best able to adapt will win!