INVENTIVE

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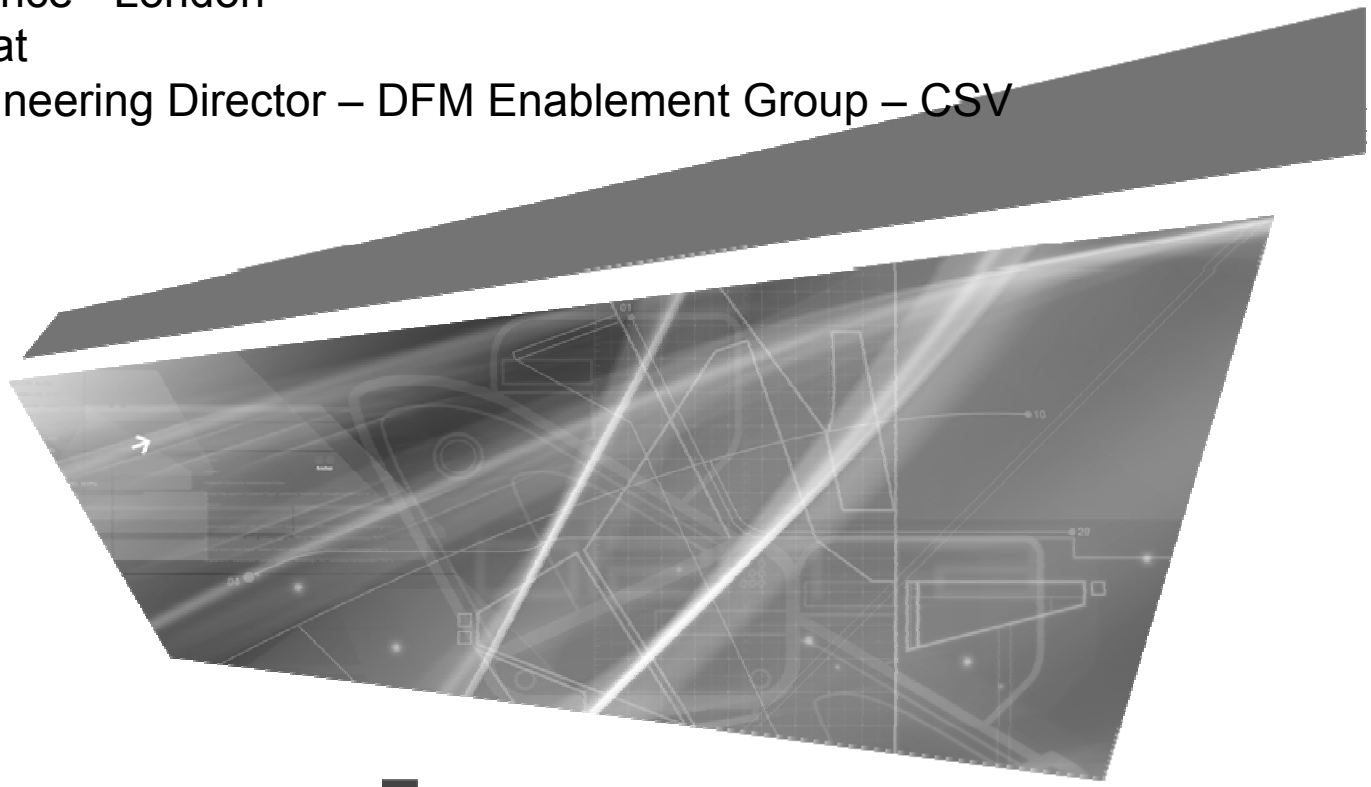
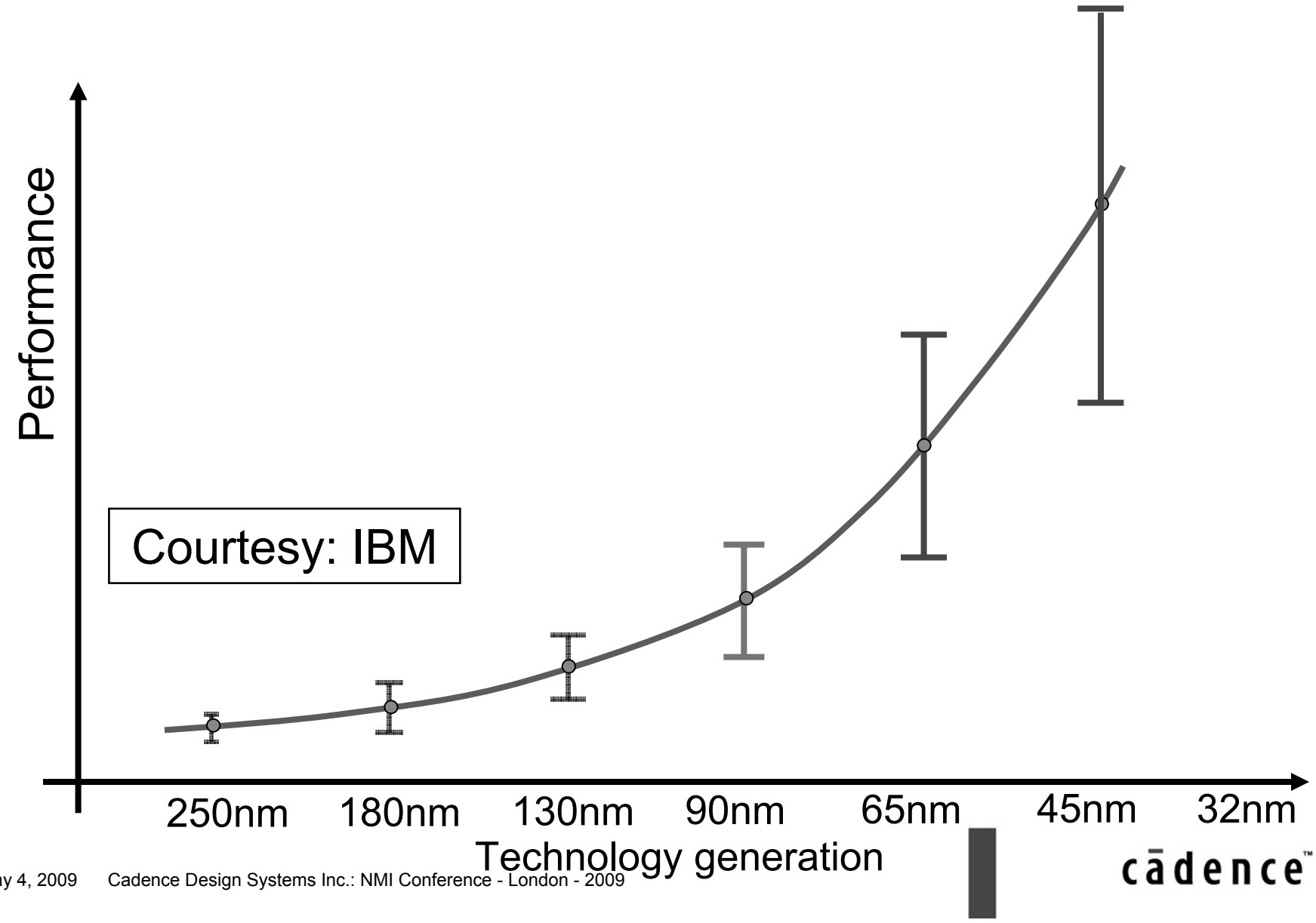
# Analyzing, preventing and correcting the impact of manufacturing variation in advanced node IC design, including physical and electrical effects induced by Litho, CMP and Stress

NMI Conference - London
Philippe Hurat
Product Engineering Director – DFM Enablement Group – CSV
May 2009



# The Variability Challenge



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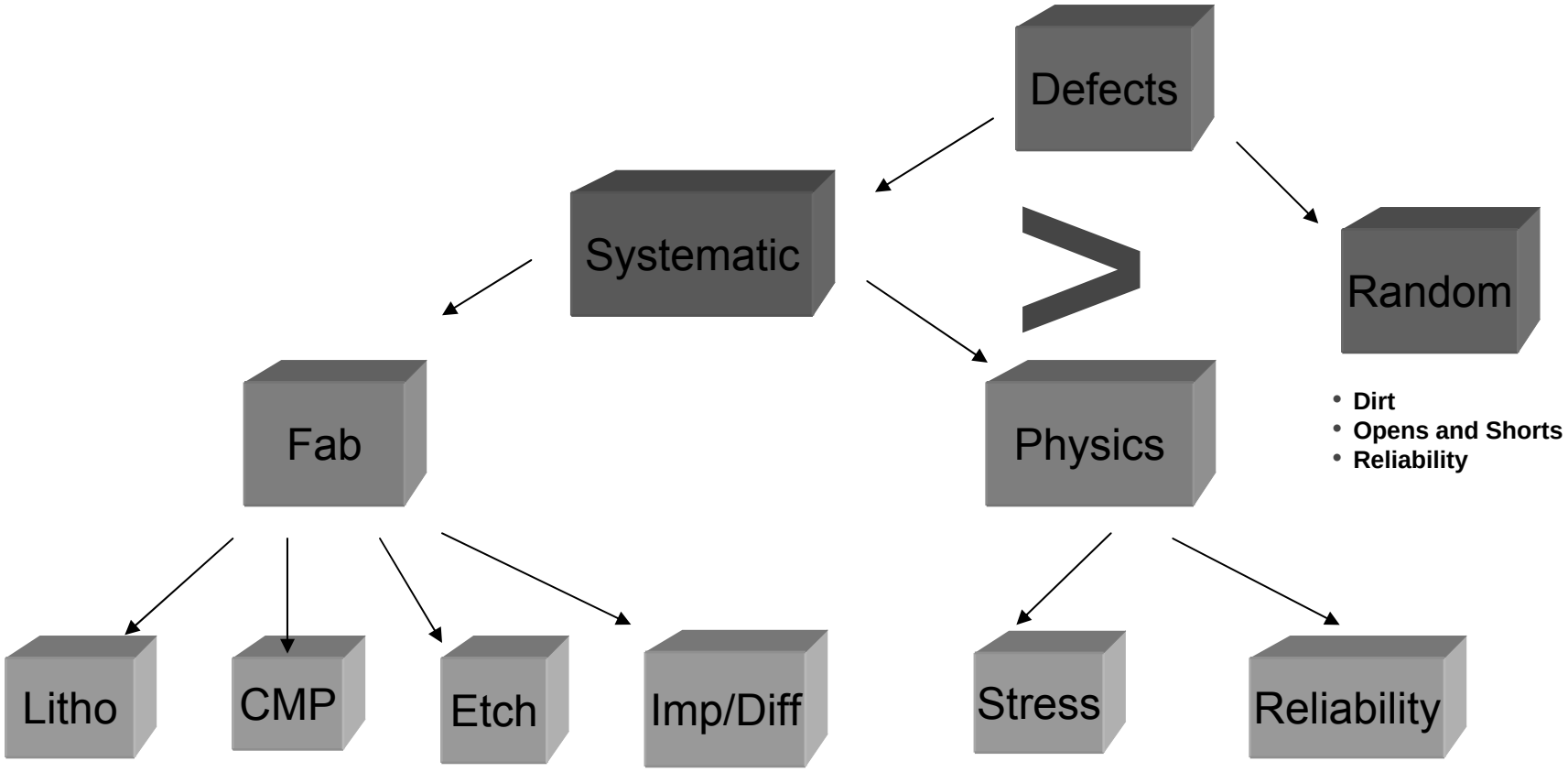
# Manufacturing Variability Sources are Multiple




- Dirt
- Opens and Shorts
- Reliability

- Focus/exposure
- Misalignment
- Aberration
- Resist integrity
- Scanner H/V
- Local density

- ILD thickness
- Dishing
- Over polish
- Density effects

- Over/Under etch
- Profile
- CD control
- Local density
- Line edge roughness

- Implant shadowing
- RTA control
- Thermal uniformity
- Oxide control
- Random dopant fluctuations
- Drain overlap (Leff)
- Dopant activation

- DSL
- STI/Oxide growth
- SiGe
- Via failure
- Line Failure
- Delamination

- Electro migration
- Hot carrier
- NBTI
- Gate oxide
- ESD



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# Challenge of Manufacturing Effects and their Impact on Designs

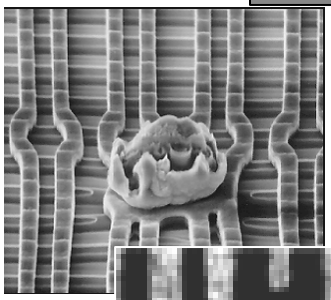
130nm

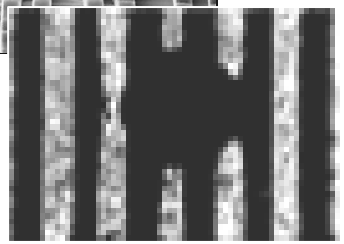
45nm

32nm

Via failure

Particle defects





Increase in systematic variations

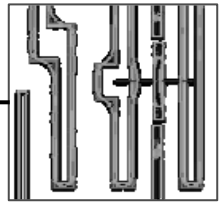
Via failure

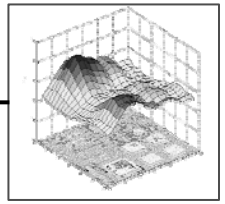
Particle defects

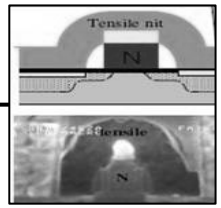
Litho and etch effects

CMP effects

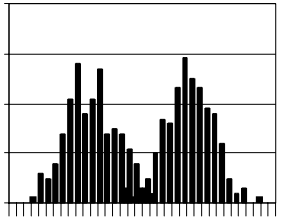
Stress effects








Litho and CMP Hotspots



Timing, power variation

Physical changes creates electrical variations

Via failure

Particle defects

Litho and CMP Hotspots

Timing, power variation

| Typical context variation on | 45nm | 32nm |
|---|---|---|
| Transistor delay due to litho | 5-7% | ? |
| Transistor delay due to stress | 15% | ? |
| RC interconnect due to CMP | 5% | ? |
| RC interconnect due to Litho | 5% | ? |



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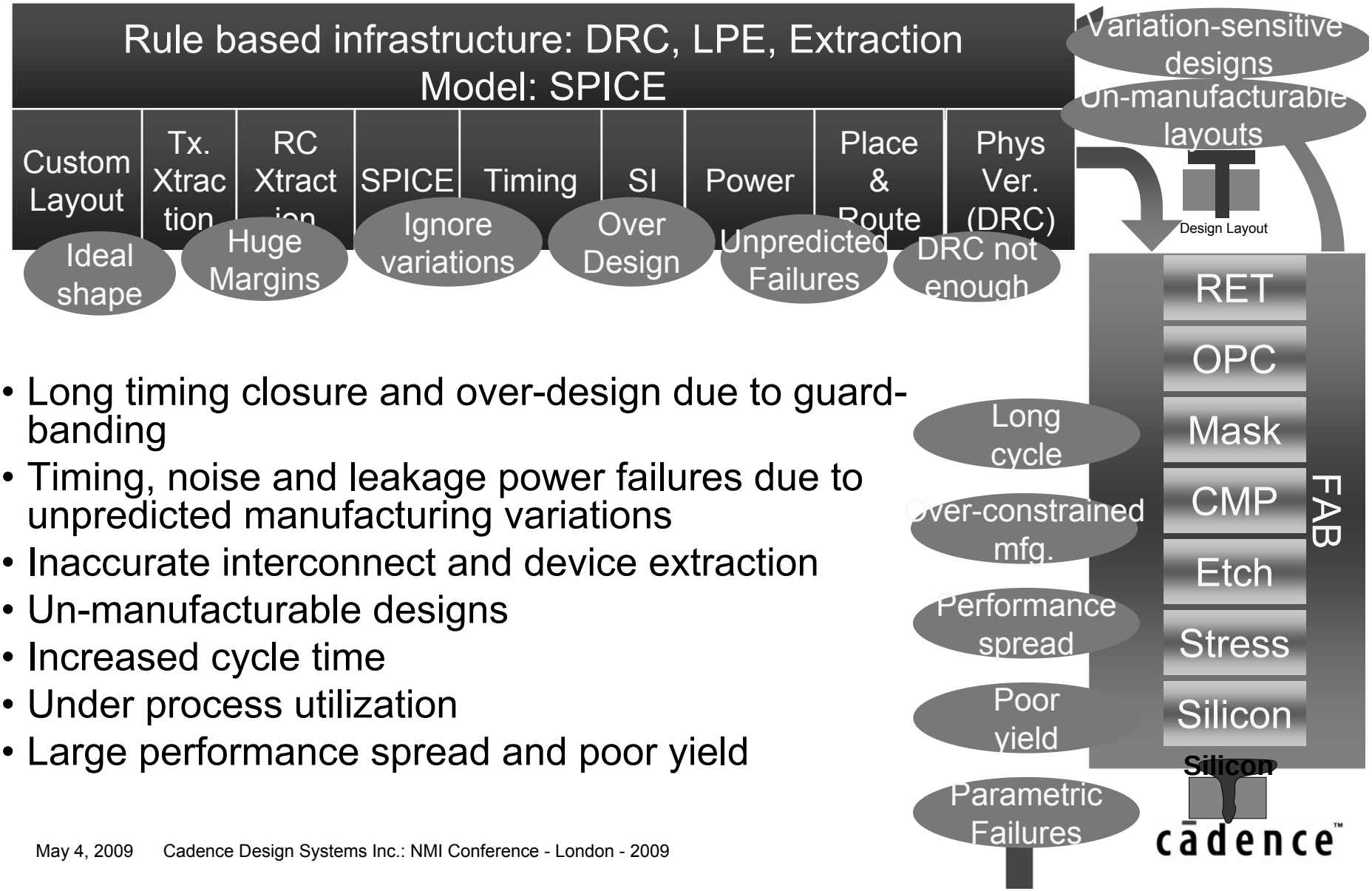
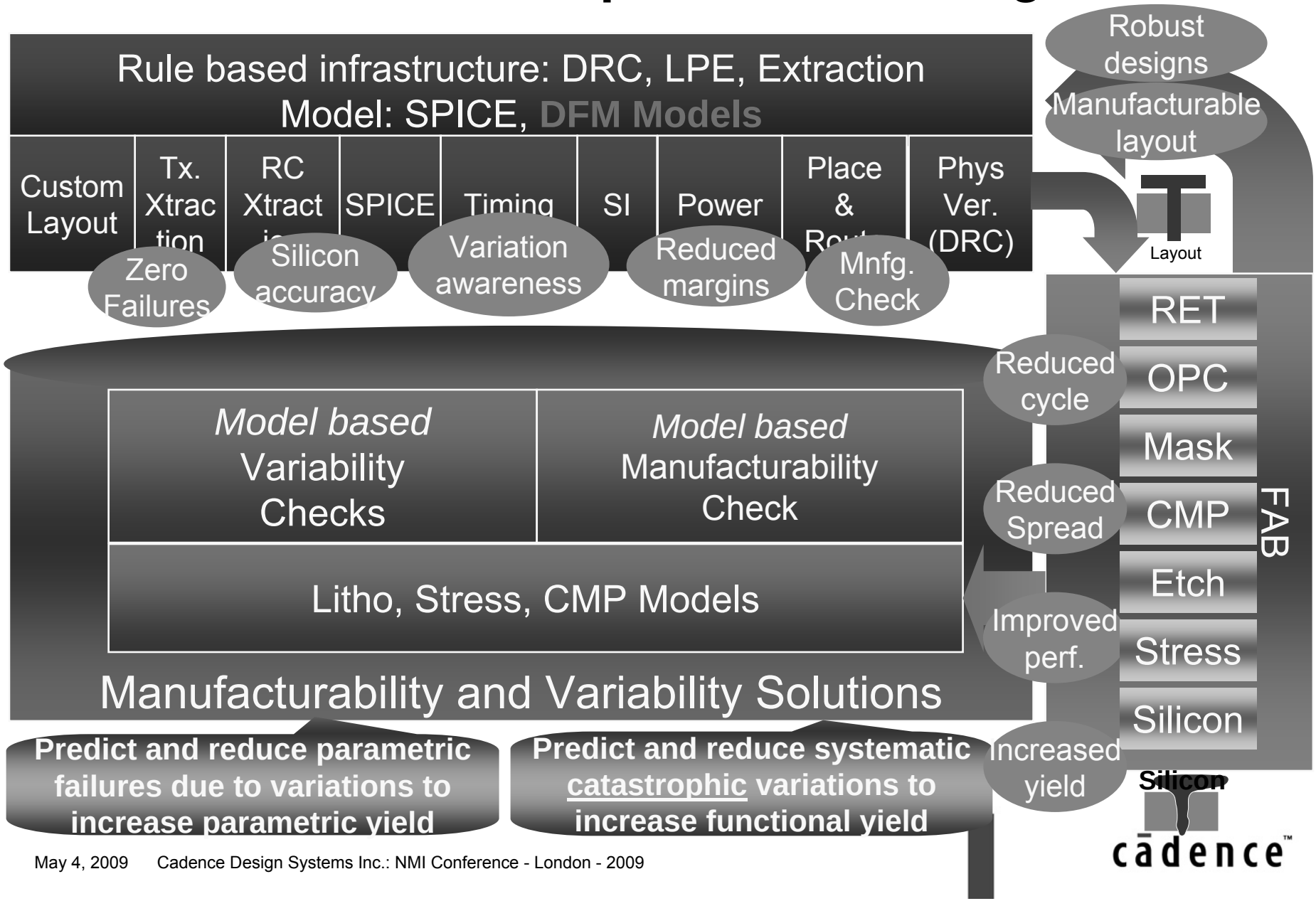
# Rule-Based Infrastructure is Unable to Account for Advanced Node Mfg. Variations




- Long timing closure and over-design due to guard-banding
- Timing, noise and leakage power failures due to unpredicted manufacturing variations
- Inaccurate interconnect and device extraction
- Un-manufacturable designs
- Increased cycle time
- Under process utilization
- Large performance spread and poor yield

# Design Infrastructure Evolution to Predict Mfg. Variations and their Impact on the Design



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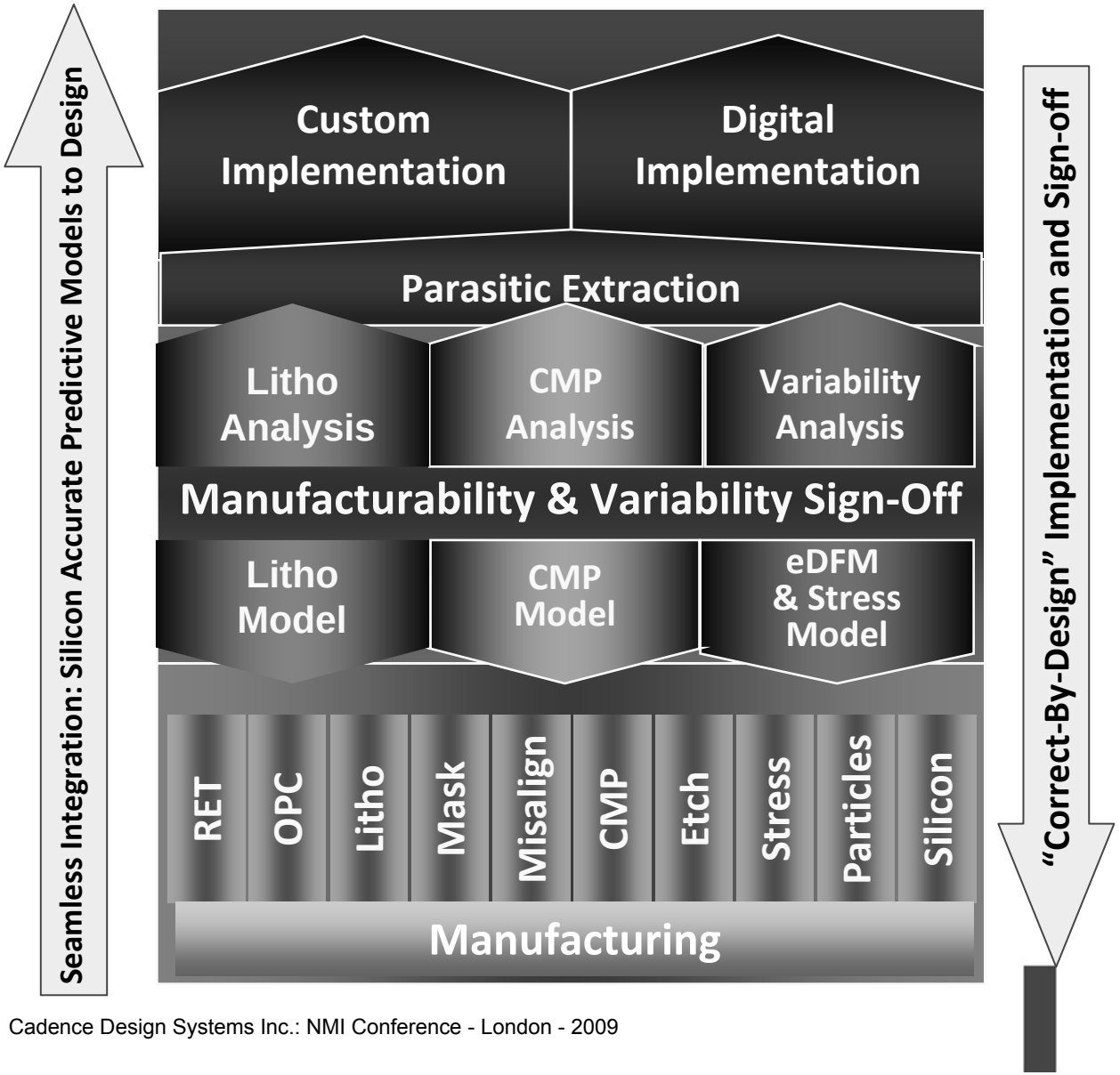
# Manufacturability and Variability Solutions

## Prevention, Analysis, Optimization and Sign-Off



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# Manufacturability and Variability Solutions

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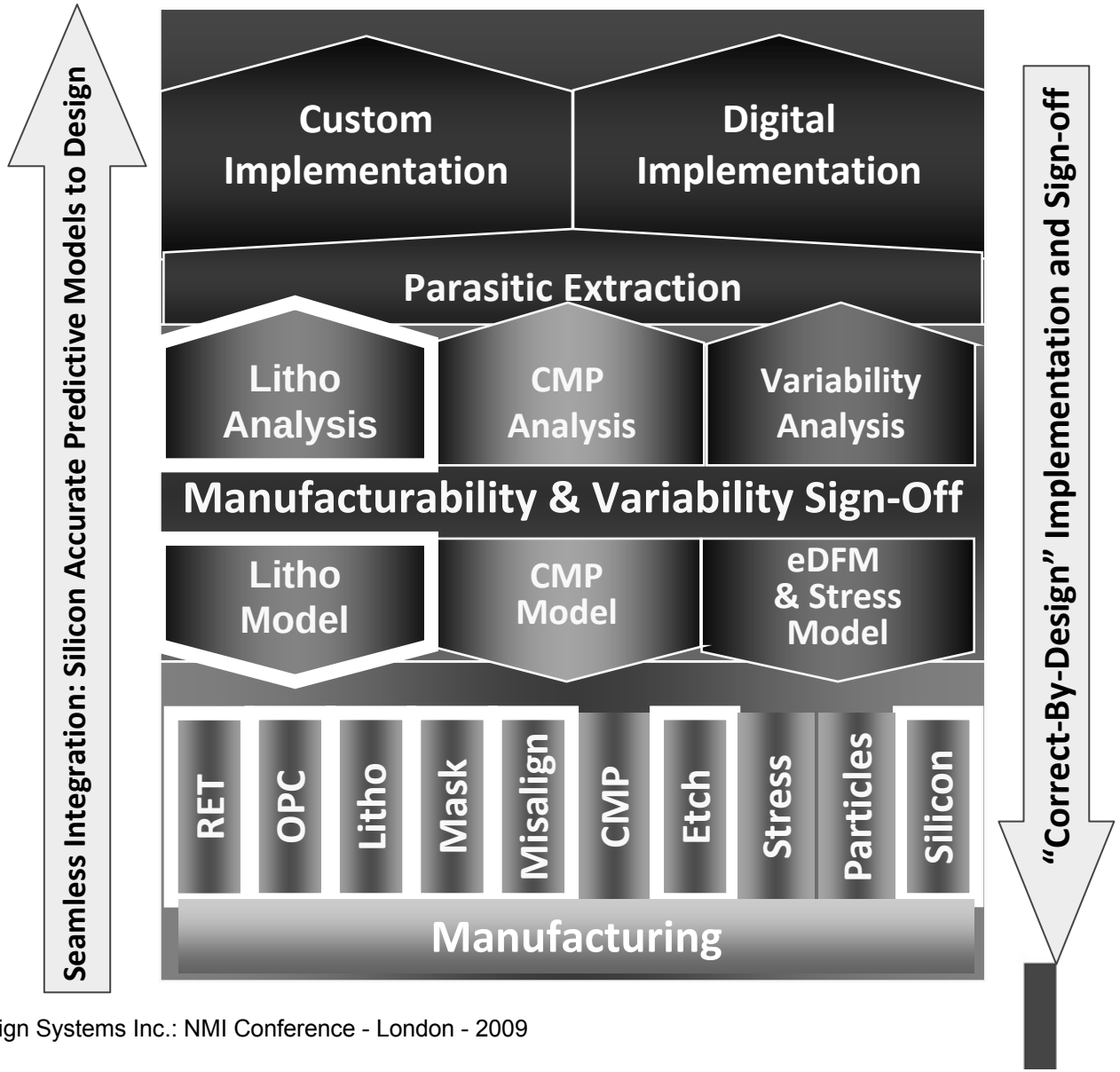




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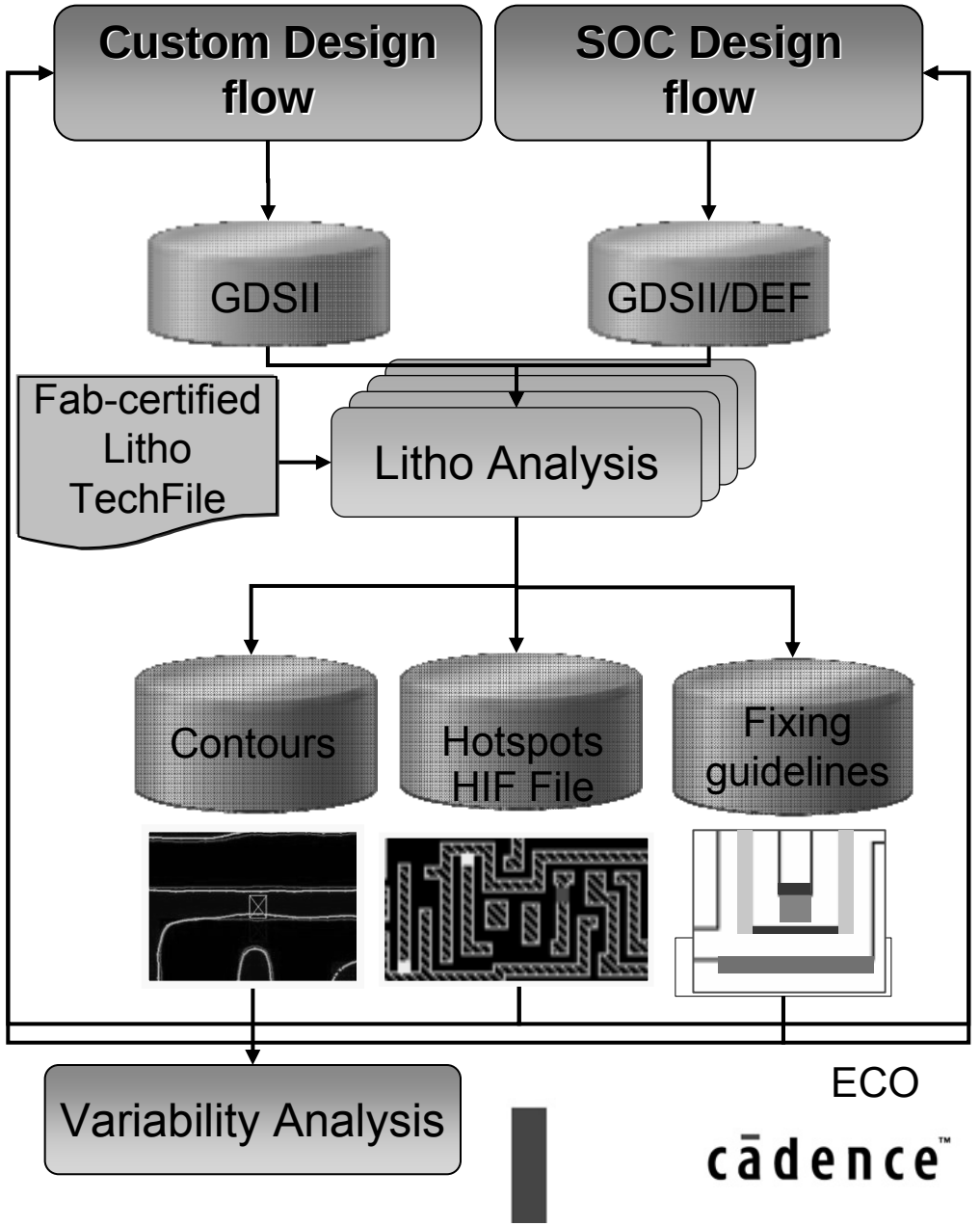
# Litho Analysis Requirements

- Multi foundry support
  - Capture foundry specific litho performance
  - Litho and OPC aware but OPC independent
- Meet designers' runtime expectations
  - Order of magnitude faster than OPC
  - Scalable and distributed on cheap H/W platform
  - Fully support hierarchical approach
- Fits into design flows
  - Integrated in custom layout editors for interactive checks
  - Convergent automated fixing flow for SOC designs
  - Provide fixing guidelines to designers or design tools



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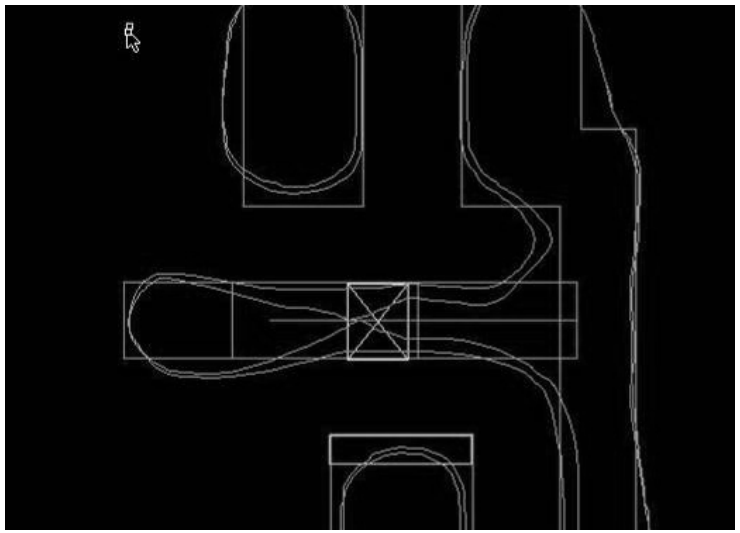
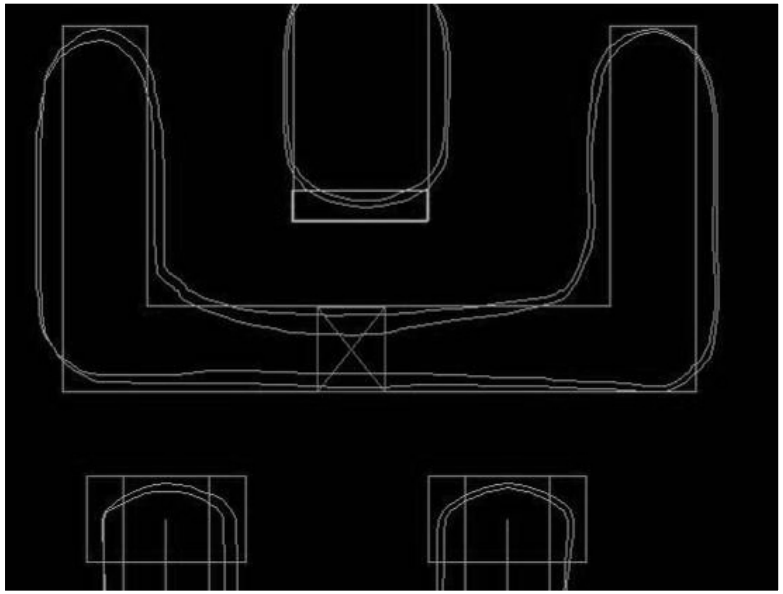
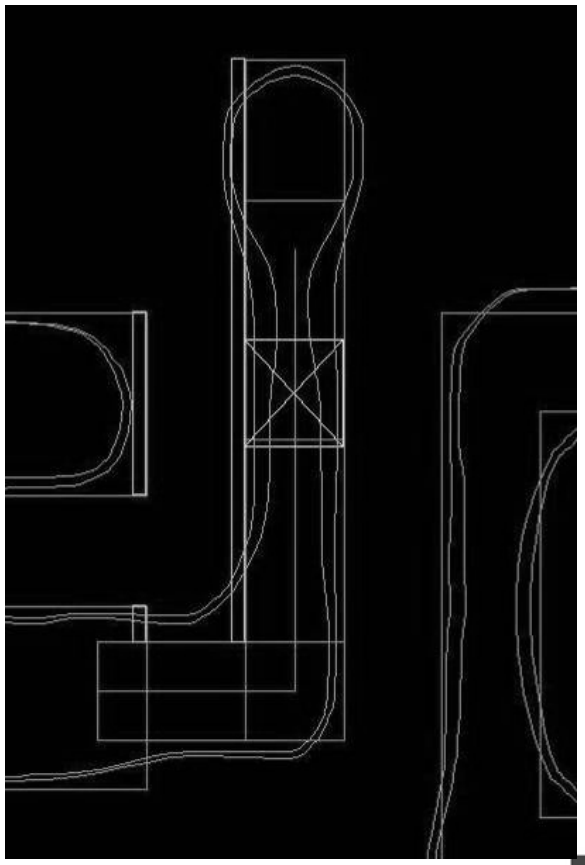
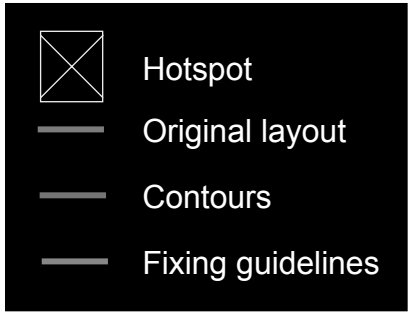
# Level 1 Litho Hotspots on 45nm Design







- Litho analysis tool detects Must-Fix hotspots and produces fixing guidelines



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# Lithography-Checking development and Deployment at 45nm



## Freescale SoC-Level DFM Matrix

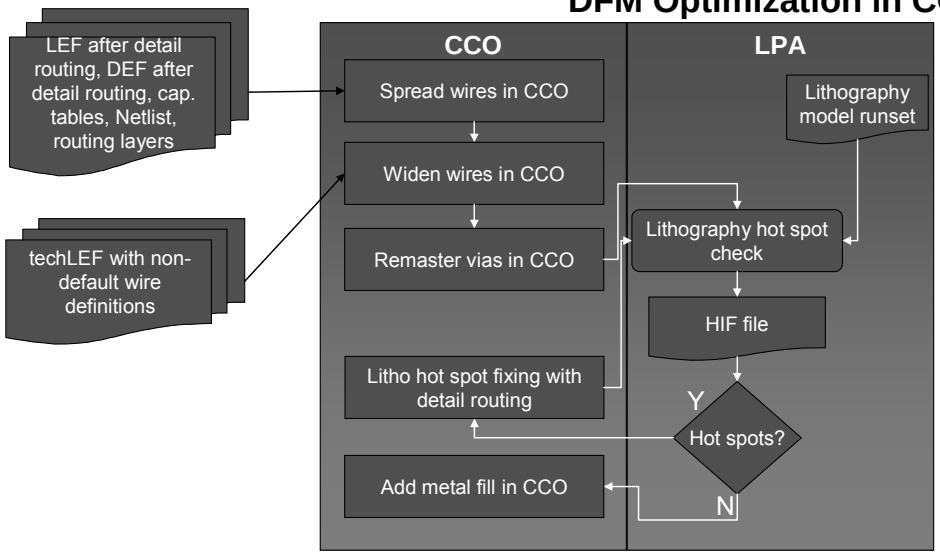
| Defect Class | DFM Technique | Process technologies → | | | | |
|---|---|---|---|---|---|---|
| Random | Redundant Vias | | | | | |
| | Wire Spreading | | | | | |
| | Wire Widening | | | | | |
| | Logic Restructuring | | | | | |
| Systematic | Timing-aware Fill | | | | | |
| | Model-based Litho Analysis / Fix | | | | | |
| | Model-based CMP Analysis | | | | | |
| Parametric | Model-based Extraction | | | | | |
| | SSTA | | | | | |

## Requirement for Design-Oriented Litho DFM Solution

- ►Mission Statement for Litho Check
  - Improve yield and reliability by using foundry-qualified simulation models and LPA to identify and eliminate Litho Hot Spots
- ►Foundry support
  - Model-based litho DFM solution must be qualified by foundry
    - Freescale is using multi-source for foundries
  - Too expensive to support multiple tools
    - Selected tool with most extensive foundry support
- ►Design Integration
  - Must cover all design styles: Analog, mixed-signal, standard cells, custom IP, large SOC
  - Should be integrated in custom and SOC design flows
- ►Ease of deployment
  - Speed of model-based solution is key for designers' adoption
  - Ease of setup and maintenance
  - Integration in design flow



## DFM Optimization in CCO




CMP-model driven hot spot fixing and extraction flow not shown

# Convergent Automated Chip Level Lithography Checking and Fixing at 45nm

SPIE 2009

## LPA Model Validation

- The models were checked against contours created with the production flow by using verification test patterns that were not used for the techfile calibration.

| 2.0nm condition | layer | cut_cs | cs_in_CT | Ratio |
|---|---|---|---|---|
| EnFn | 300 | 92.22902197 | 91.8317891 | 99.57% |
| E0Fn | 301 | 92.40148303 | 92.02110459 | 99.59% |
| EpFn | 302 | 92.61511853 | 92.23824203 | 99.59% |
| EnF0 | 303 | 92.41944169 | 91.98462309 | 99.53% |
| E0F0 | 304 | 92.52451681 | 92.02391206 | 99.46% |
| EpF0 | 305 | 92.65903813 | 91.87532503 | 99.15% |
| EnFp | 306 | 92.28602003 | 91.80205259 | 99.48% |
| E0Fp | 307 | 92.42639722 | 91.98578628 | 99.52% |
| EpFp | 308 | 92.58319238 | 92.11063191 | 99.50% |

| 1.5nm condition | layer | cut_cs | cs_in_CT | Ratio |
|---|---|---|---|---|
| EnFn | 300 | 92.22902197 | 91.54909544 | 99.26% |
| E0Fn | 301 | 92.40154116 | 91.73884056 | 99.28% |
| EpFn | 302 | 92.61516516 | 91.97546641 | 99.31% |
| EnF0 | 303 | 92.41958309 | 91.70825191 | 99.23% |
| E0F0 | 304 | 92.52456672 | 91.86318159 | 99.07% |
| EpF0 | 305 | 92.65900944 | 91.24254566 | 98.47% |
| EnFp | 306 | 92.28602294 | 91.50426269 | 99.15% |
| E0Fp | 307 | 92.42645191 | 91.66538331 | 99.18% |
| EpFp | 308 | 92.56324628 | CRASH | NA |

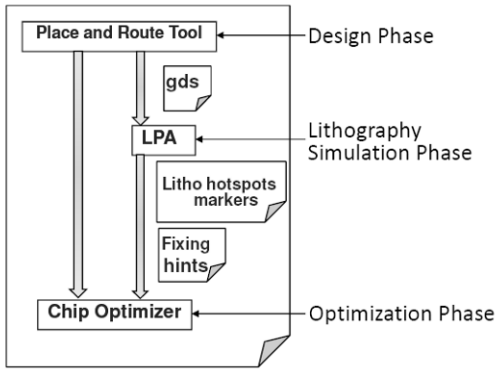
| 1nm condition | layer | cut_cs | cs_in_CT | Ratio |
|---|---|---|---|---|
| EnFn | 300 | 92.22902197 | 90.98662247 | 98.63% |
| E0Fn | 301 | 92.40154116 | 91.13841544 | 98.63% |
| EpFn | 302 | 92.61516516 | 91.44302019 | 98.73% |
| EnF0 | 303 | 92.41955309 | 91.20003222 | 98.69% |
| E0F0 | 304 | 92.52456672 | 91.01387563 | 98.37% |
| EpF0 | 305 | 92.65900944 | 90.19578253 | 97.34% |
| EnFp | 306 | 92.28602294 | 90.96382081 | 98.57% |
| E0Fp | 307 | 92.42645191 | 90.96716903 | 98.42% |
| EpFp | 308 | 92.58324628 | 90.60715684 | 97.89% |

| 0.5nm condition | layer | cut_cs | cs_in_CT | Ratio |
|---|---|---|---|---|
| EnFn | 300 | 92.22902197 | 89.06725041 | 96.57% |
| E0Fn | 301 | 92.40154116 | 89.19074981 | 96.53% |
| EpFn | 302 | 92.61516516 | 89.9344085 | 97.11% |
| EnF0 | 303 | 92.41955309 | 90.03338397 | 97.42% |
| E0F0 | 304 | 92.52456672 | 89.81191534 | 97.07% |
| EpF0 | 305 | 92.65900944 | 88.39235572 | 95.38% |
| EnFp | 306 | 92.28602294 | 89.59740169 | 97.09% |
| E0Fp | 307 | 92.42645191 | 89.09386613 | 96.39% |
| EpFp | 308 | 92.56324628 | 87.43603922 | 94.46% |

- **The LPA models matched the production contours at more than 99% with a 2nm tolerance, 97.3% with 1nm tolerance and 94.6& with a 0.5nm tolerance.**

## Model Application

**Integration of Litho Hotspot detection and fixing in a conventional design flow**




26 Feb 2009, SPIE

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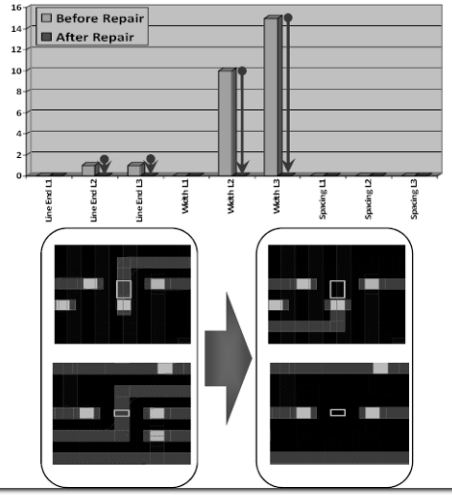
## Fixing Results

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# Design-side Signoff to prevent lithography-driven physical failures of advanced node chips



## Run-time

| | Area ($mm^2$) | Layers | # of CPUs | Run-time |
|---|---|---|---|---|
| N65 | 83 | All | 40 | 22h |
| N65 | 58 | All | 40 | 16h |
| N65LP | 108 | All | 40 | 27.5h |
| N65LP | 4.8 | All | 40 | 1.3h |

| Area ($mm^2$) | Layers | # of CPUs | Run-time |
|---|---|---|---|
| 82 | PO | 20 | 10.8h |
| 82 | PO | 40 | 5.5h |
| 82 | PO | 60 | 3.82h |

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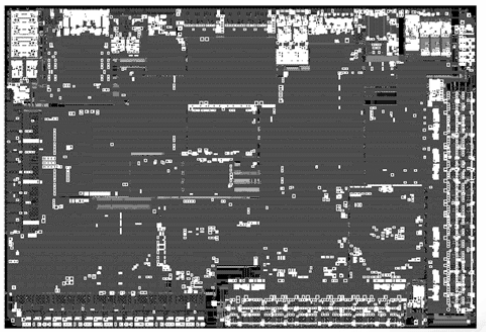
## Accuracy

- A 12mmx9mm chip was sent to foundry to run internal LPC service. Litho hot-spot was compared to the LPA simulation. The result matches.
- Other small standard cell and memory test cases was verified with foundry and LPA also.



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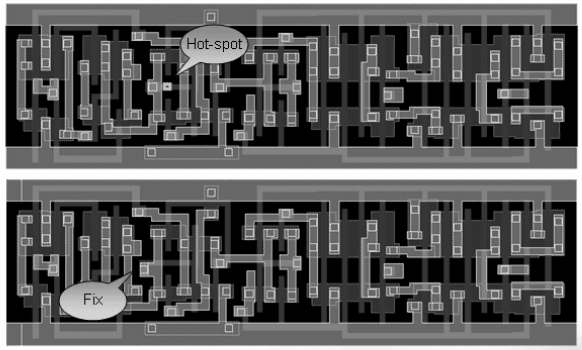
## IP level hot-spot

- Standard cell hot-spot and fix. All hot-spot could be fixed without increasing area, in most case just a few nm touch.

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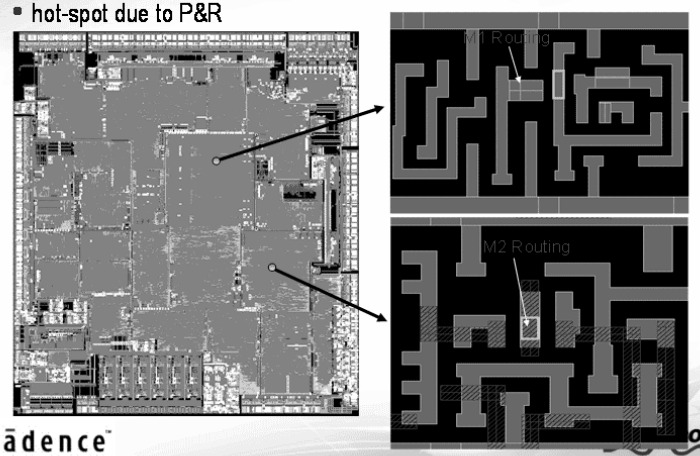
## Chip Level Hot-Spot

- hot-spot due to P&R

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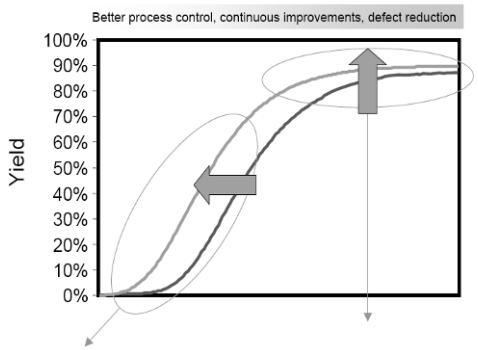
# Design for Manufacturability in Advanced Node Design Flow

## Yield from Ramp-up to Volume

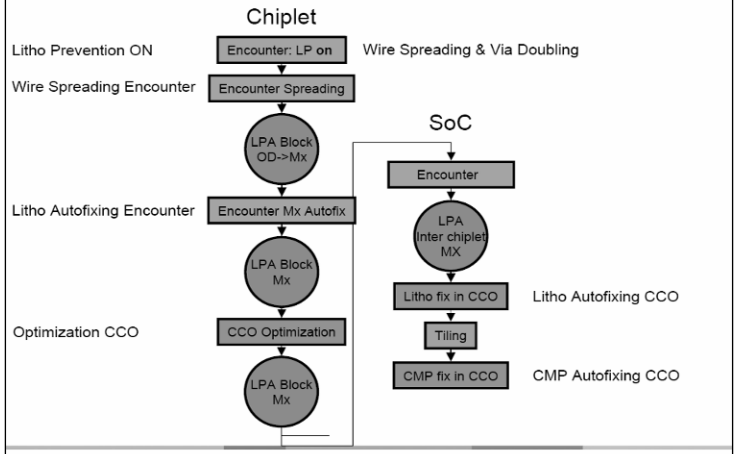



DfM in Phase1:
Desensitize to systematic yield loss
→ **Time-to-Market**

DfM in Phase2:
Desensitize to random defects
→ **Die price**

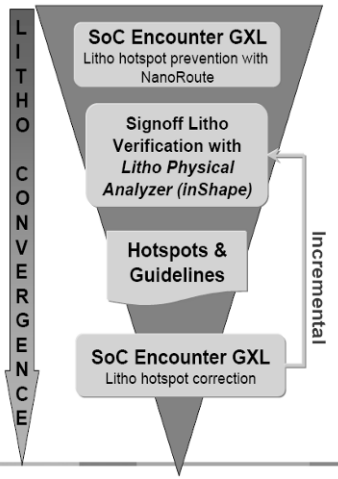


## Solution: Manufacturing Aware Design Flow






## Litho Prevention with NanoRoute

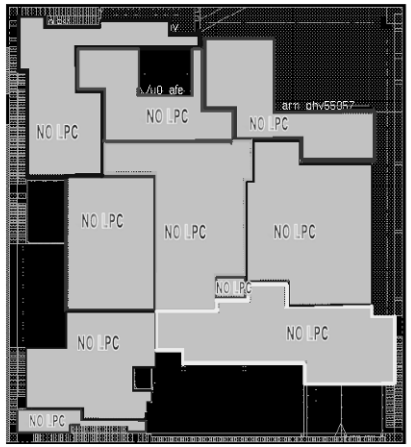



– **Via/Wire Optimization**
– **Swap Via** (Remaster Via)
– **Reduce Via**
– **Spread Wire**
– **Widen Wire**
– **Remove Jog**
– **Widen Jog**

setNanoRouteMode -
routeWithLithoDriven true



## Hierarachy Lithography Checks




-Check Litho at Chiplet Level

-Create no lpc marker arround chiplet boundaries

- Run Full chip LPC





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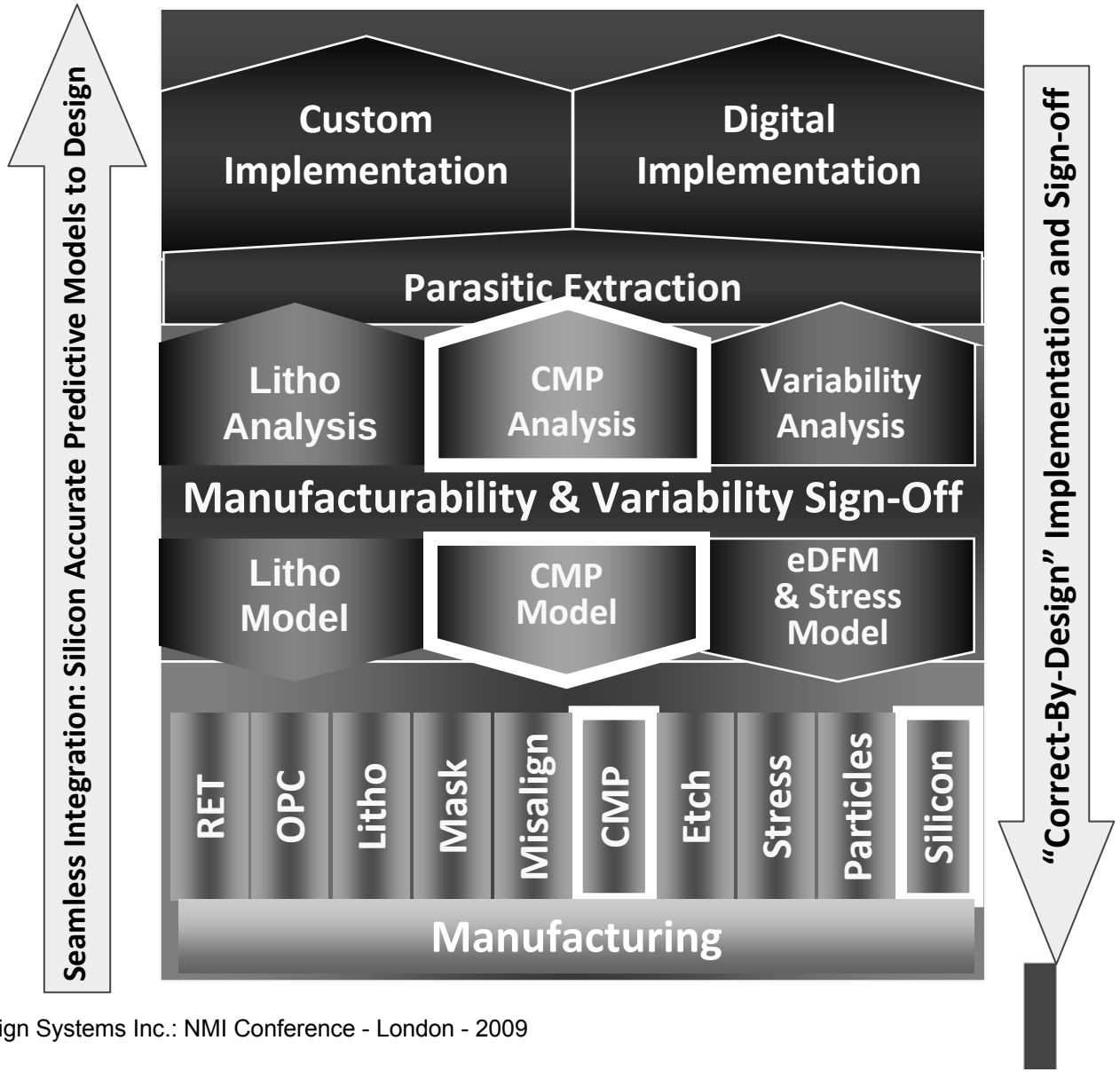
# Manufacturability and Variability Solutions

## Prevention, Analysis, Optimization and Sign-Off



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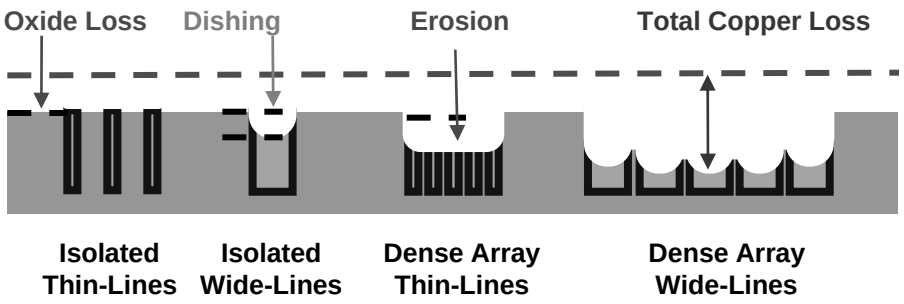
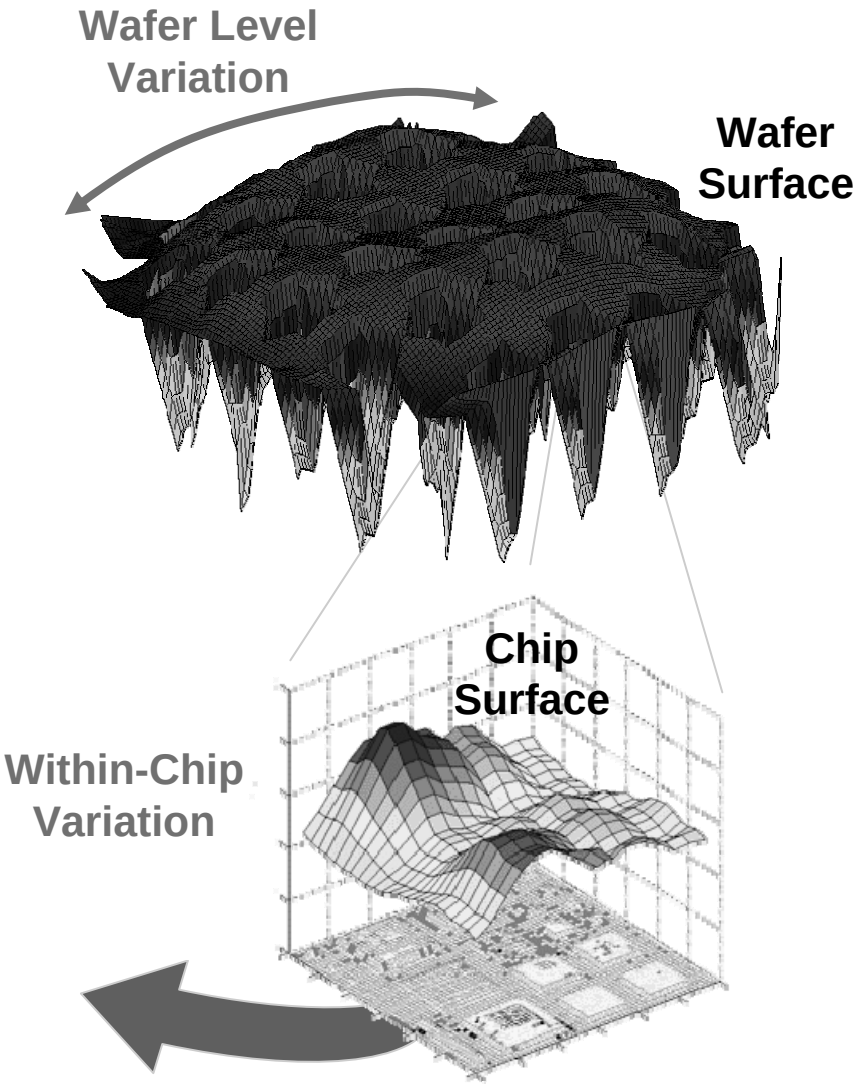
# CMP Effects: Interconnect Variation

- Within-Chip Variation is Huge!
  - Thickness Variation: 10% to 40%
  - Width Variation: 10% to 40%
- Due to Design Impact on Manufacturing
  - Varying Feature Density
  - Varying Feature Widths
- Variation Leads to Over-Compensation in Design
  - Timing Failures
  - Decreased Performance
  - Increased Power Consumption



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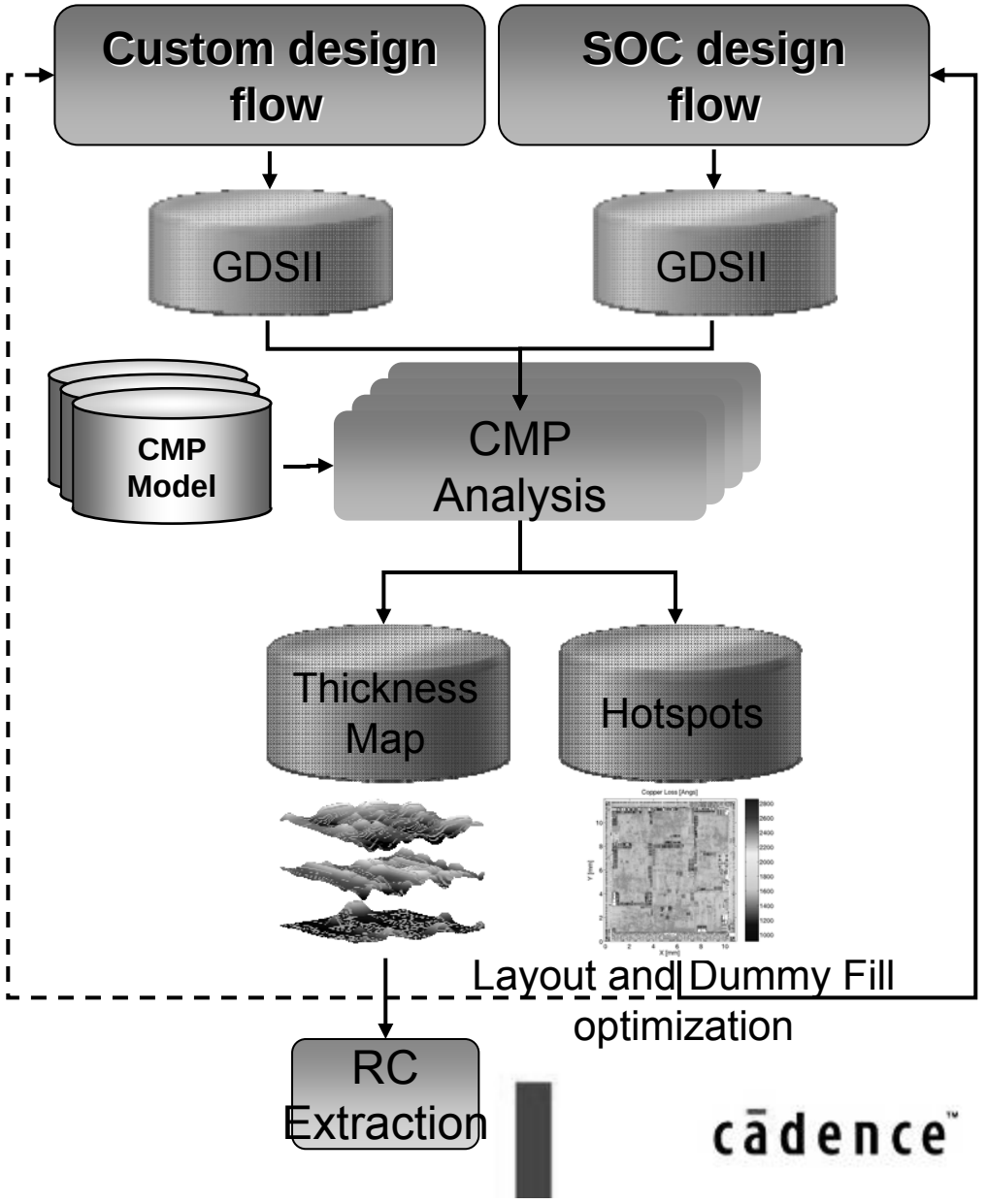
# CMP Analysis Requirements

- Accurate interconnect and dielectric thickness prediction
  - Physics-based process model
  - Multi-level and long-range effects – neighboring die and scribe lines
- Multi-foundry support
  - Can calibrate to silicon data
  - Flexible hotspot definition to capture foundry specific weakness
- Meets designers' runtime requirements
  - Scalable and distributed on cheap H/W platform
  - Support hierarchical approach
- Integration into design flow
  - Automated fixing flow based on model-based dummy insertion
  - Interface to extraction tools for CMP-aware interconnect RC extraction



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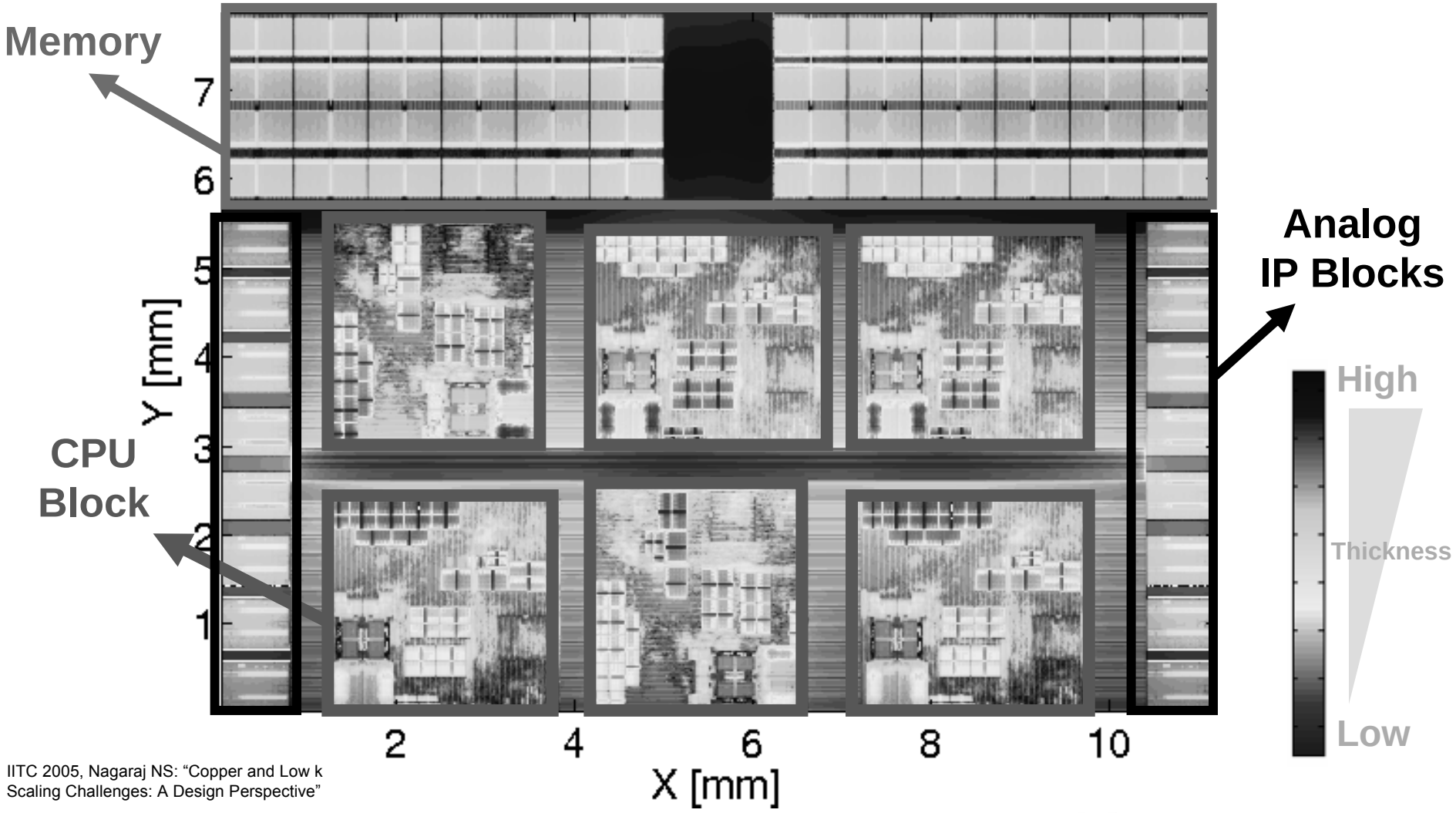
# Impact on Floor Planning

***IP Block Performance Can Have Very Different Cu Loss Depending on Placement***




IITC 2005, Nagaraj NS: "Copper and Low k Scaling Challenges: A Design Perspective"



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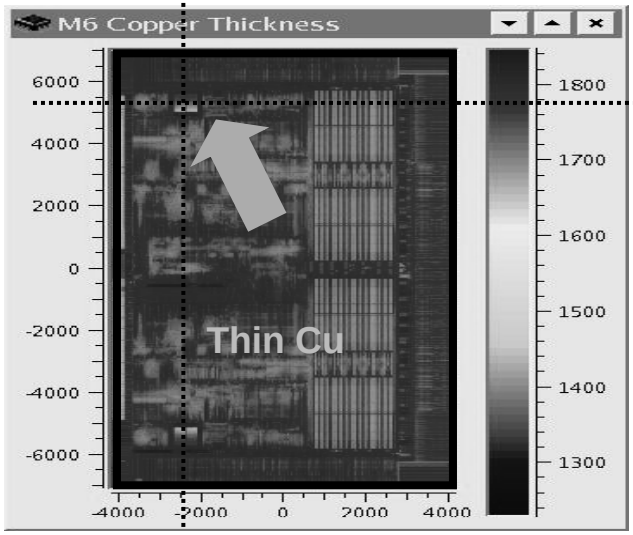
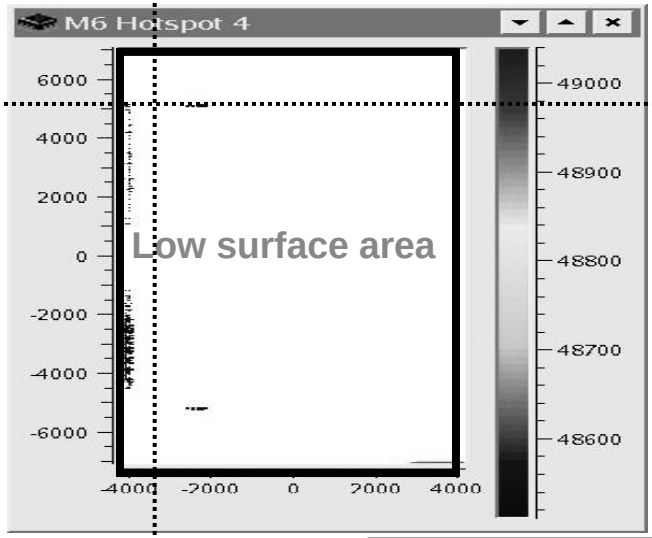
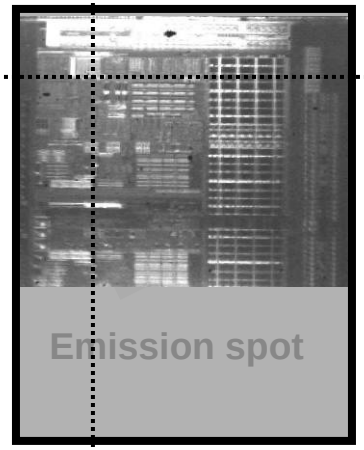
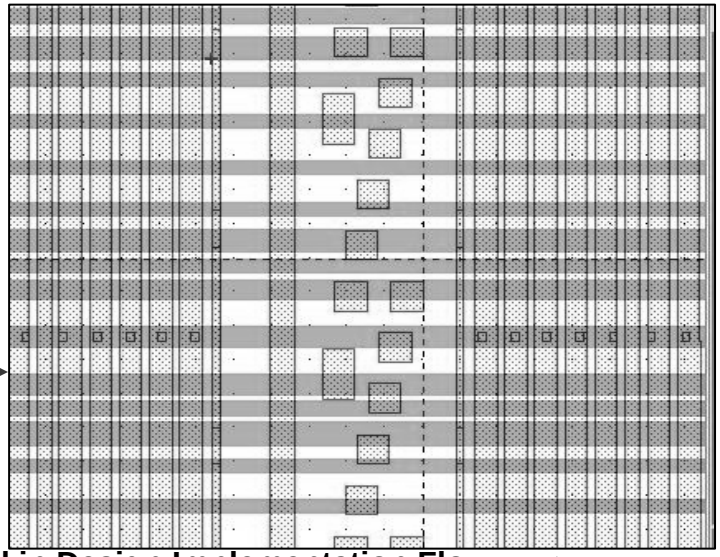
# CMP Hotspot Detection




- **Changed Fill algorithm to allow fill in areas with higher than average density target.**
- **Allow fill at M06 even though area had enough density.**
- **Prevent dishing at M07.**




**Accepted by ISQED, 2008, "Hotspot Prevention Using CMP Model in Design Implementation Flow**

**Norma Rodriguez, Li Song, Shishir Shroff, Kuang Han Chen, Taber Smith, Wilbur Luo**



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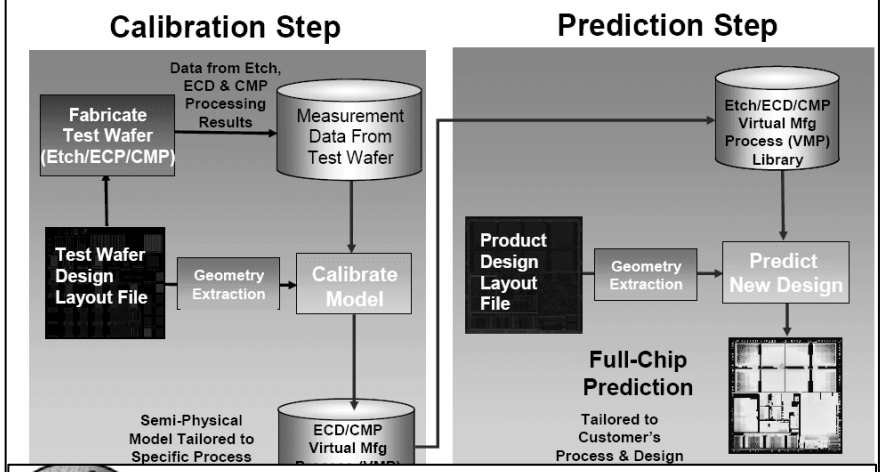
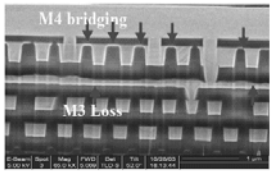
# Hotspot Detection and Design Recommendation Using Silicon Calibrated CMP Model

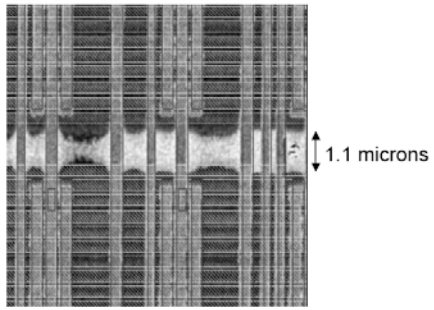
## CMP Modeling Technology - Introduction




## CMP Hotspots Despite of Rule Adherence

- Despite of the adherence to a set of traditional design rules and metal fill …
  *certain layout configurations can be prone to Cu puddling*
  *– wire short or bridging*




Copper puddling after Mx CMP (Mx design shapes are vertical, and Mx – 1 design shapes are horizontal)

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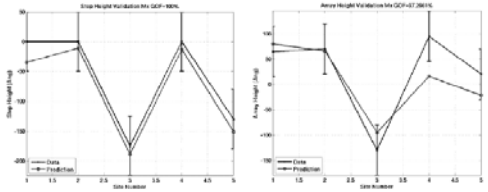
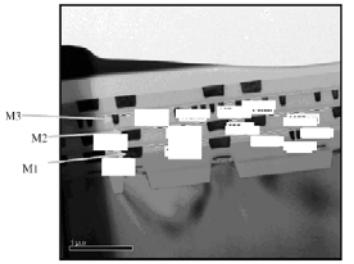
## CMP Modeling Technology – Calibration

- Calibration covers
  - the physical etch process,
  - electrochemical deposition (ECD), and
  - various CMP processes including bulk removal, touchdown and barrier removal



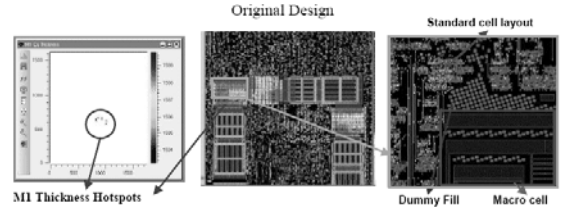
Model parameter fitting during CMP model calibration process

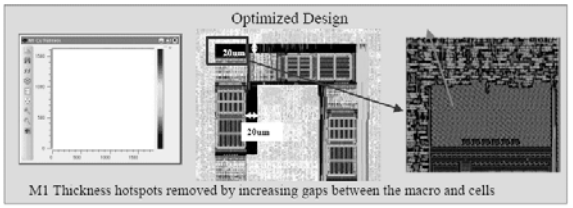



TEM measurement of Chartered 45nm process (where the white boxes were inserted intentionally)

## Design Optimization – Block Placement

- **Block Placement Optimization**




M1 Thickness hotspots removed by increasing gaps between the macro and cells

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# Model-based Intelligent Metal Fill (IMF) Flow on 45nm Design

- Full metal fill flow (rule-based + model based) :
  - Dummy Fill insertion (Rule based Metal-Fill)
  - Model-based CMP analysis
  - Model based Metal-Fill

| | No Fill | | Rule-based | | Model-based | |
|---|---|---|---|---|---|---|
| | Density violation | Hotspots | Density violation | Hotspots | Density violation | Hotspots |
| Results | 260 | 10 | 0 | 8 | None | None |



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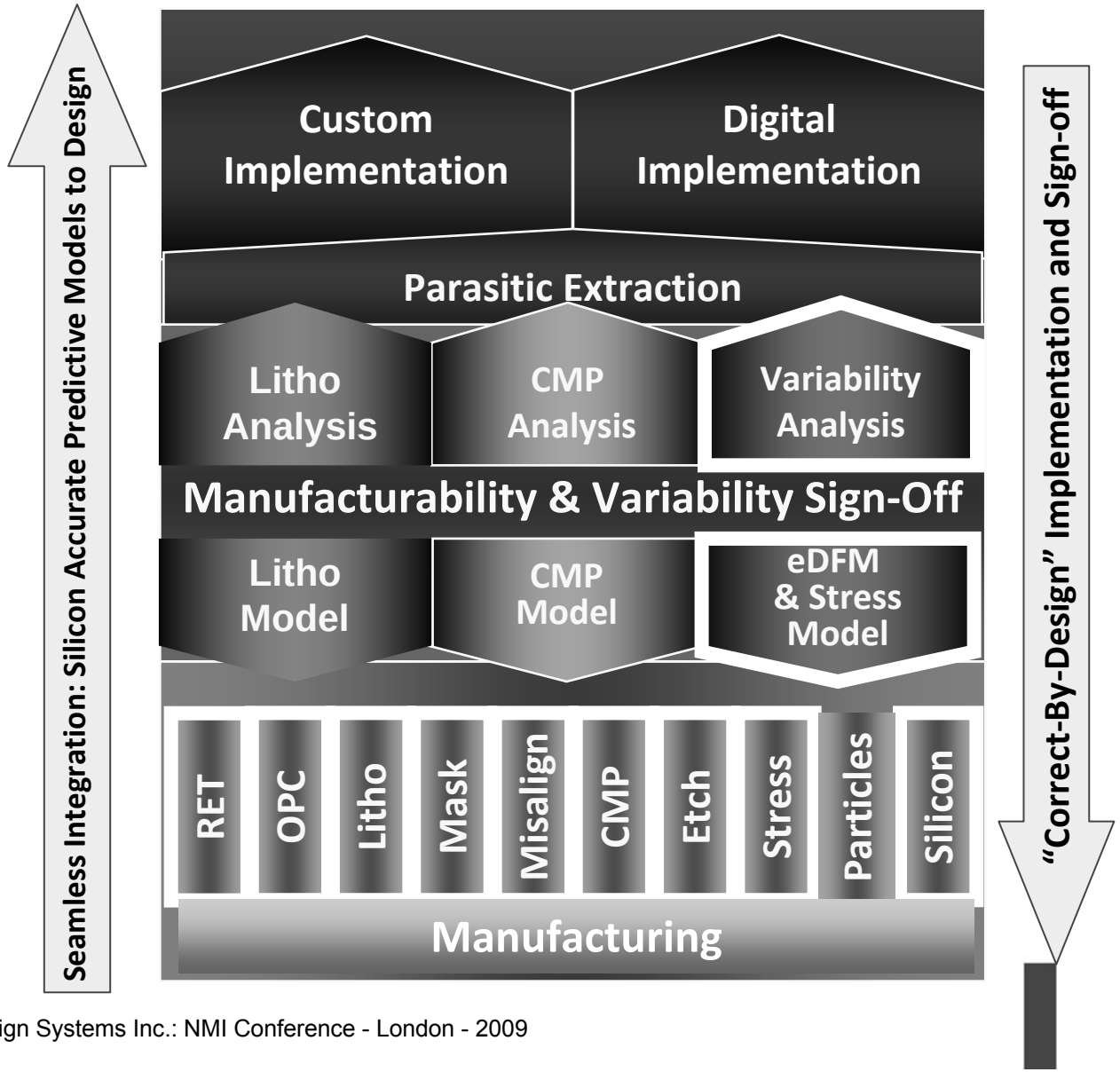
# Enabling “Correct-By-Design” Flow

## Prevention, Analysis, Optimization and Sign-Off



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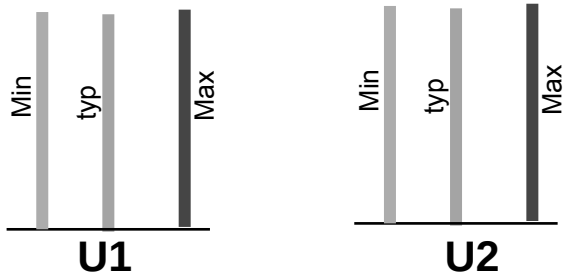
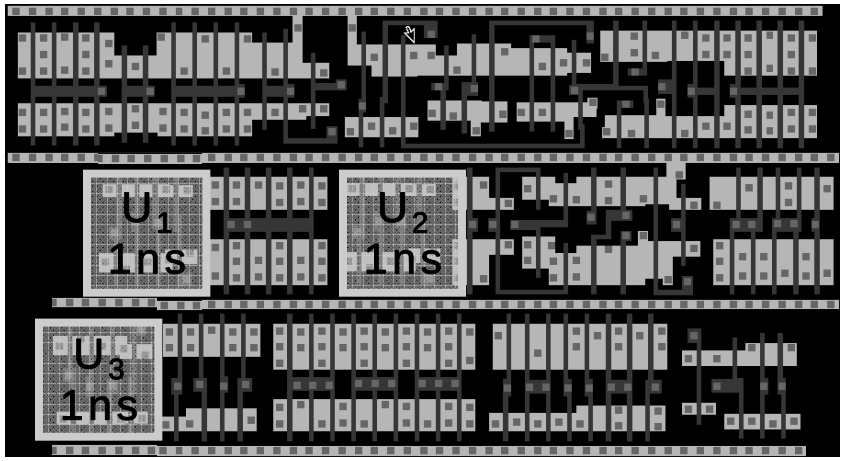
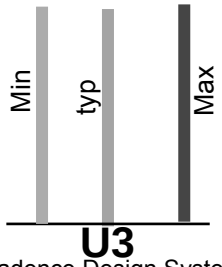
# Traditional Rule & Corner-Based Methodology




With traditional timing analysis




- Margins are applied everywhere regardless of context
- Over margin slow-down timing closure
- Unexpected manufacturing variations yield to parametric failures



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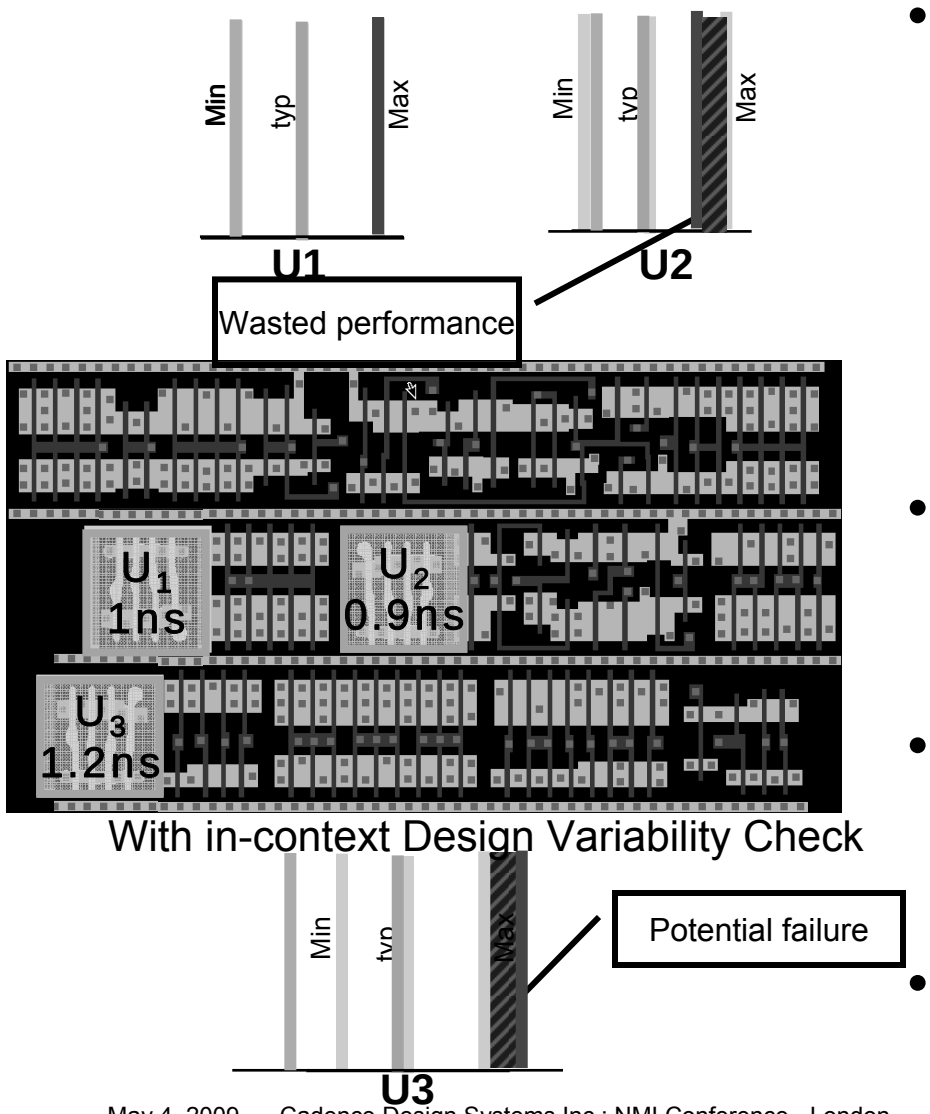
# Model-based In-Context Variability Analysis




- Accurate litho, stress and CMP-aware variation analysis during design
  - In-Context prediction of variations due to litho and stress: $\Delta LW$, $\Delta Vt$, $\Delta Mu$, $\Delta VSat \rightarrow \Delta\tau$
- Reduce margins, over design and performance spread
- Enable faster chips and faster timing closure
- Early detection of potential timing failures



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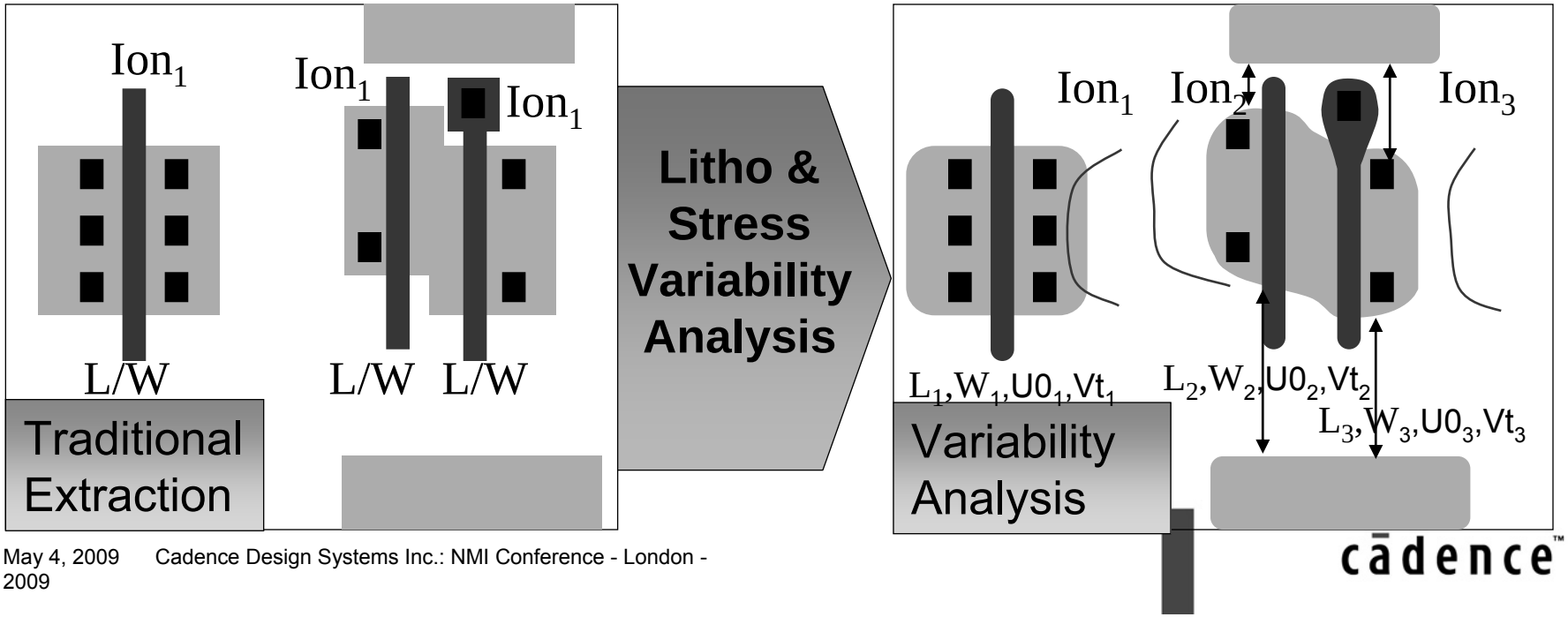
# Variability Analysis Must Capture Layout-Proximity Dependent Litho and Stress Effects

- Litho and stress effects have a proximity effect of 1um or more
- Litho change gate dimension
- Stress change the mobility of carriers in transistors (delay)
- Stress amount depends on
  - LOD (Length of Diffusion) and WPE (Well Proximity Effect)
  - SiGe volume (area of diffusion layer in PMOS)
  - Poly-silicon Pitch (transistor gate pitch)
  - Active layer (diffusion) spacing
  - Contact effects
  - DSL (Dual Stress Liner)

**Context dependent**





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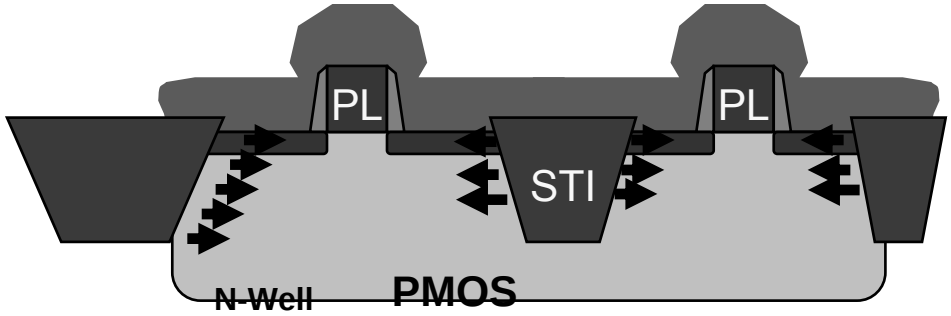
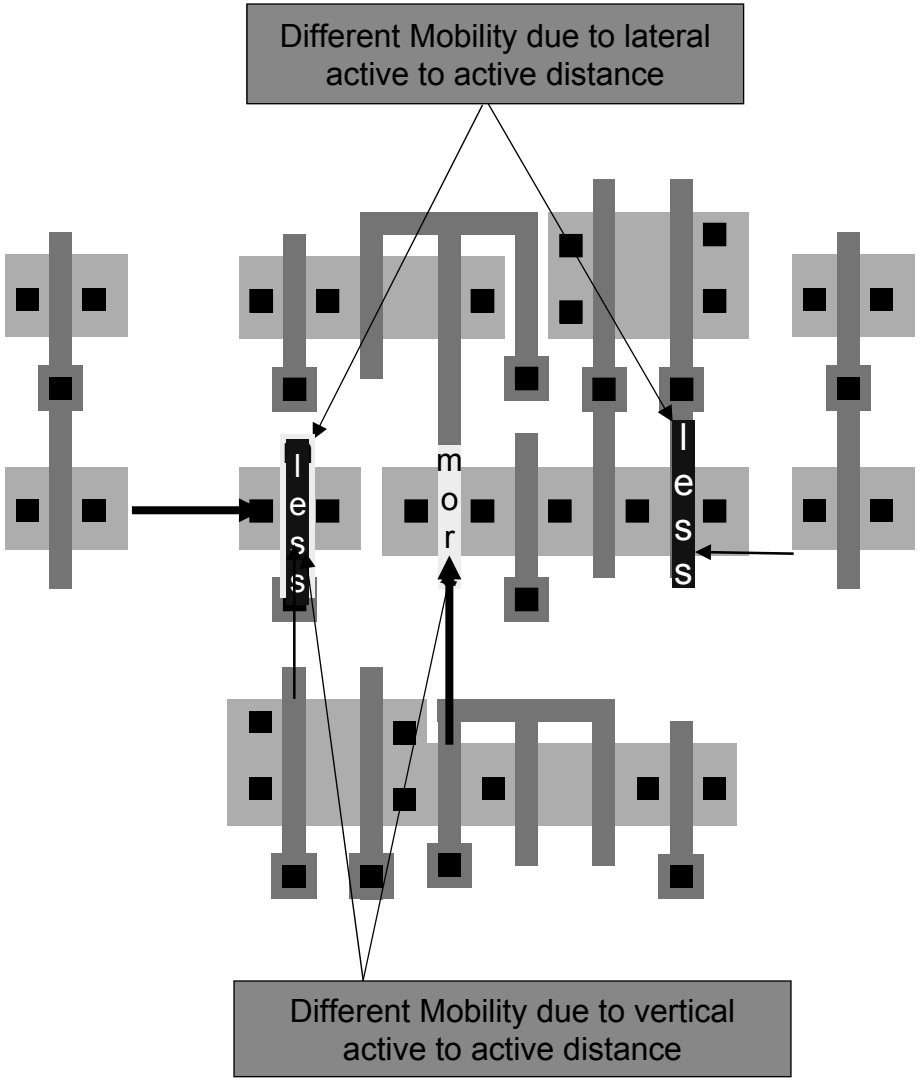
# STI/Active-to-Active Spacing




- When the wafer cools down after processing the STI usually becomes compressive due to the thermal expansion mismatch between Si & SiO2 (The stress of STI is SiO2 fill recipe dependent though)
- The wider the STI the higher the compressive stress
- Hence the width of STI (Active to Active Spacing) plays a strong role in determining the stress in the channel region
- Context dependent



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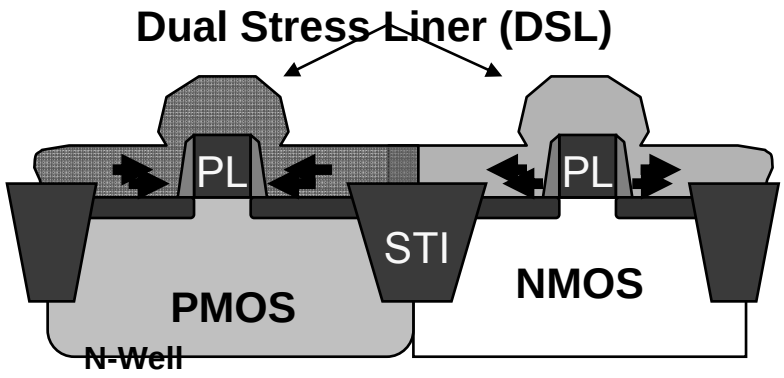
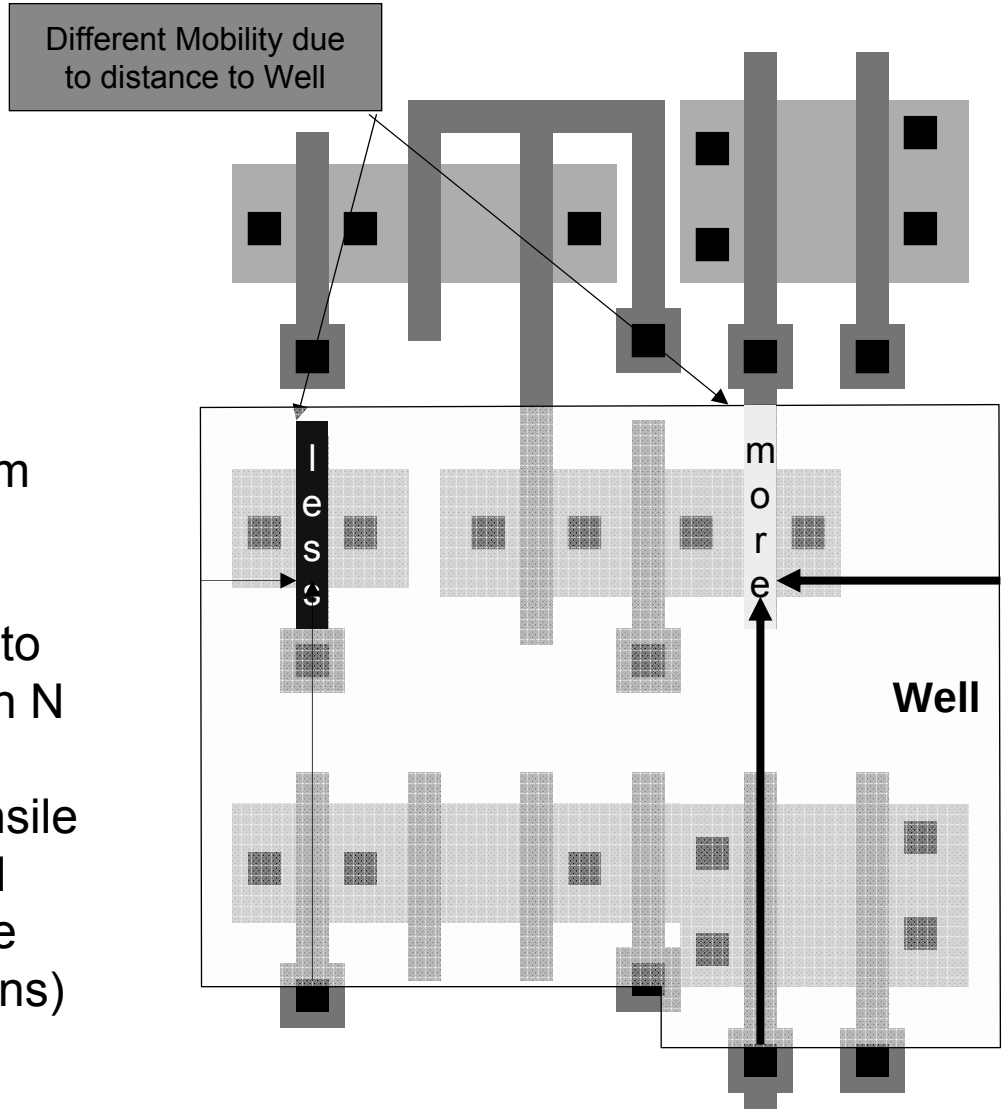
# Dual Stress Liner/Well Boundary Stress Effect




- Dual stress liner is usually a SiN film that is deposited after Salicidation
- This liner is intentionally deposited to be compressive on P and tensile on N
- The boundaries of compressive/tensile is usually synthesized from the well layer (Therefore, the distance to the well boundary has stress implications)
- Context dependent



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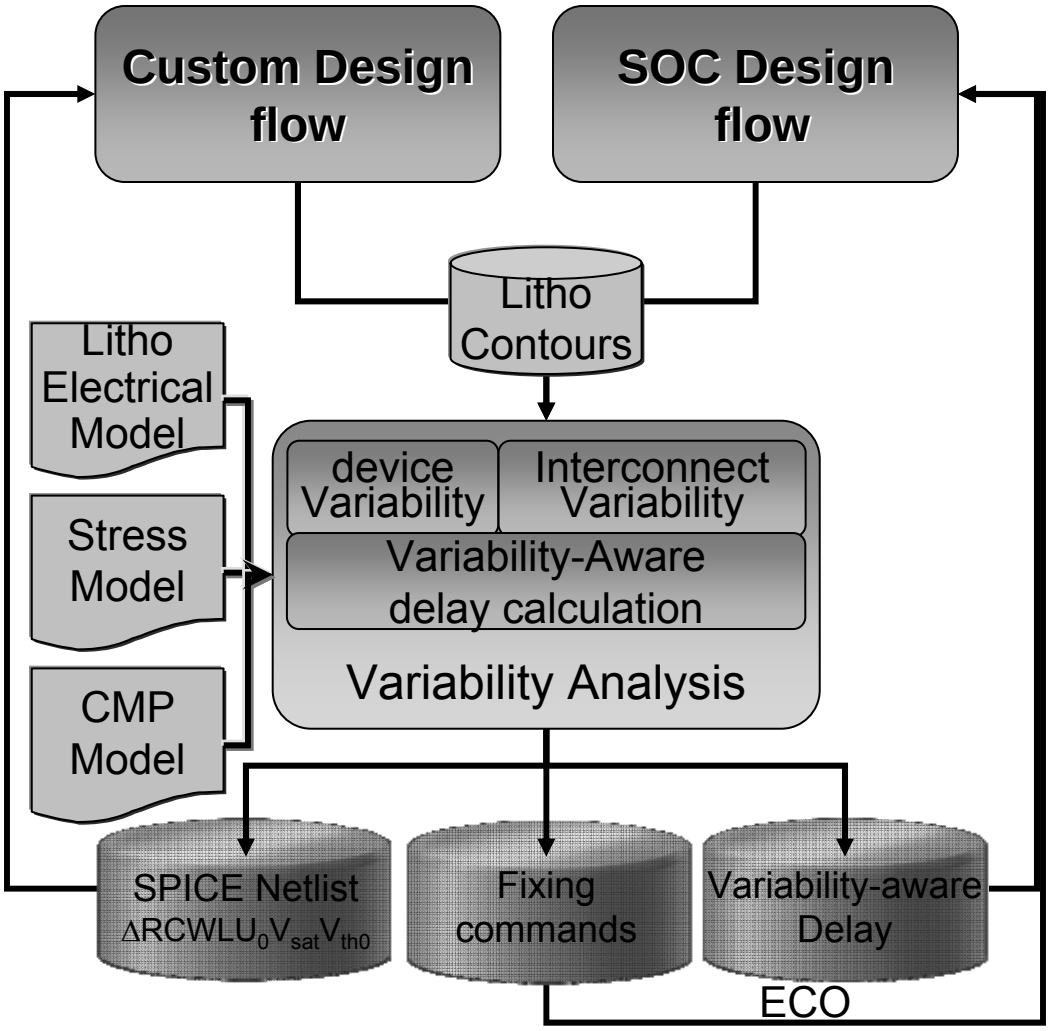
# Variability Analysis Requirements

- Accurate variability prediction
  - Physics-based models anchored in silicon
  - Litho, stress and CMP combined effects
  - Predicts variation on device and interconnect
- Multi-foundry support
  - Can calibrate to silicon data or existing proxy models
- Provide comprehensive value to designers
  - Integrated into library, custom, and chip design flows
  - Enable prevention, detection and fixing
  - Reduce design margins and improve parametric yield and chip performance



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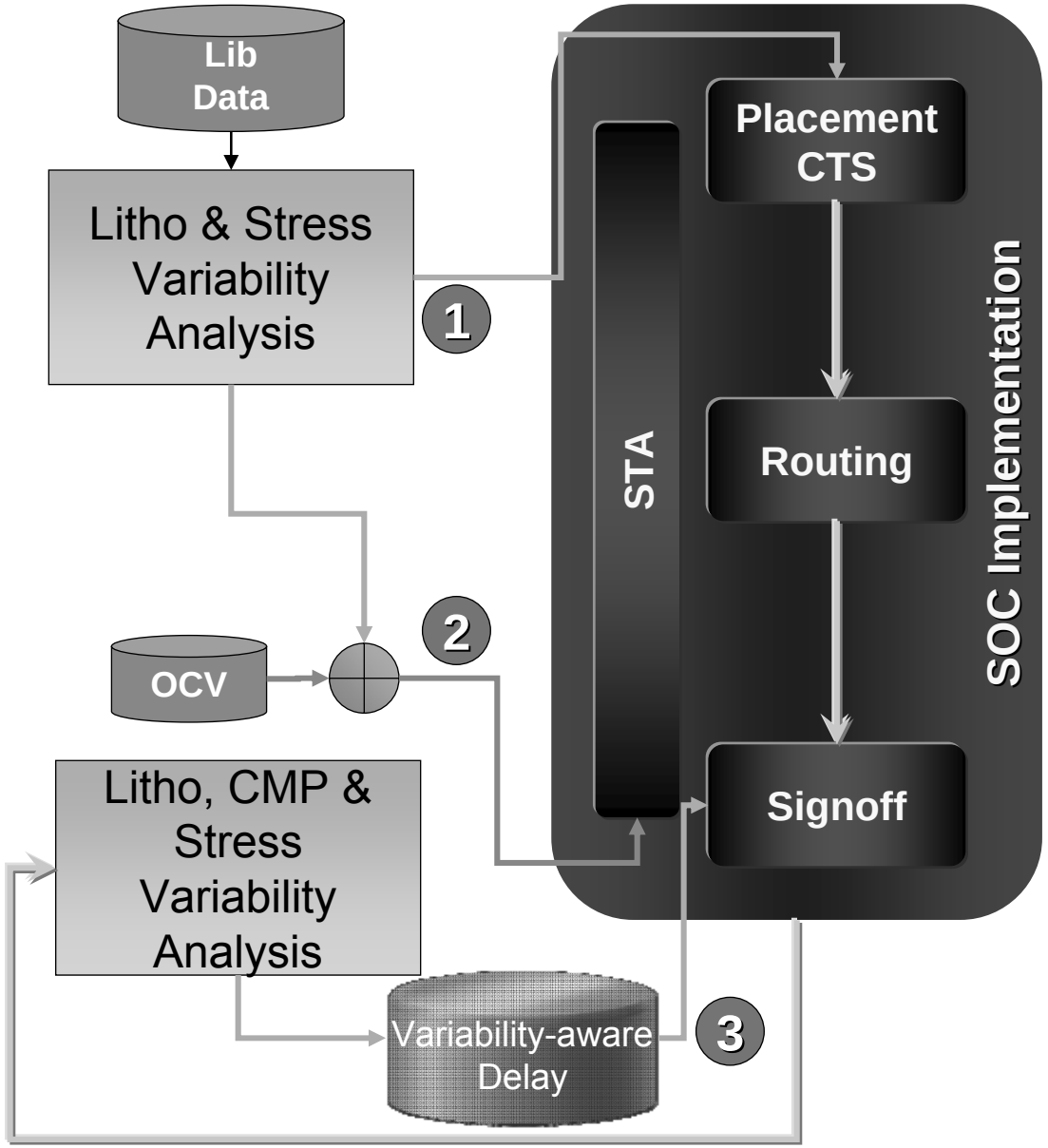
# Variability-Aware Implementation




1. **Drive placement to reduce sensitivity to litho and stress variations on critical paths**

2. **Accelerate timing closure and reduce over-design**
   - Reduce OCV using systematic variation analysis

3. **Accurate context-based litho, stress and CMP timing analysis and optimization**
   - Context-analysis of critical paths during block/chip implementation
   - Optimization of critical path to reduce sensitivity to variations



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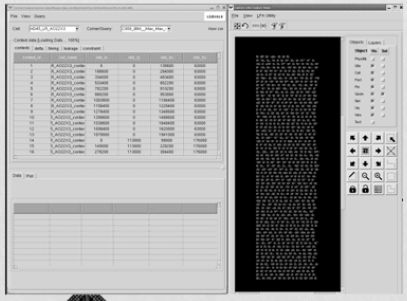
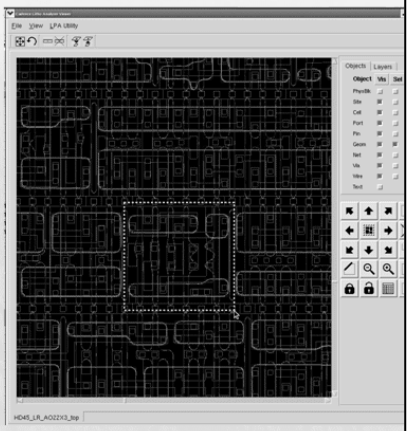
# Layout Electrical Co-optimization

## Analysis Done Across Multiple Contexts

- Analysis was performed with up to 800 random contexts created by LEA





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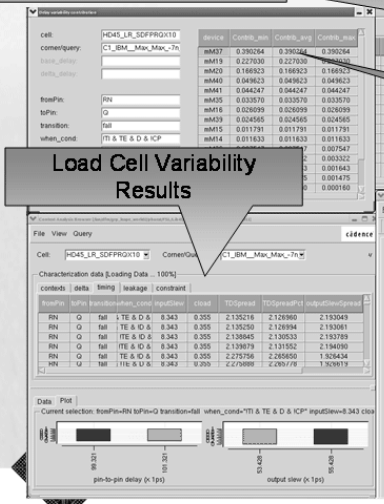
## Identifying Outliers in LEA Data

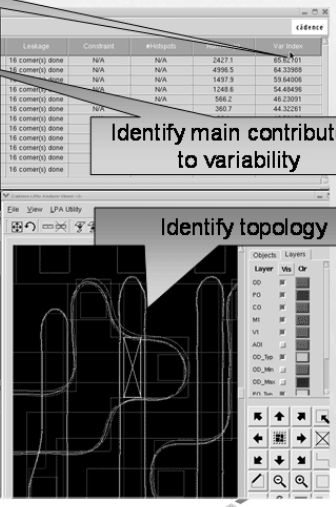
Sort by Variability Index

Identify main contributors to variability

Load Cell Variability Results

Identify topology





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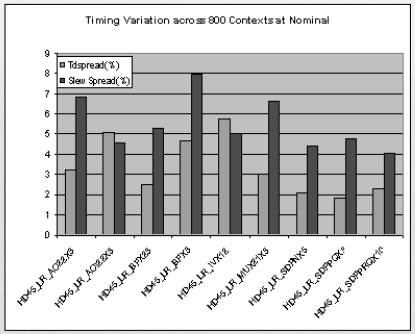
## Delay and Slew variations on 800 contexts – Contours to Contours

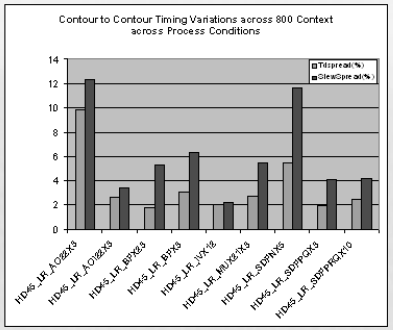
Typical




SPICE TT; VDD 1v; Temp 105C
Shape OD: Typ PO: Typ; Misalignment X=0 Y=0

Up to 5.7% delay and 8% slew variation due to context at Nominal

Across Process Window




SPICE TT; VDD 1v; Temp 105C
Shape OD: Max PO: Max
Misalignment X=-7nm Y =+7nm

Up to 10% delay and 12% slew variation at some process conditions across contexts

Slide 37

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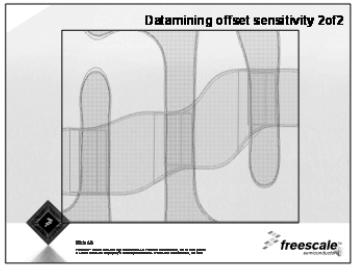
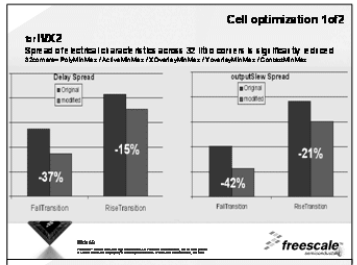
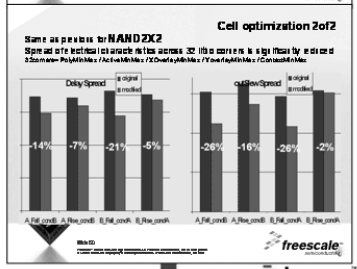
## Freescale Leverages LEA to Reduce Variability

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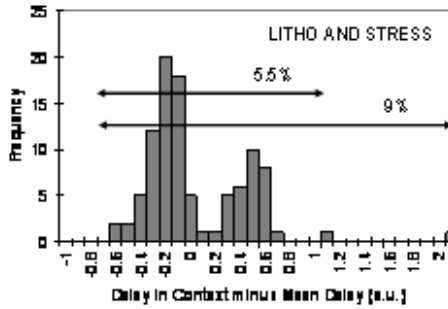
# Lithography and Stress Induced Systematic Variations in 45nm Designs

**CDNLive 2008– SPIE 2009**

## Variations due to Litho and Stress

- **Context dependent variation in cell delay for a small NAND2 cell (fall transition, moderate input slew and load, nominal spice corner, 100 random contexts).**




- **The isolated context is slower than all dense contexts.**
- **The structure of context dependence reflects details of the process.**
- **Several percent variation is seen in this case.**

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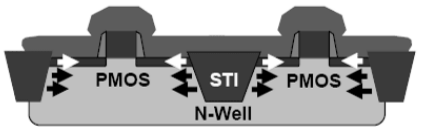
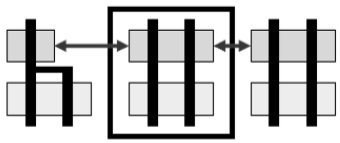
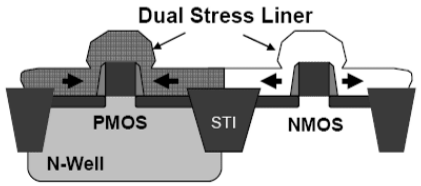
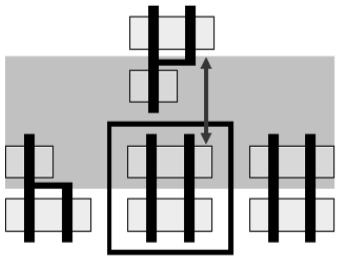
## Motivation

- Recent processes employ stress to improve transistors.
- Stress effects may result in context dependence at the cell level.





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## Overview of Variations

- For each source of variation, a library may show worst-case transitions (*) with a few to several percent variation. Worst-transition variations values seen for each source alone include

| | |
|---|---|
| Shape effects | 6.5 % |
| Overlay error in X & Y | 9.5 % |
| Poly defocus | 4 % |
| Active defocus | 8 % |
| Context dependence (including stress) | 7 % |

**Latest stress variability results shows up to 18% variations**

- Worst-case transitions for different sources are not the same cell/transition.
- Combining all source of variation should involve awareness of
  - different yield impacts of each source
  - whether or not (and which components of) each source are included in the spice model

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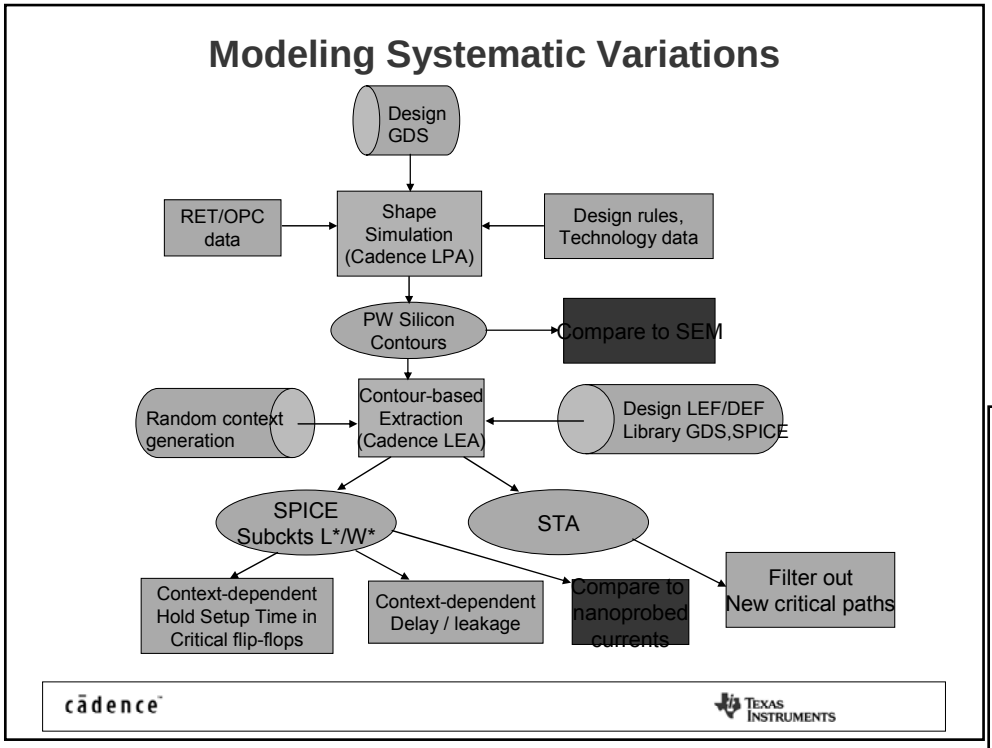
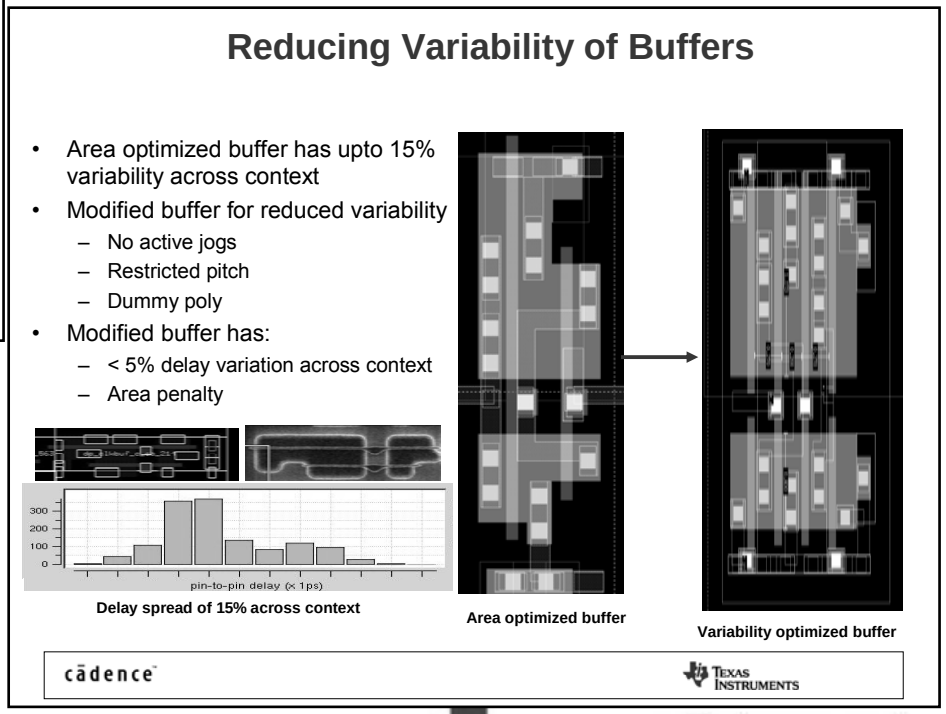
# Context analysis of lithography induced systematic variations in 65nm designs




- Robust design enabled by context variability analysis
- Analysis of variability in the design flow enabled at
  - Library design and characterization: PPAV tradeoff
  - Chip Level: Fix outliers for design robustness and margin




*"Context analysis and validation of lithography induced systematic variations in 65nm designs"*

SPIE 2008 - TI - Cadence



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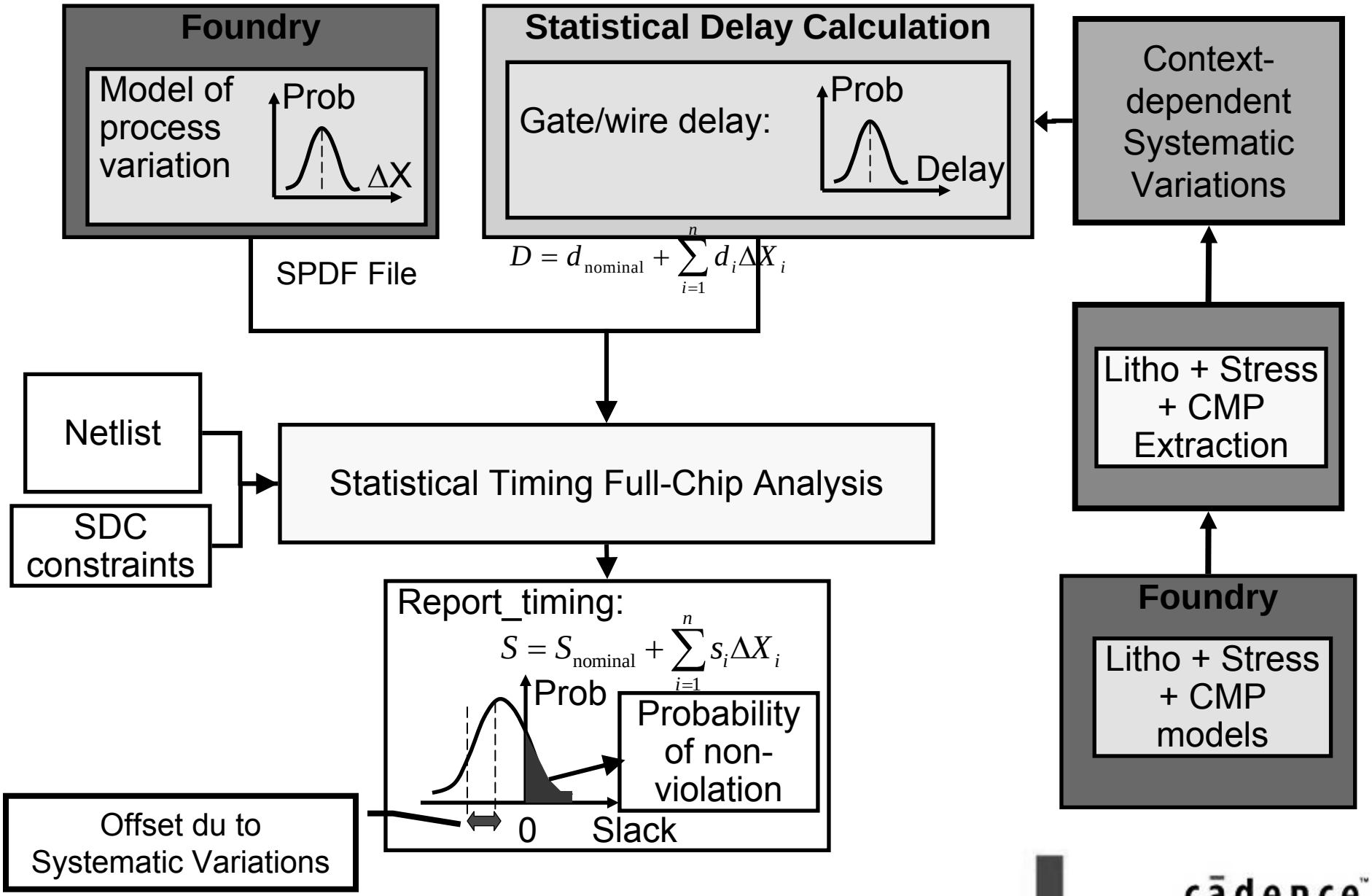
# Combining Systematic and Random Variations



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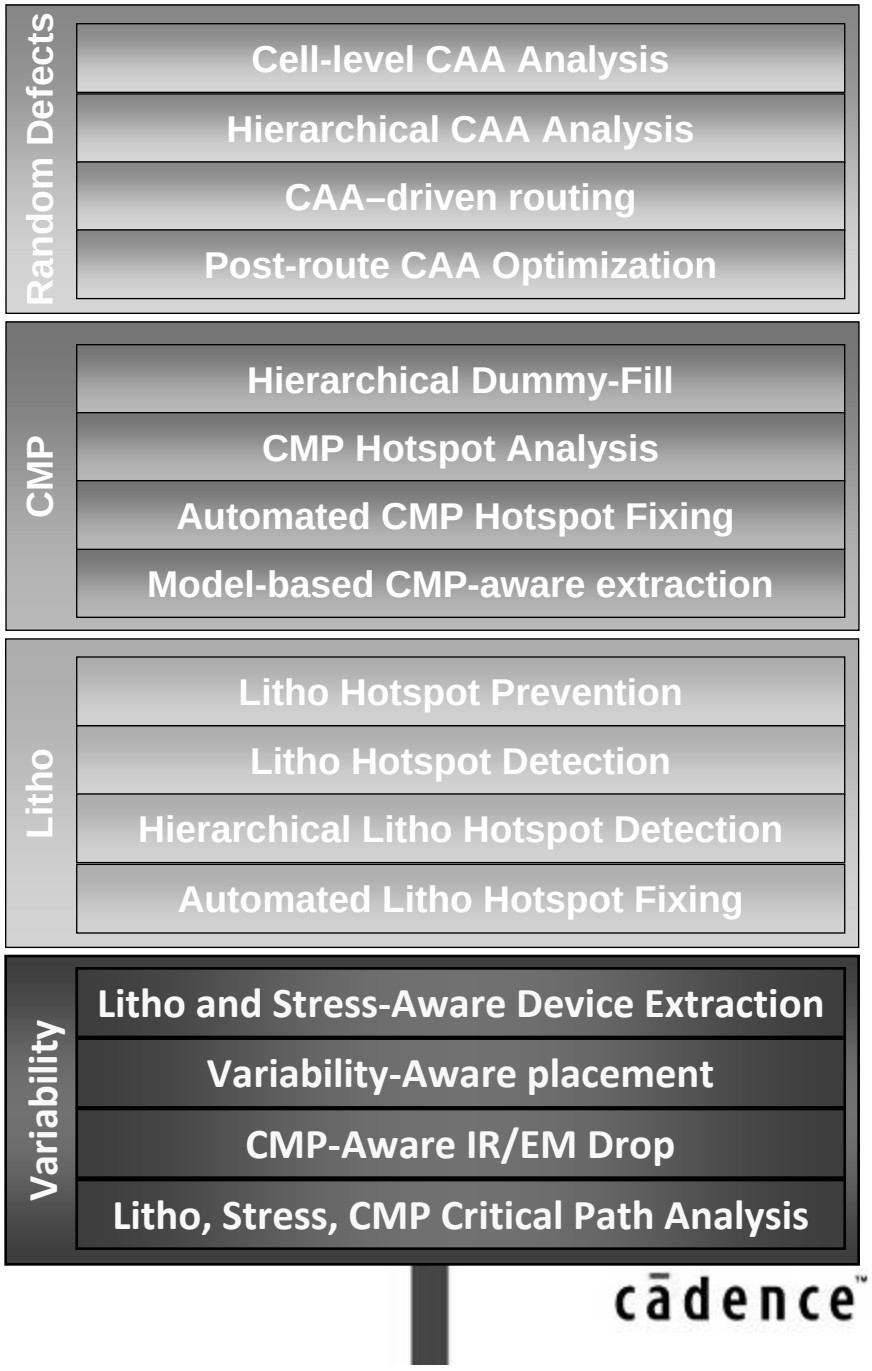
# Typical DFM Flow

- Comprehensive DFM solution should cover all types of:
  - Manufacturing effects
    - Random
    - Litho
    - Stress
    - CMP
  - Design steps
    - Prevention during implementation
    - Detection during sign-off
    - Correction (fixing) with automated solutions
  - Design components
    - Interconnect
    - Devices (Transistors)
  - Design style
    - Custom layout
    - Standard cells
    - Hierarchical SOC



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# Manufacturability and Variability Design Sign-Off Applications

<table>
<tr><th></th><th>Manufacturing-Aware Design</th><th>Variability-Aware Design</th></tr>
<tr><td rowspan="3">Custom & Analog Designs</td><td rowspan="2">Litho hotspot detection & correction of standard cell libraries & custom analog layouts</td><td>Litho & stress-aware timing analysis of custom layouts</td></tr>
<tr><td>Litho & stress-aware timing analysis of standard cell libraries</td></tr>
<tr><td colspan="2">Variability (litho and stress) hotspots detection</td></tr>
<tr><td rowspan="3">Cell-Based SOC Digital Designs</td><td rowspan="3">Litho & CMP Hotspot Detection and automated single-pass Fixing</td><td>Variability-Aware Placement</td></tr>
<tr><td>Reduced-margin Timing Analysis</td></tr>
<tr><td>Variability-Aware (Litho + Stress + CMP) Timing Analysis</td></tr>
</table>



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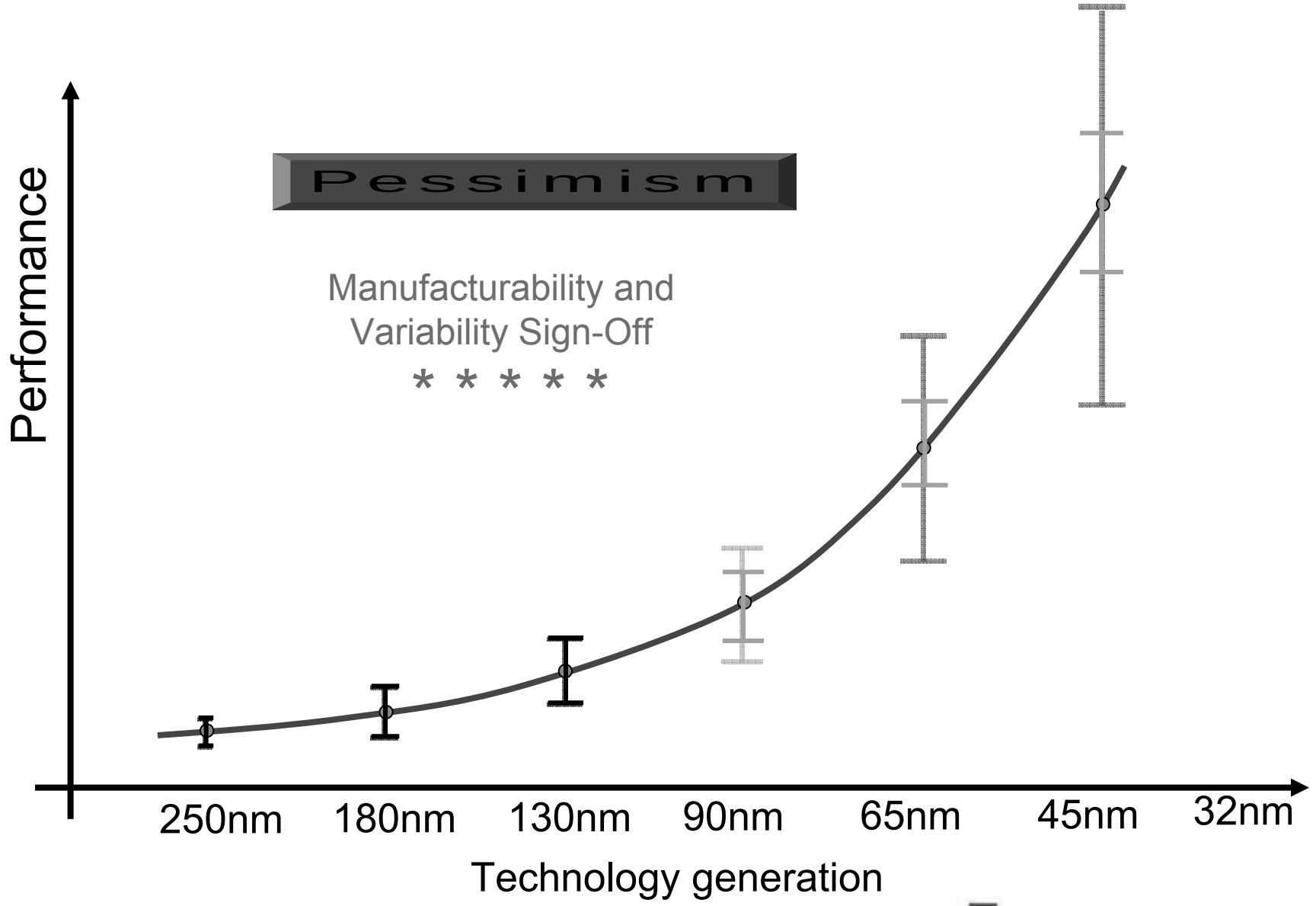
# Master the Variability Challenge



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# Summary

- Manufacturability and variability solutions must be deployed:
  - For litho, stress, CMP effects
  - On custom, library and SOC design flows
  - To cover physical and electrical variations
  - At the prevention detection and fixing stage of the design
- These solutions enables design teams to
  - Account for the growing manufacturability and variability effects
  - Quantify variability and reduce its impact on designs
  - Reduce failures, margins and over design

**Variability is here to Stay!**
**Deal with it!**



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