SYNOPSYS®
Predictable Success

Designing Chips in the Era of Increasing Variability

ICCV 2009, London

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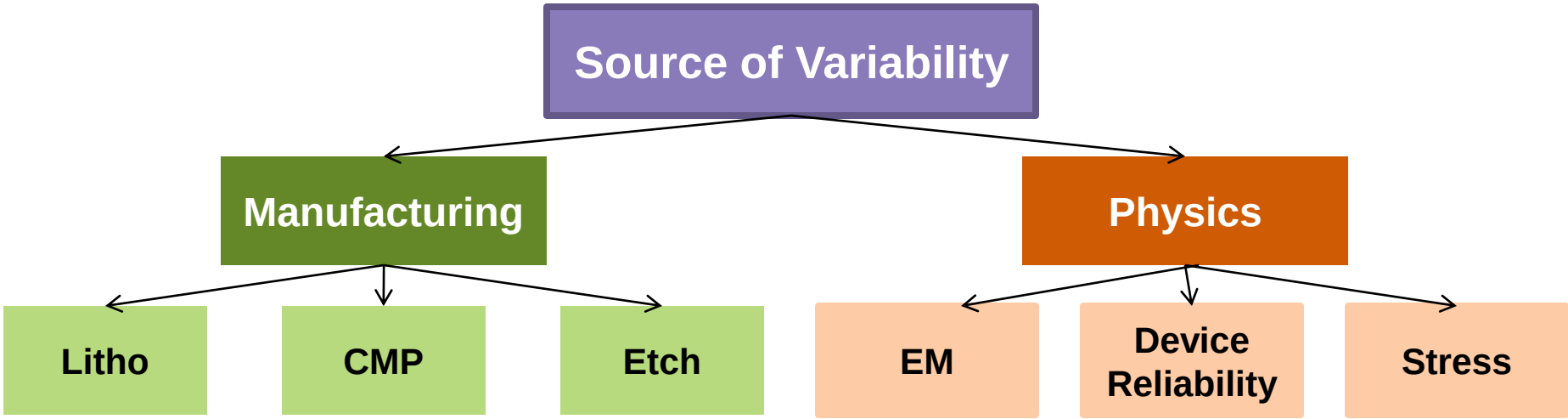
Scaling and Variability

Source: ITRS 2005	**90nm**	**65nm**	**45nm**
ASIC (Gates/mm^2)	500K	1M	2M
Equivalent T_{ox} (# of SiO_2 Molecules)	4 - 5	3 - 4	2 - 3
V_{DD} Variability (%)	10%	10%	10%
V_{TH} Variability (%)	20%	30%	40%
Timing Variability (Performance) (%)	40%	45%	50%
Power Variability (%)	50%	55%	60%

Source: ITRS 2007	65nm	45nm	**32nm**
Moore's Law (Integration Capacity)	1X	2X	**4X**
Equivalent T_{ox} (# of SiO_2 Molecules)	3 – 4	~ 2	**< 2**
Timing Variability (Performance) (%)	45%	50%	**60%**
Power Variability (%)	55%	> 65%	**80%**
Manufacturing Cost (microcents/Tx)	1X	0.82X	**0.9X**

Sources of Variability



- Depth of Focus
- Misalignment effects
- CD control
- Break, Thinning, Bridging, etc…
- Forbidden pitches
- Scanner effects (XY difference)
- Field/aberration effects

- ILD Thickness variations
- Dishing
- Over polishing

- Gate damage due to antenna effect
- Profile control
- CD control

- Interconnect and via failure due tp current density
- Jogs on high drive nets

- Hot carriers
- ESD
- NBTI (Negative Bias Threshold Instability)
- Gate Oxide Integrity

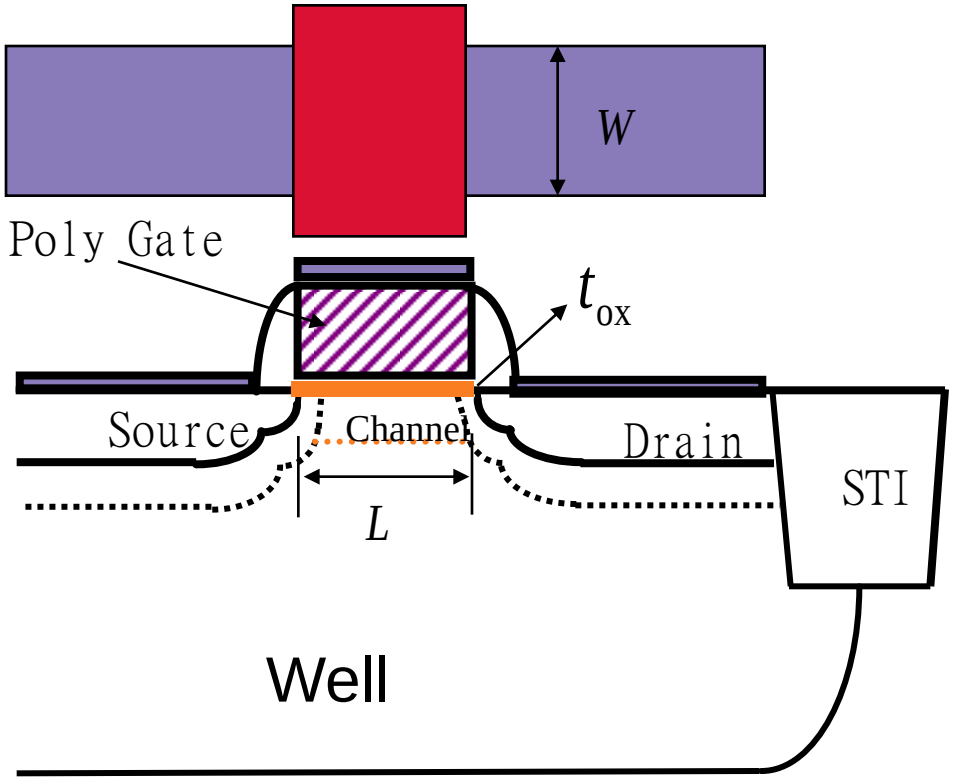
- Via failure
- Line failure
- Dielectric delamination
- Length of Diffusion (LOD) effects

Taxonomy of Variation

- **Process (static) vs. Operational (dynamic)**
  - Process: due to optical, physical and chemical effects
  - Operational: IR drop, temperature (ambient or within-die)
  - Aging: EM, Vth shift (becoming important and significant)
- **Random vs. Systematic**
  - Random: Number and location of dopant atoms in channel
  - Systematic: Optical, physical, chemical effects, IR drop
- **Correlated vs. Uncorrelated**
  - Spatial, topological, derived parameters
  - Width and spacing, Metal thickness and ILD thickness
- **Within die (Intradie) vs. die-to-die (interdie)**

Device Parameter Variations

- W, L variations
  - Due to photolithography proximity effect or etching
  - Layout density dependent
  - Location dependent
- Tox variation
  - Well controlled by a product spec.
- Vth variation
  - Due to doping
  - aging
  - Getting worse @ every node
- μ(n,p) variation
  - Layout proximity dependent
  - 3-D effects
  - Short channel effects
  - Stress engineering
  - orientation



Impact of Variation

IC Implementation Perspective

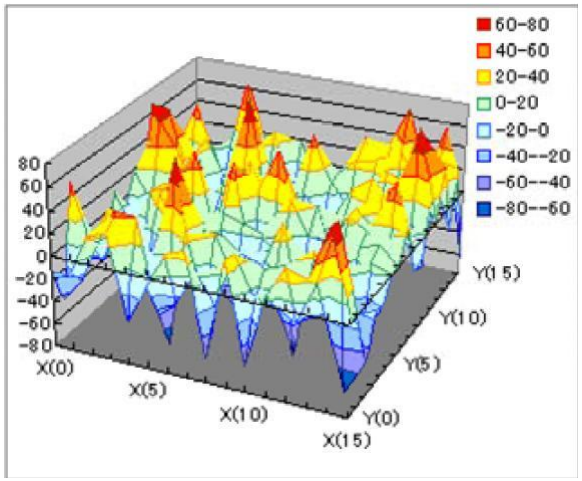
- **Higher margins impacts Quality-of-Results (QoR)**
  - **Over-engineering impacts QoR -- tradeoffs in larger area or power**
- **Robustness across expected range of variation**
  - **Some cells/nets/paths too susceptible to variations**
    → Impacts Parametric Yield
- **Cost and Productivity: TTR**
  - **More resources & time needed to analyze more corners / manage over-engineering**

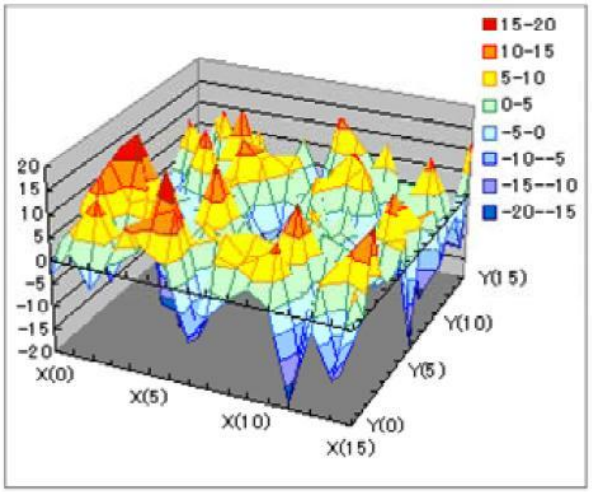
Coping With Variability

- Measure, analyze, divide and conquer
  - Understand and categorize source and impact
  - Identify an economical, reliable and sustainable solution
  - Solution space (and the cost) varies
    - Process engineering
    - Lithography techniques
    - Layout design / DFM techniques
    - Circuit design techniques
    - …
- Tool and techniques to analyze and validate
  - Tools to analyze and provide solution
  - Tools for IC designer

Intra-die Vth & Ion variability

- Spatial intra-die variability has a clear systematic component to it



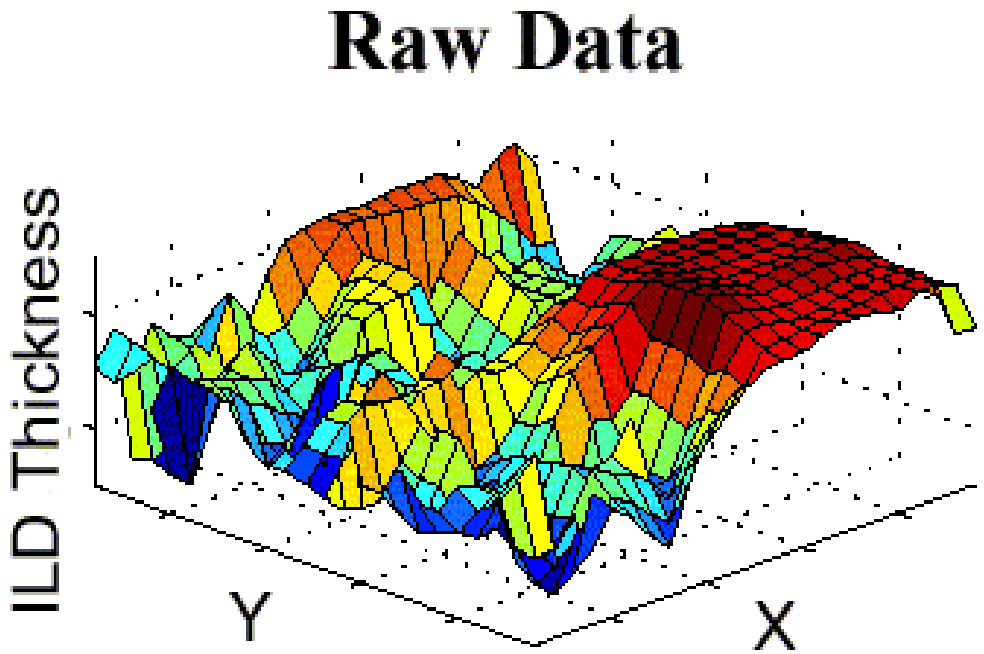


- Ion, with multi-variable dependency has a less-clear spatial systematic component and a rather large random variability

Source: Masuda et al, CICC 2005

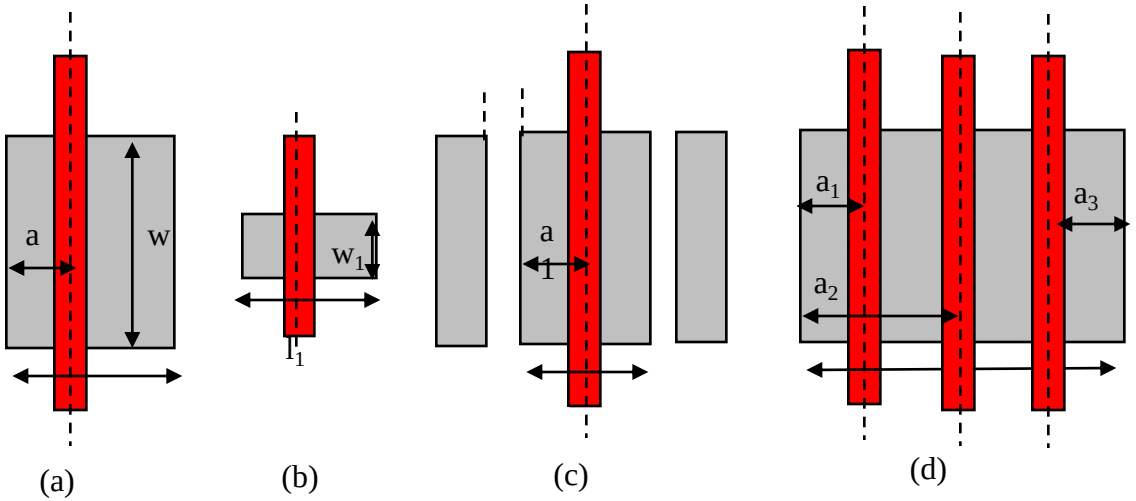
Intra-Chip ILD Thickness Variation

- Differences in wiring density within chip can cause variation of up to 20%
- Most of ILD thickness variation is systematic – can be corrected
  - Smart model based dummy fills
- The rest is ‘random’



Spanos & Poolla, UCB

Effect of layout (stress related)



TCAD tools capable of simulating these effects

a. Transistor drive current dependent on distance from edge and on poly to poly spacing)

b. 3D leads to further reduction in performance

c. Performance is altered by adjoining diffusion islands

d. Different drive current for identical transistors sharing same active area

e. Transistor orientation alters the characteristics of the device

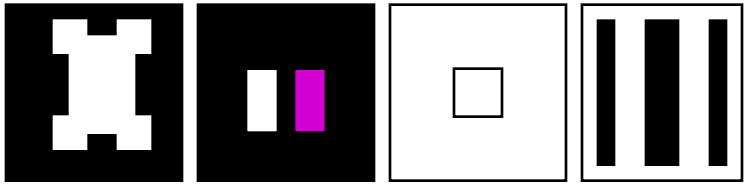
RETs in Optical Lithography

Light Source
248nm, 193nm, 157nm,...

Illumination
OAI, custom

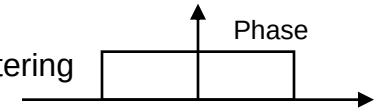
Quadrapole Annular Conventional

Mask
OPC, PSM



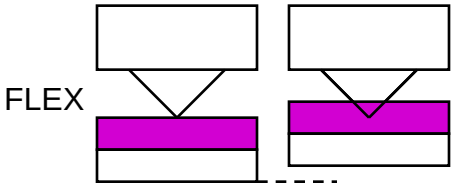
OPC (serif, bias) Alternating PSM Attenuated PSM OPC using Assist Features (SRAF)

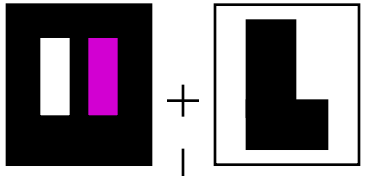
Pupil Filtering



Pupil Filtering

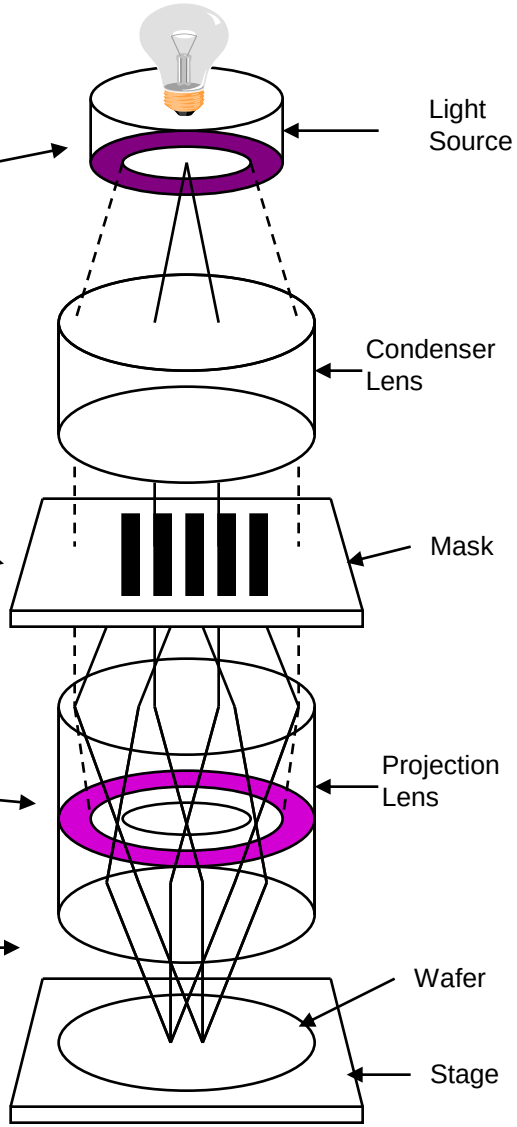
Multiple Exposure
Flex, PSM+BIN,...





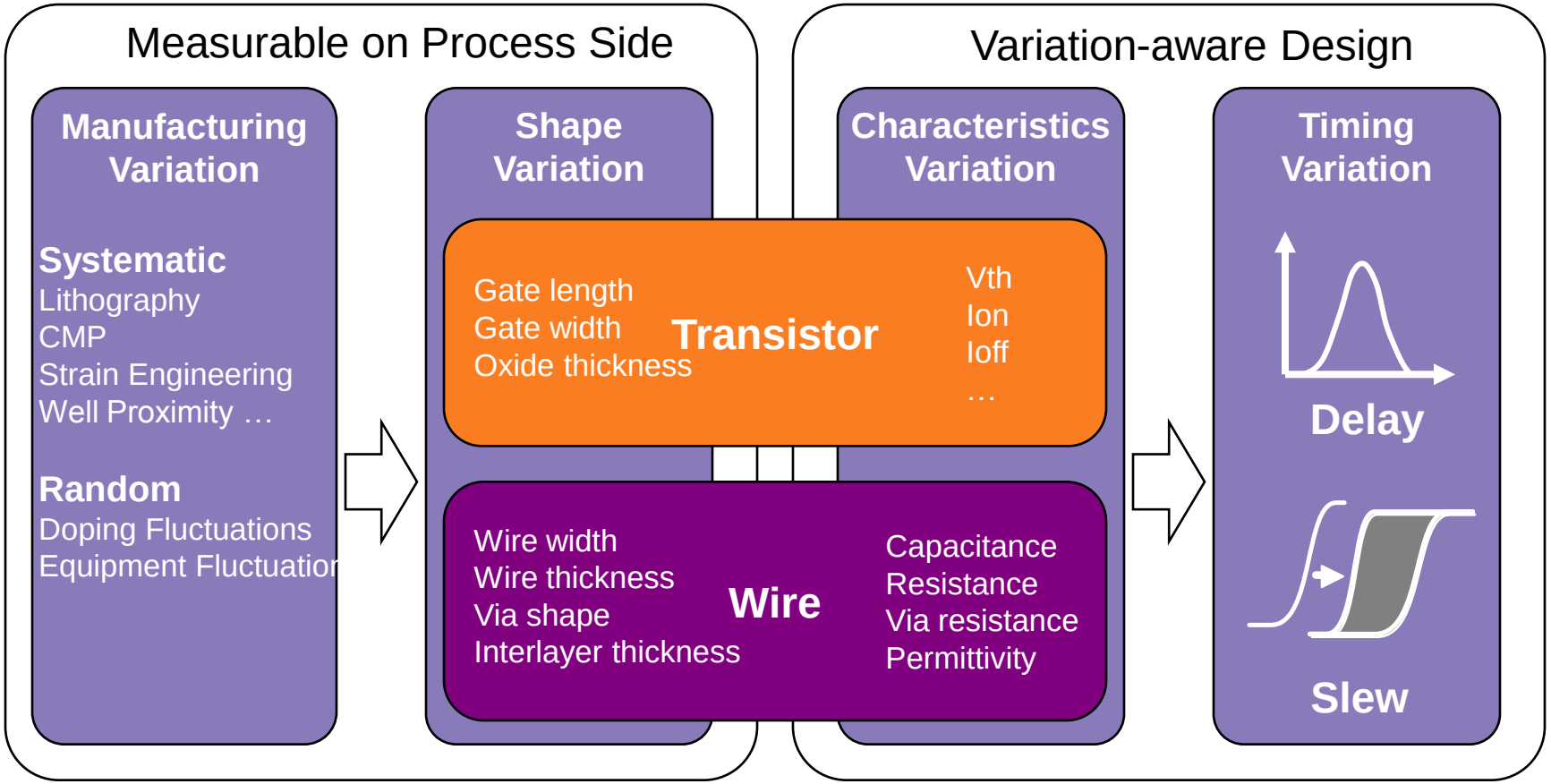
Resist and Process
TSI, TLI,...

Resist Processing: TSI (top surface imaging)
TLI (thin resist imaging)



Source: Chiang, Kawa 2007

Modeling Variation



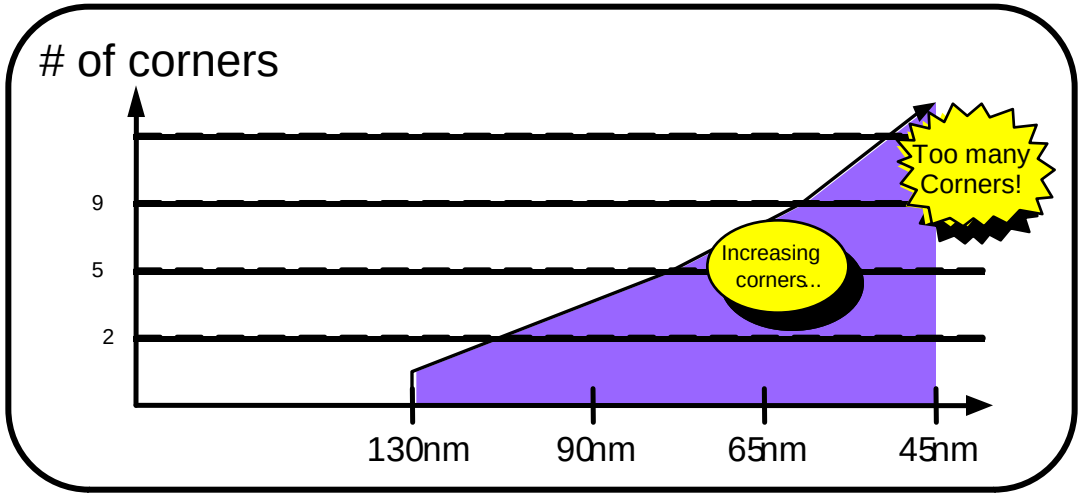
IC Implementation Perspective

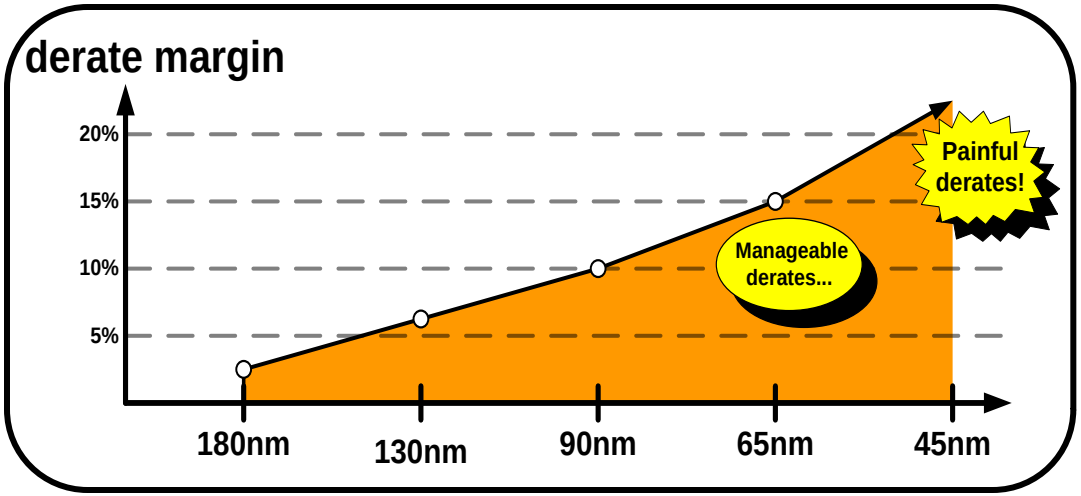
- New methodology and tools (with supporting ecosystem) to deal with variability
  - A new generation of analysis (and design) tools using statistical techniques
- Good news: technologies, tools, and methodologies are available and they are becoming more mature
  - Variation-aware timing models
  - Characterization tools and techniques
  - Sensitivity-based parasitic extraction
  - Variation-aware / statistical timing analyzer

Today's Methods for Modeling Non-Systematic

Corner analyses:

Increasing numbers of corners are defined to ensure coverage := too many runs



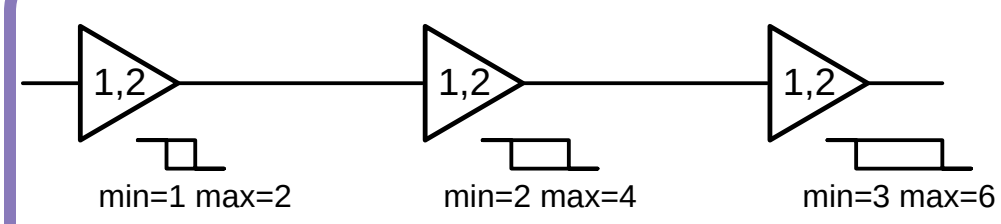


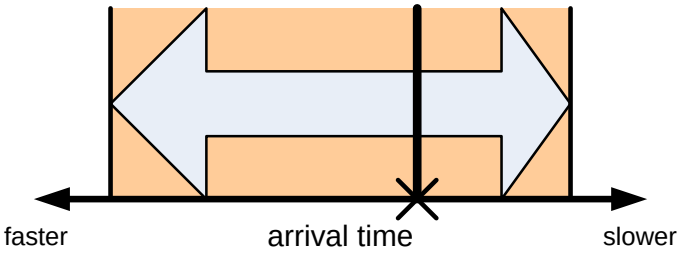
Timing Derate:

Margins are becoming excessive to ensure worst case coverage := overdesign

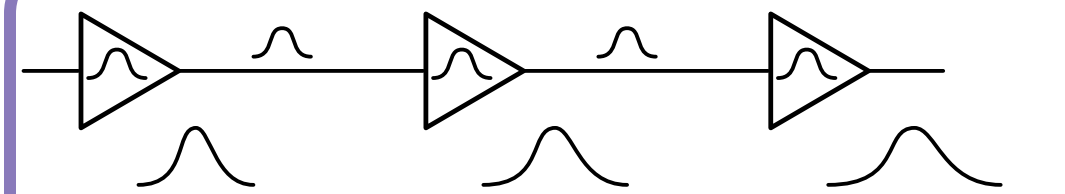
Timing Analysis: Bounded vs. Statistical

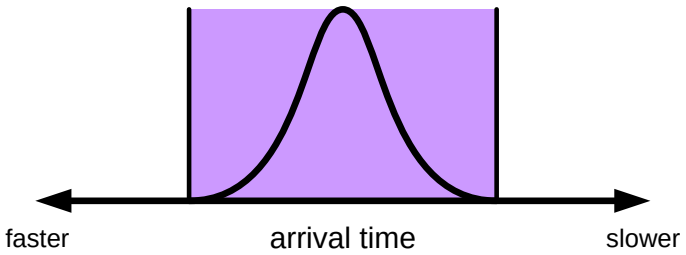
- Traditional corner-based STA bounds the timing
  - computes worst-case (improbable but safe) bounds



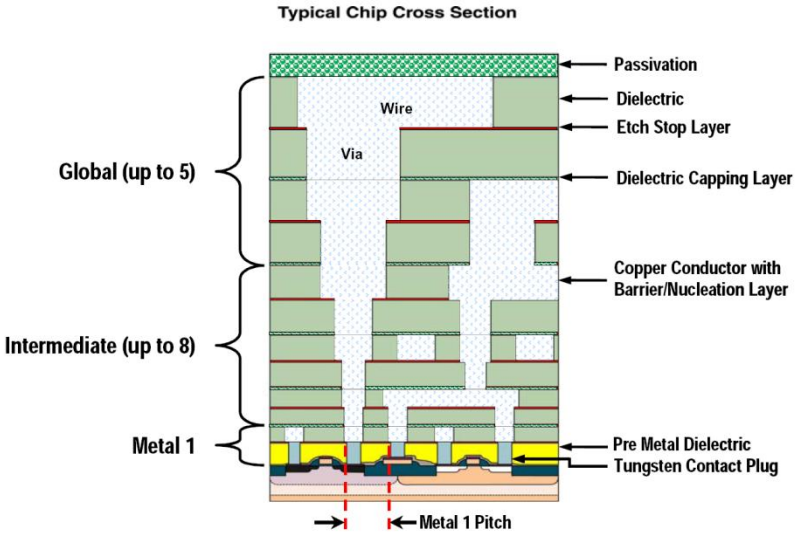


- Variation STA models the variation sources statistically
  - computes probable distribution of slews/arrivals

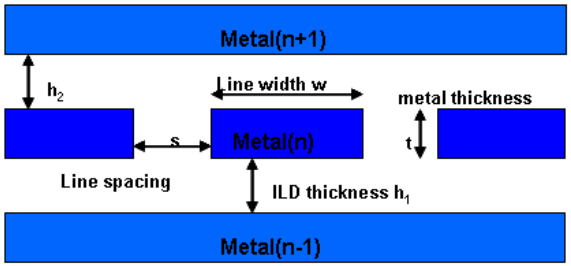




Sensitivity-Based Parasitic Extraction



Source: ITRS



ε: Dielectric constant
ρ: Resistivity

"**Sensitivity Model**" (first-order Taylor expansion):

$$C = C_o + C_{sys} + (\partial C/\partial p) \times \Delta p$$

$$R = R_o + R_{sys} + (\partial R/\partial p) \times \Delta p$$

where

$(\partial C/\partial p)$ = sensitivity of ***C*** w.r.t. ***p***

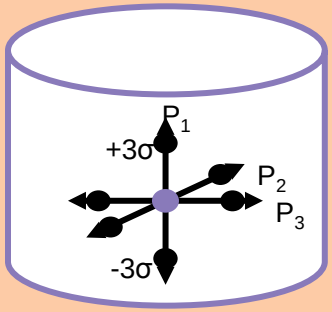
$(\partial R/\partial p)$ = sensitivity of ***R*** w.r.t. ***p***

Synopsys' Complete Variation-Aware Analysis Solution

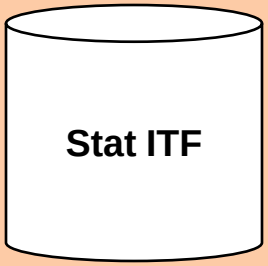
Liberty NCX

Library Characterization Tools

Variation-aware CCS models



Variation-aware Interconnect Tech



PrimeTime VX | Star-RCXT VX

Statistical / Advanced OCV

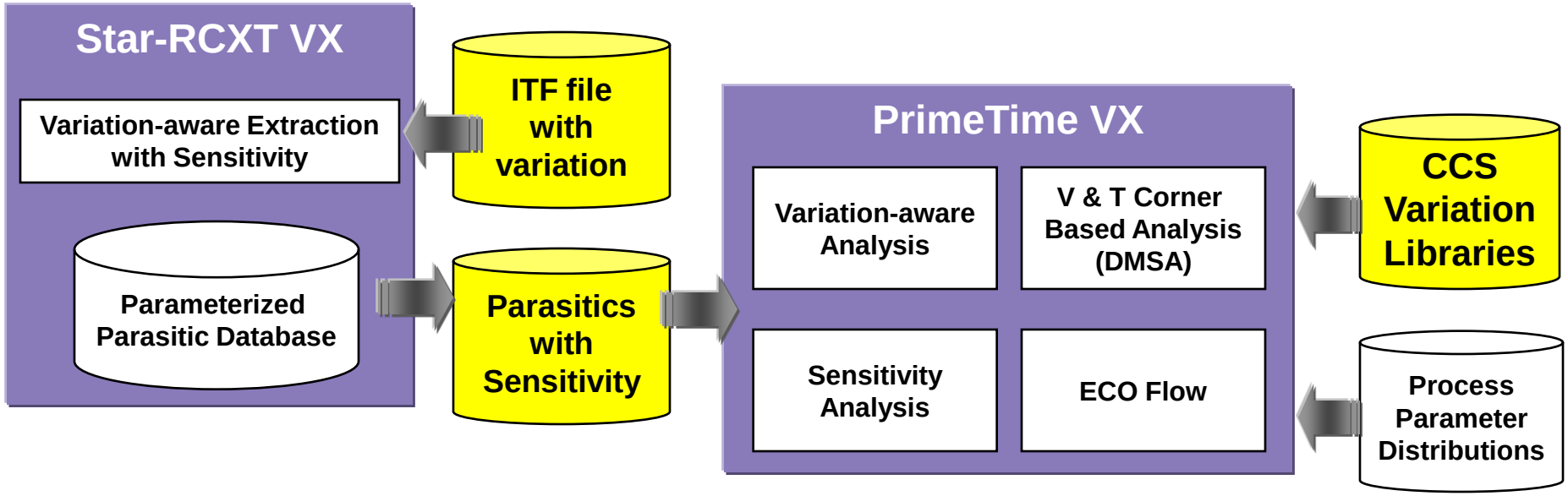
Multi-Scenario

Corner Analysis

PrimeTime | Star-RCXT

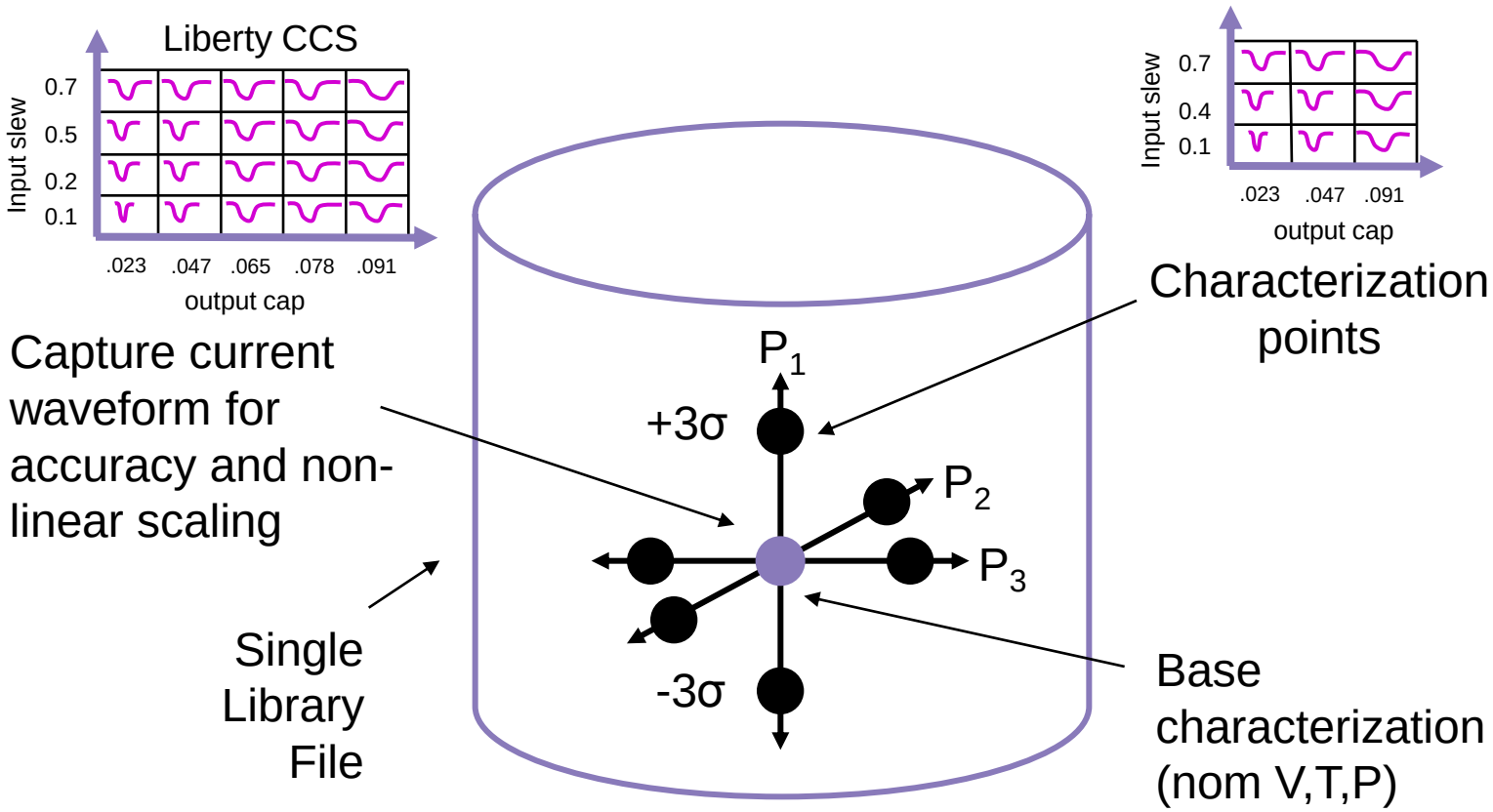
Analysis Flow

Supplying Variation Information



CCS Variation-aware Library

Characterization Example



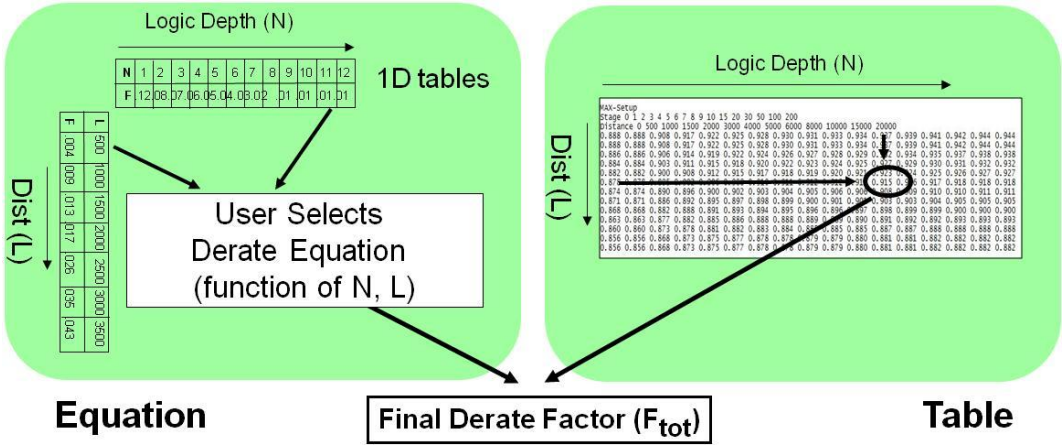
PrimeTime® Variation Modeling

A Staged, Evolutionary Approach

	On Chip Variation (OCV)	Advanced OCV (AOCV)	Variation-aware STA (PrimeTime VX)
Approach	Global derate for early/late timing	Path derate as a function of logic depth & cell location	statistical propagation of delay & slew
Benefit	Easy set-up using single bc/wc numbers	Intermediate step to statistical	Most accurate; concurrent die-to-die and on-chip analysis
Usage	Down to 65-nm/45-nm	90 to 40-nm, 32nm?	Initial usage at 40-nm
Challenge	Safe, but can be pessimistic; becomes overloaded to model many effects	Requires silicon data from foundries / fab	Requires most characterization: variation-aware libraries
Cost of Adoption	Very low	Low to medium	High

Advanced OCV

- Models random variation (on die variation)
  - Deeper paths exhibit less variation than short paths
  - 1D table – derates decrease as path depth increases
- Models systematic variation (location based)
  - Paths comprised of cells in close proximity will exhibit less variation
  - 1D tables - derates increase as path distance increases
- Models both random & systematic variation
  - 2D tables – derates as a function of both depth & distance



Summary

- Greater variation at <65nm node is real
  - A plethora of techniques are being deployed to contain its impact
- Evolutionary and revolutionary **flow-based** EDA techniques have emerged
  - Advanced OCV, Variations-aware / Statistical STA, sensitivity-based extraction, characterization tools, libraries
  - DFM and layout techniques, etc.
- To a large extent, the industry has been successful in containing this problem at low cost at 65nm through 40nm