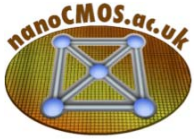
Statistical Variability and Reliability in the Next Generation CMOS Technologies and the ITRS Response

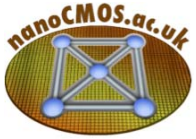


A. Asenov

University *of* Glasgow

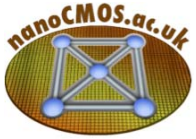
www.elec.gla.ac.uk/groups/dev_mod

University of Glasgow



Summary

- Background
- Bulk MOSFETs
- Novel device architectures
- Statistical reliability
- Conclusions



Summary

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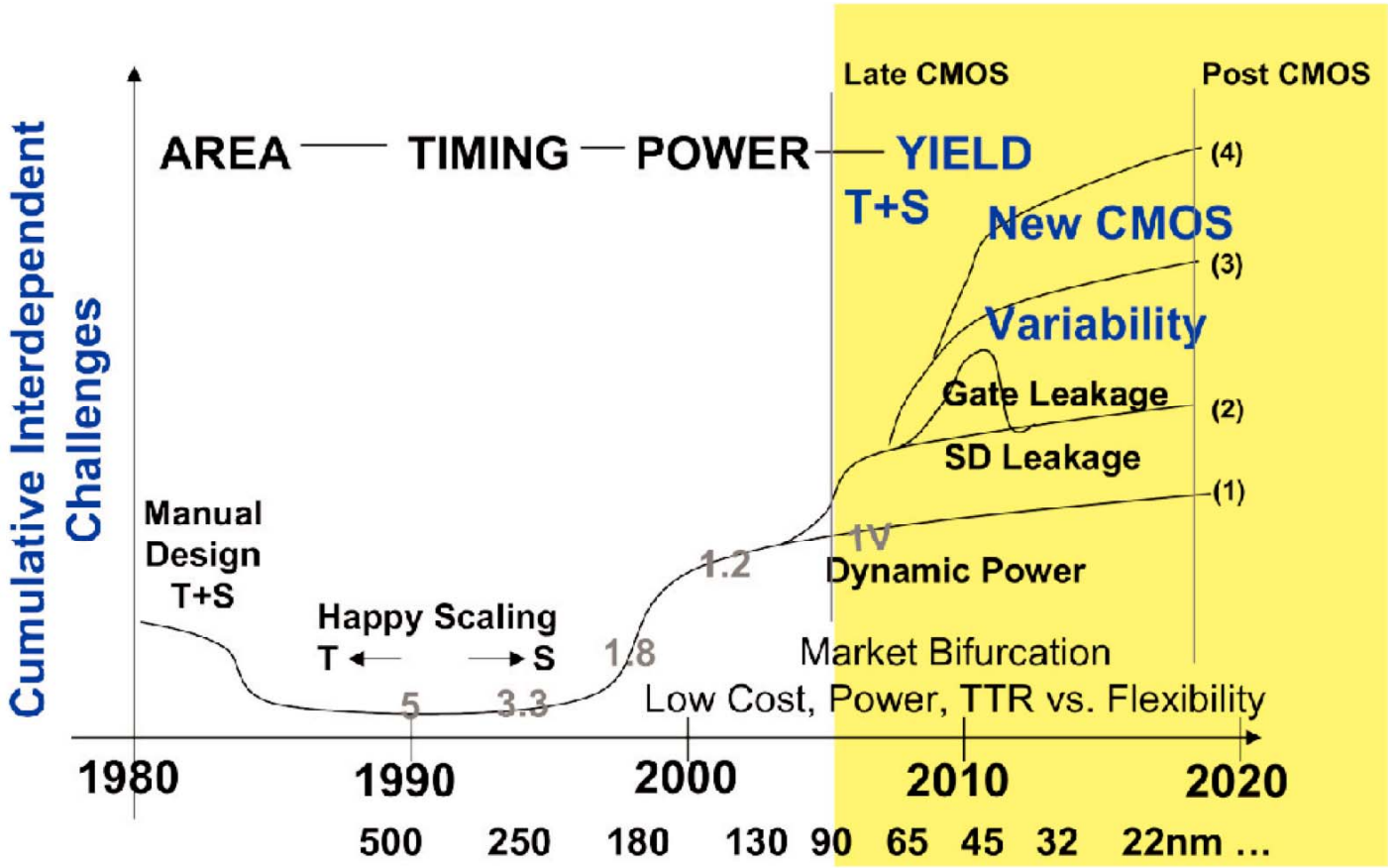
Variability has become a major challenge to scaling and design



G. Declerck, Keynote talk, VLSI Technol. Symp. 2005

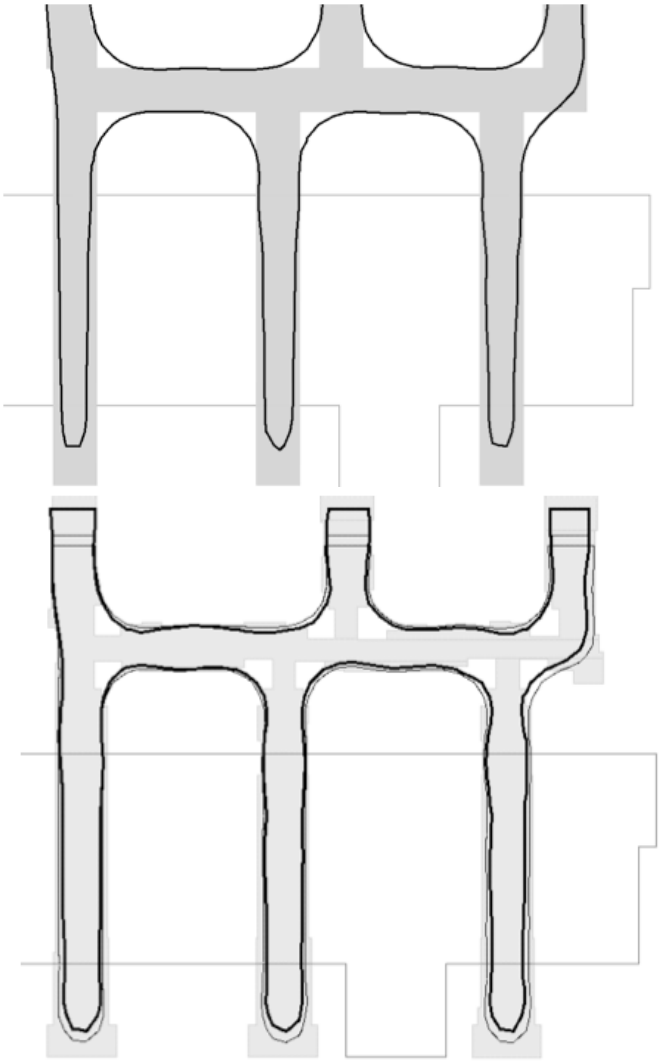
Local statistical variability is a major source of concern

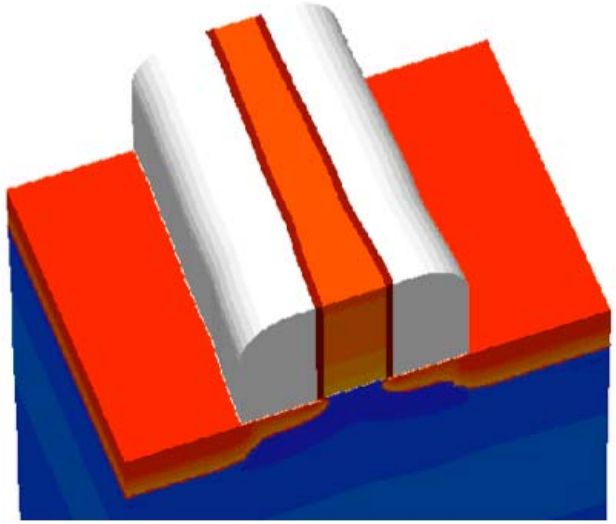
		Process	Environment	Temporal
Global		<L_g> and <W> <layer thicknesses> <R>'s <doping> <V_{body}	T environment range V_{dd} range	<NBTI> Hot electron shifts
Local	Systematic	OPC Phase shift Layout mediated strain Well proximity	Self-heating IR drops	Distribution of NBTI Voltage noise SOI V_{body} history Oxide breakdown history
Local	Statistical	**Random dopants** **Line Edge Roughness** **Poly Si granularity** **Interface roughness** **High-k morphology**		
Across-chip		Line width due to pattern density effects	Thermal hot spots due to non-uniform power dissipation	Computational load dependent hot spots

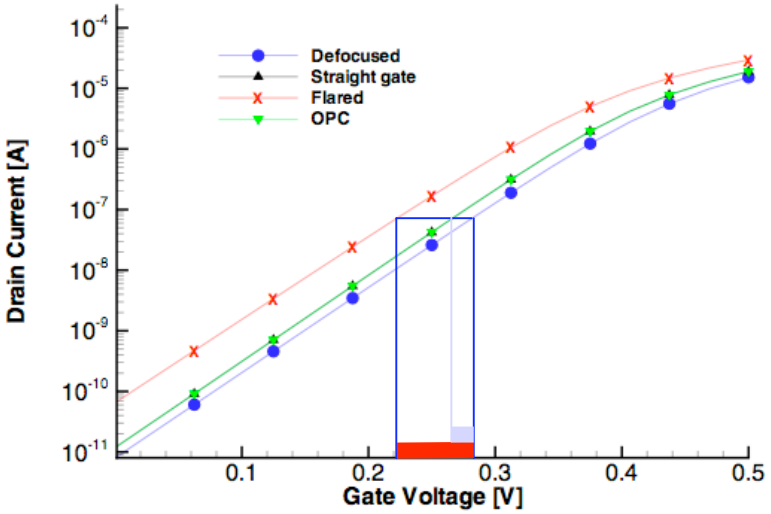
After D. J. Frank (IBM)

OPC and strain related variability

65 nm example Synopsys (SISPAD 06)

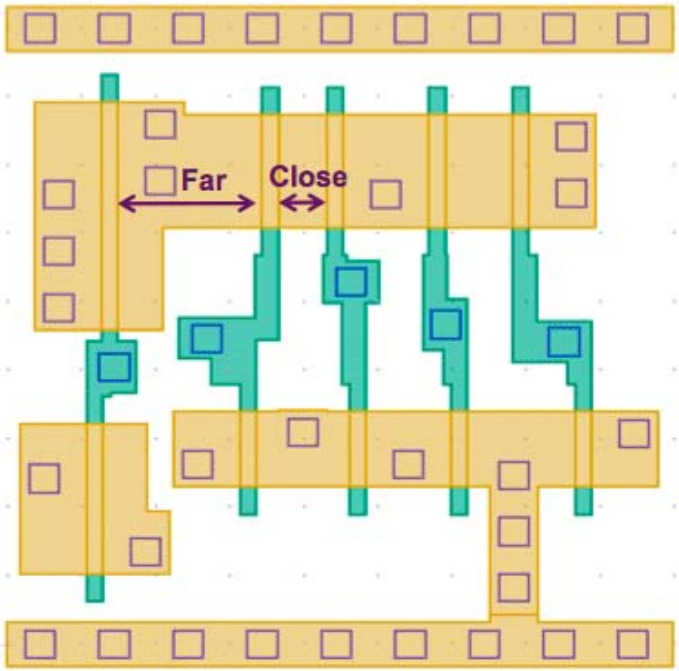


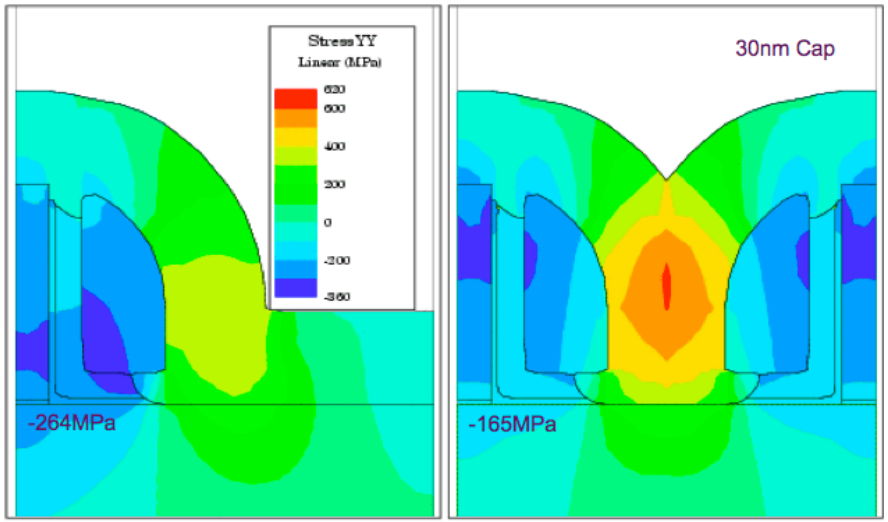


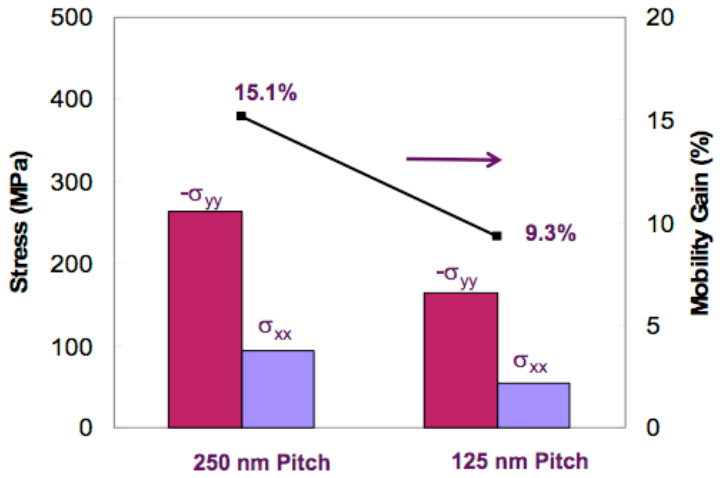


Strain induced variability

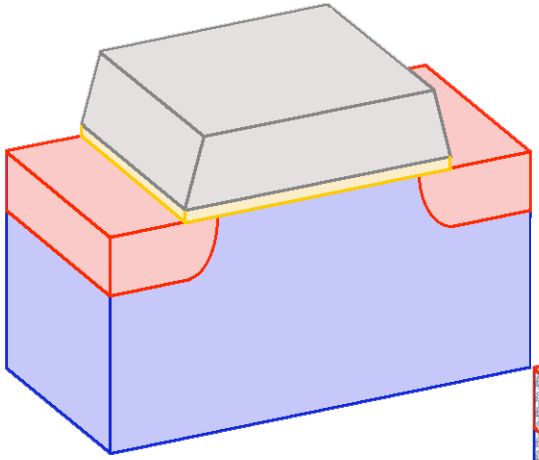
After W. Fichtner



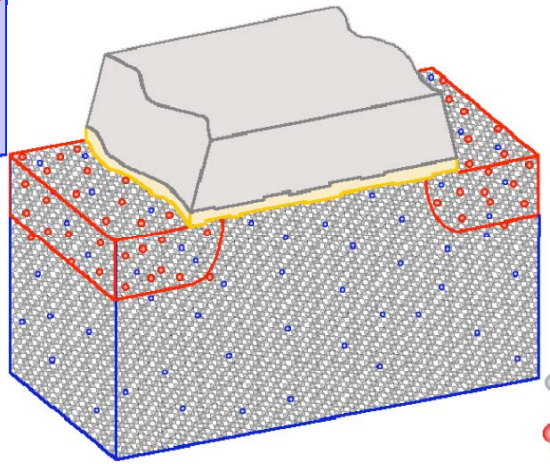




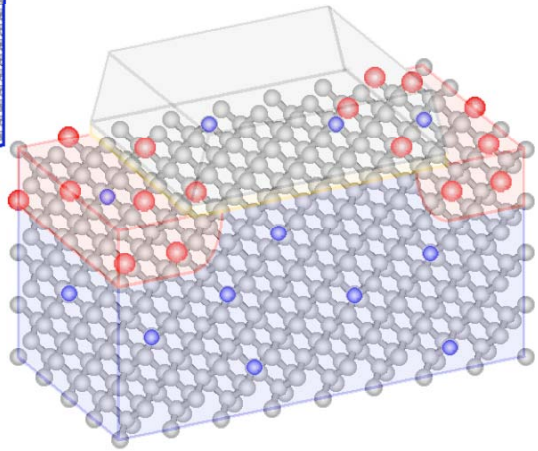
Statistical variability



The ideal transistor

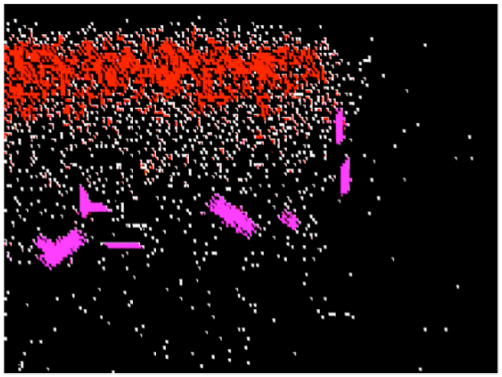


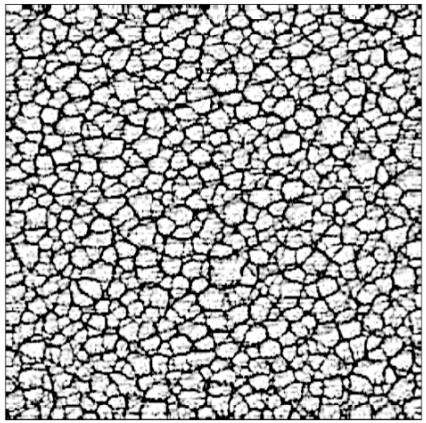
A 22 nm MOSFET

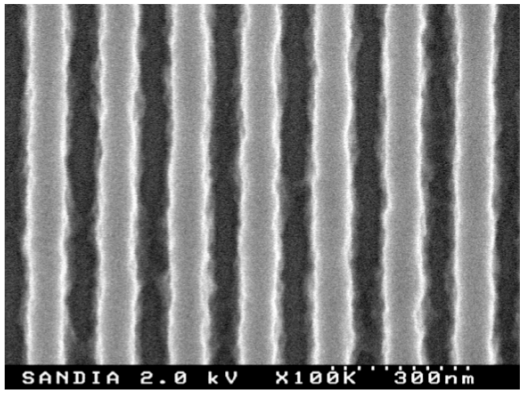


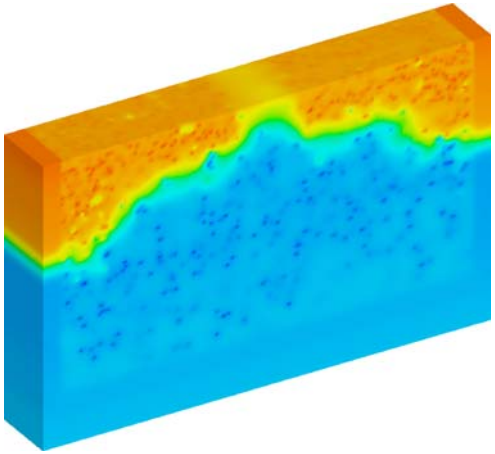
A 4.2 nm MOSFET

Statistical variability

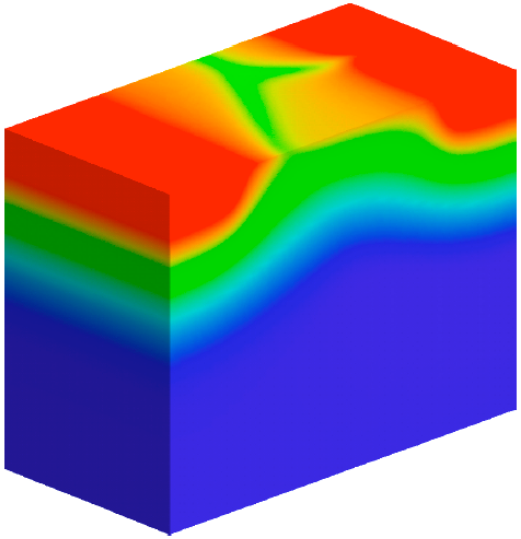




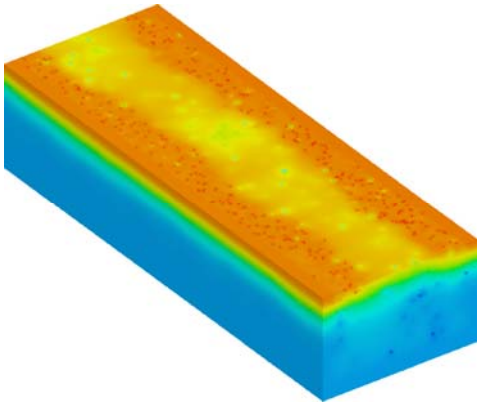




Random dopants

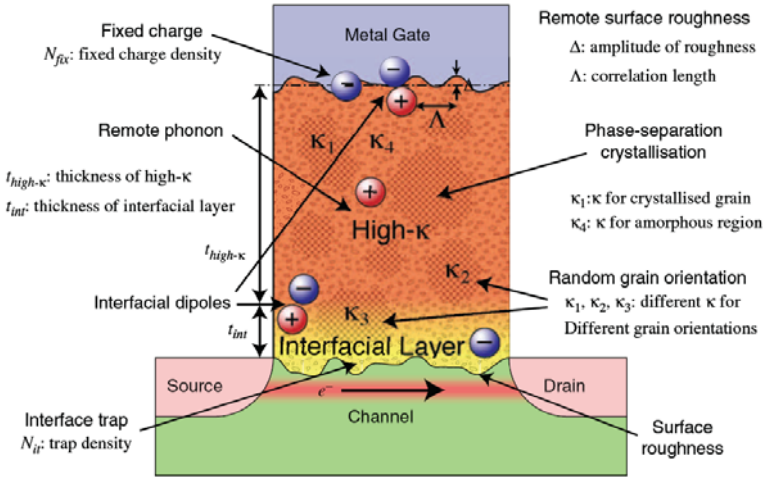


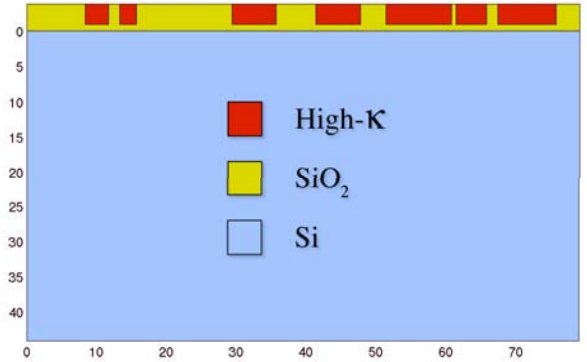
Polysilicon/high-k
Granularity

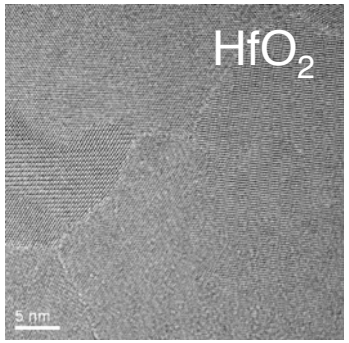


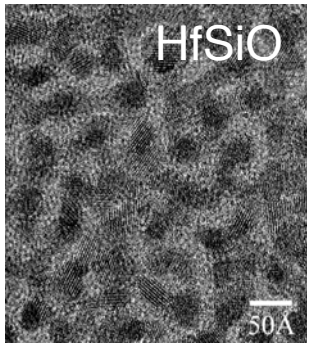
Line edge roughness

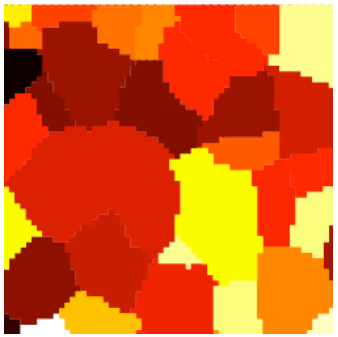
High-κ and metal gate morphology

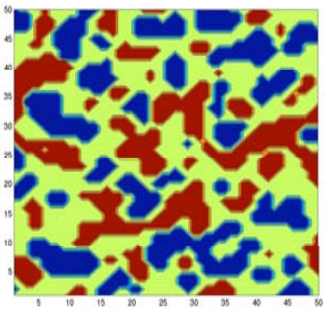


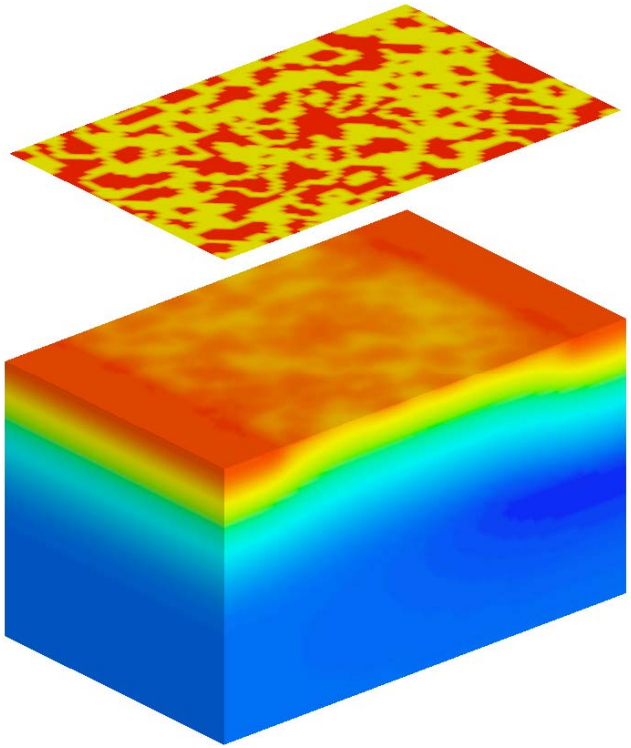






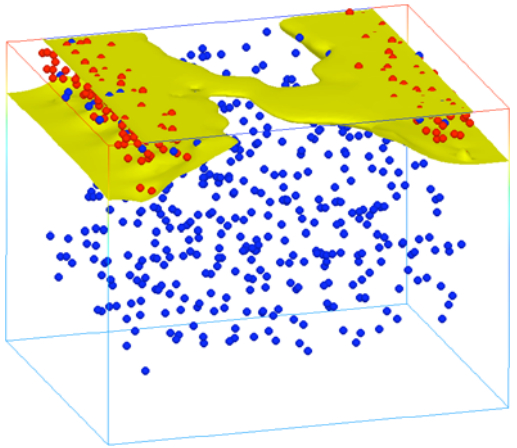




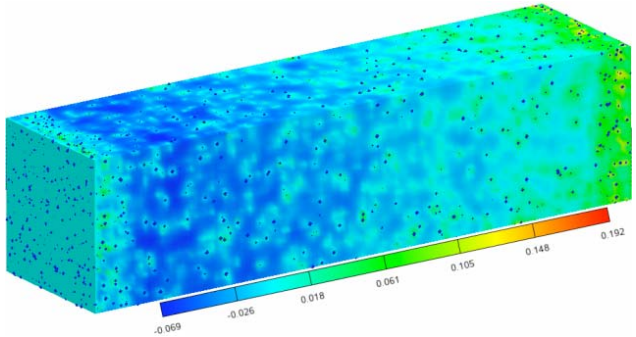


Glasgow statistical 3D simulation tools

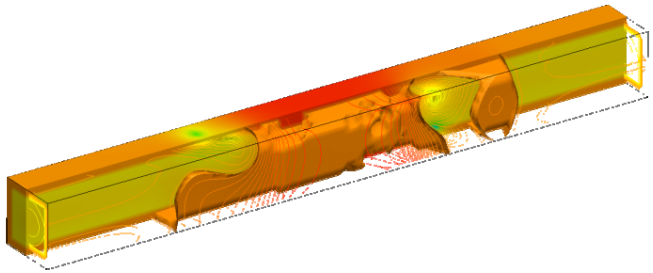
- Drift-Diffusion (DD) with quantum corrections.



- Ensemble Monte Carlo (MC) with *ab-initio* impurity scattering.

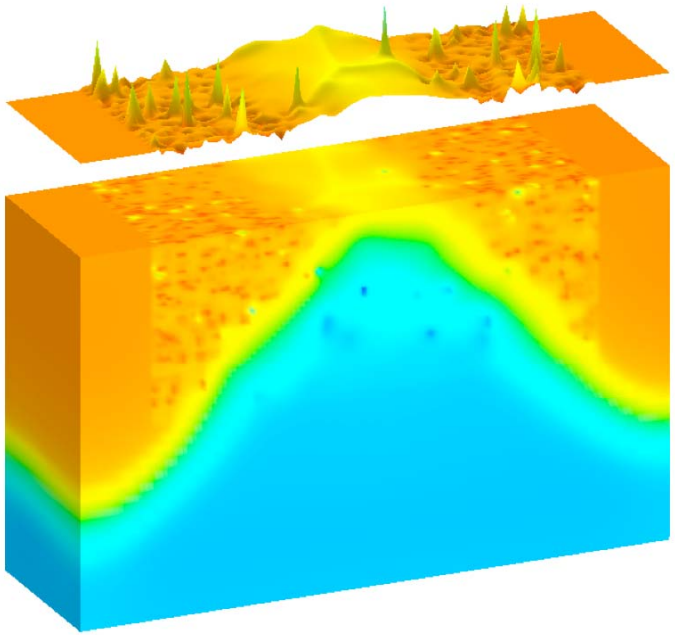


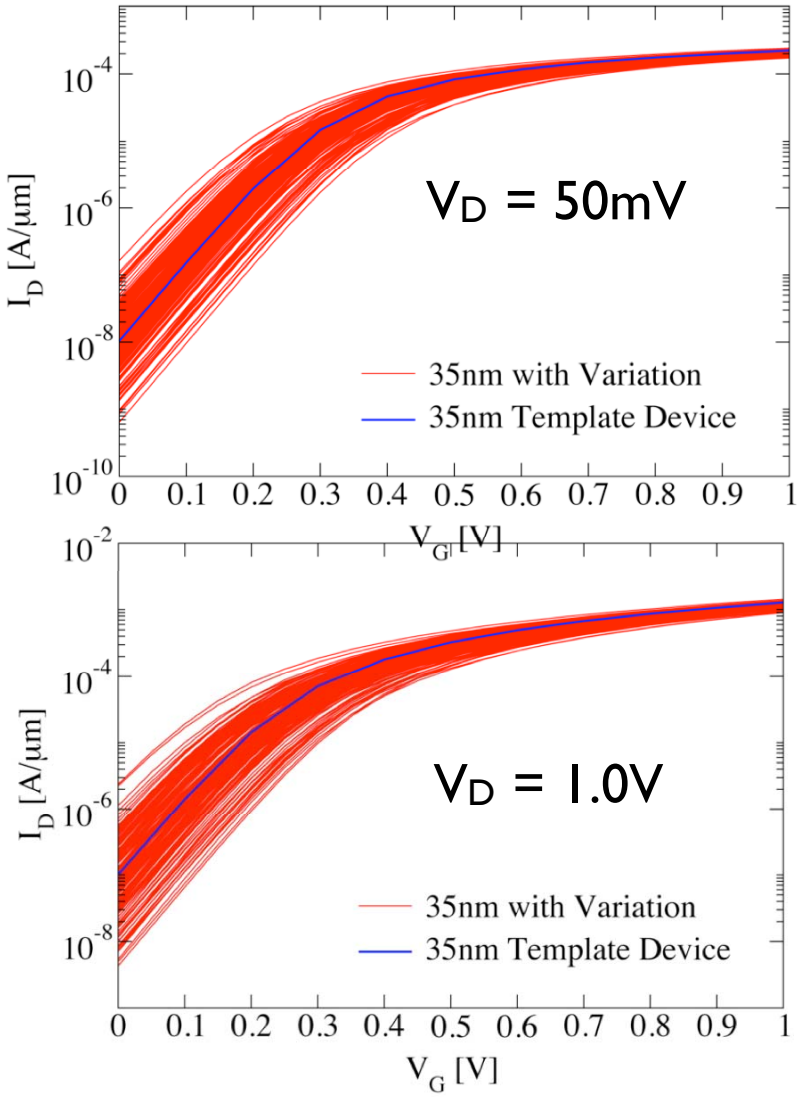
- Non-Equilibrium Green's Functions (NEGF).



Enabled by the power of cluster and grid computing

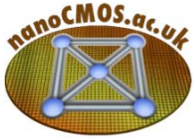
The most comprehensive technology available





RDD+LER+PSG
Compact models

University of Glasgow



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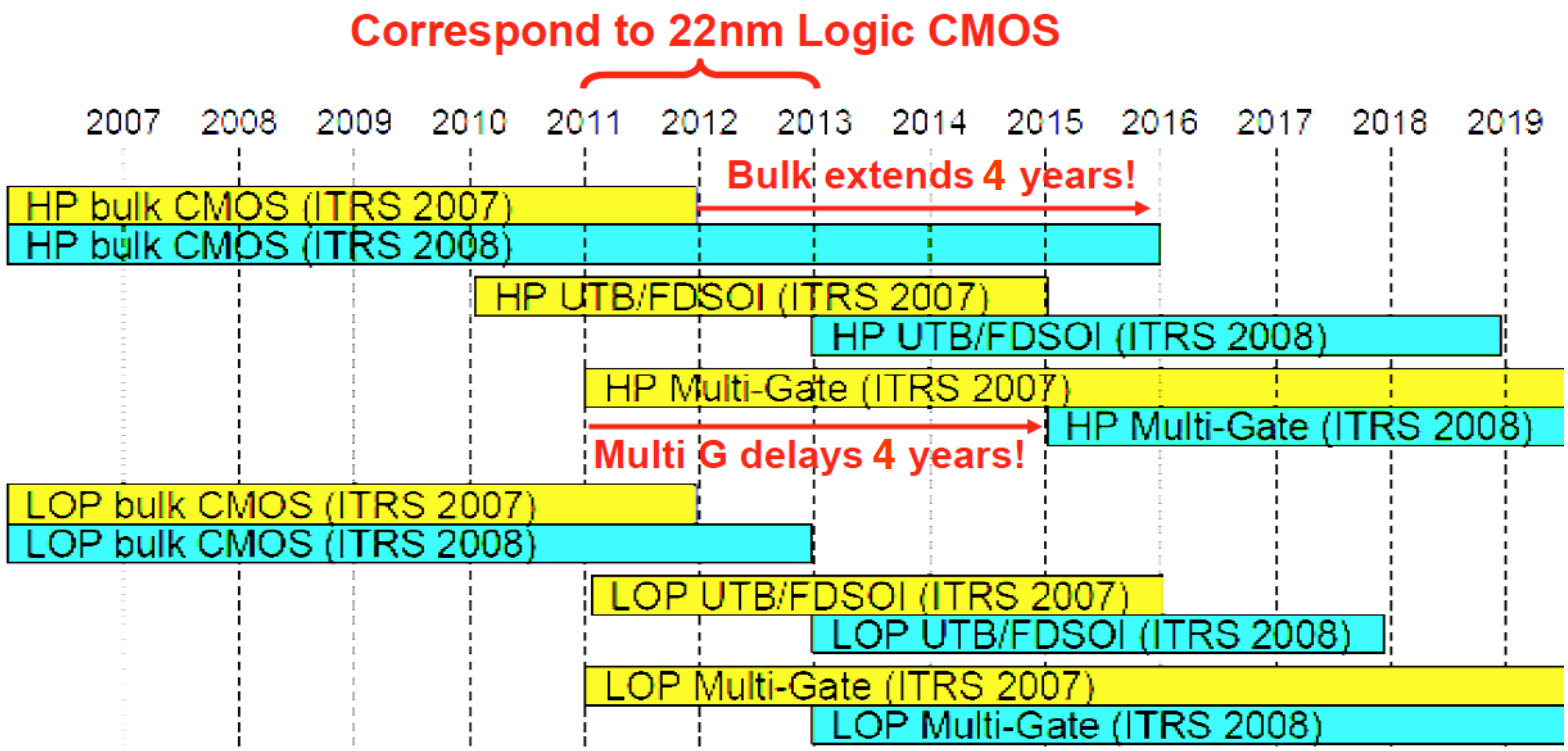
Bulk MOSFETs are here to stay longer

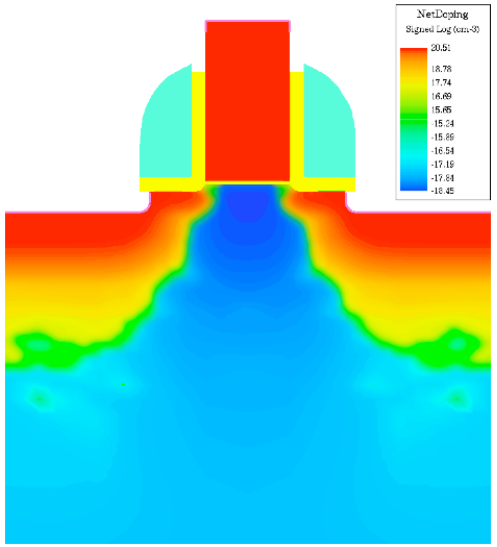
Timing of CMOS innovations shifts backward.

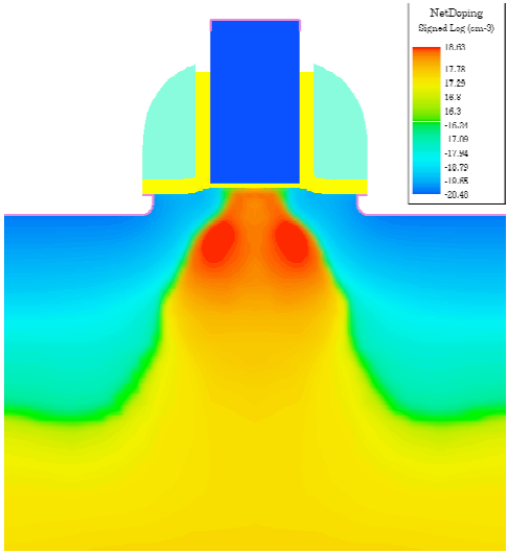
Bulk CMOS has longer life now!

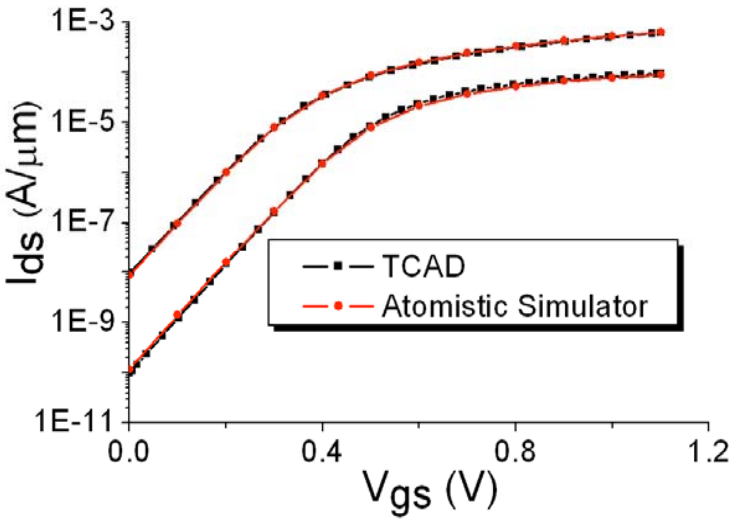


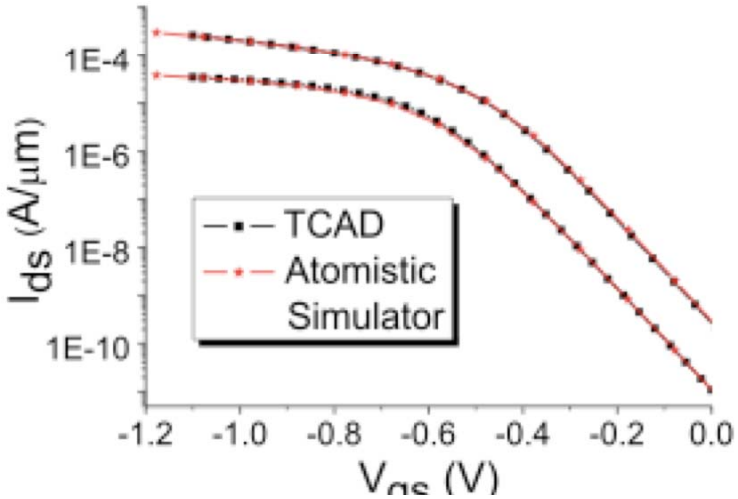
After H. Ivai

Variability in 45 nm LP transistors



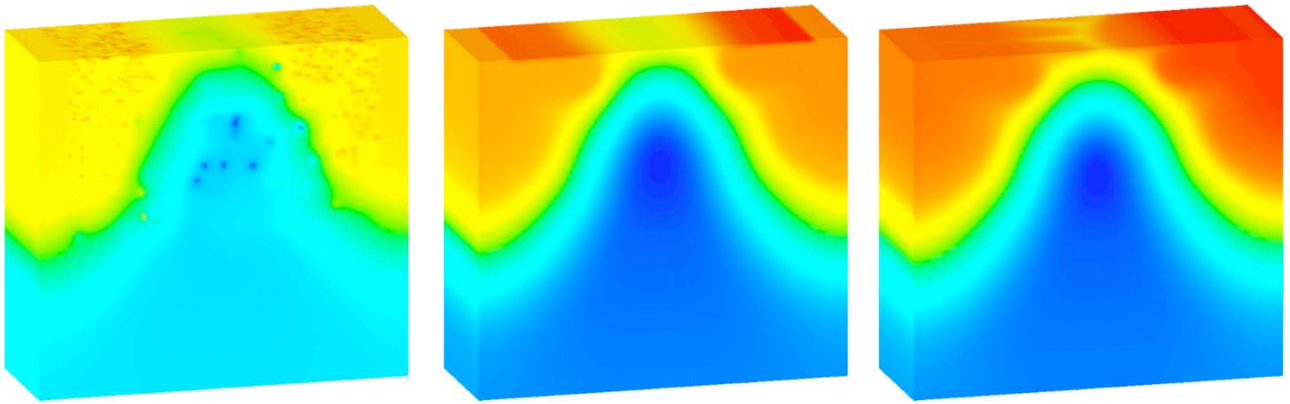






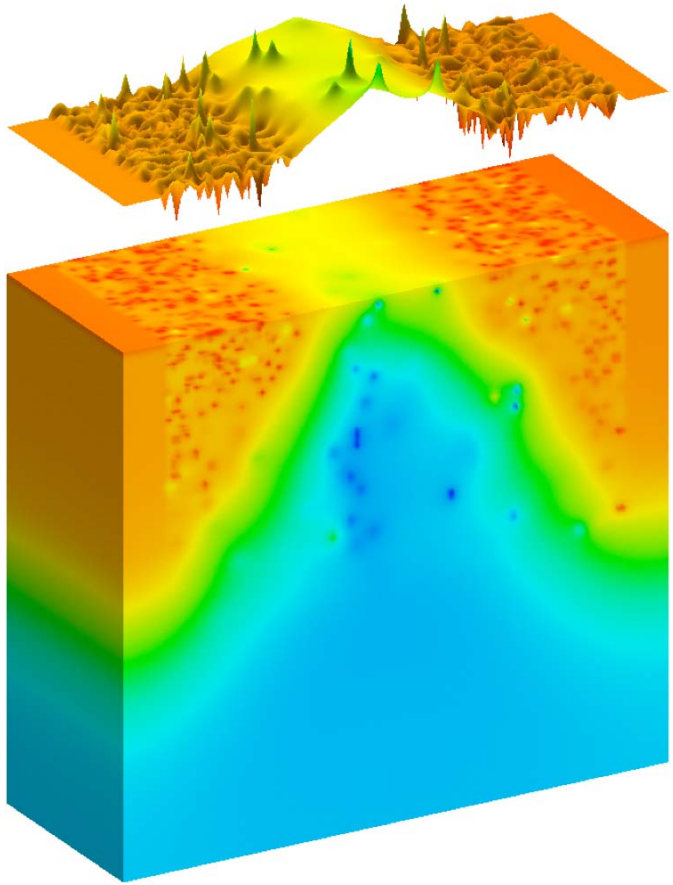
In collaboration with ST Microelectronics

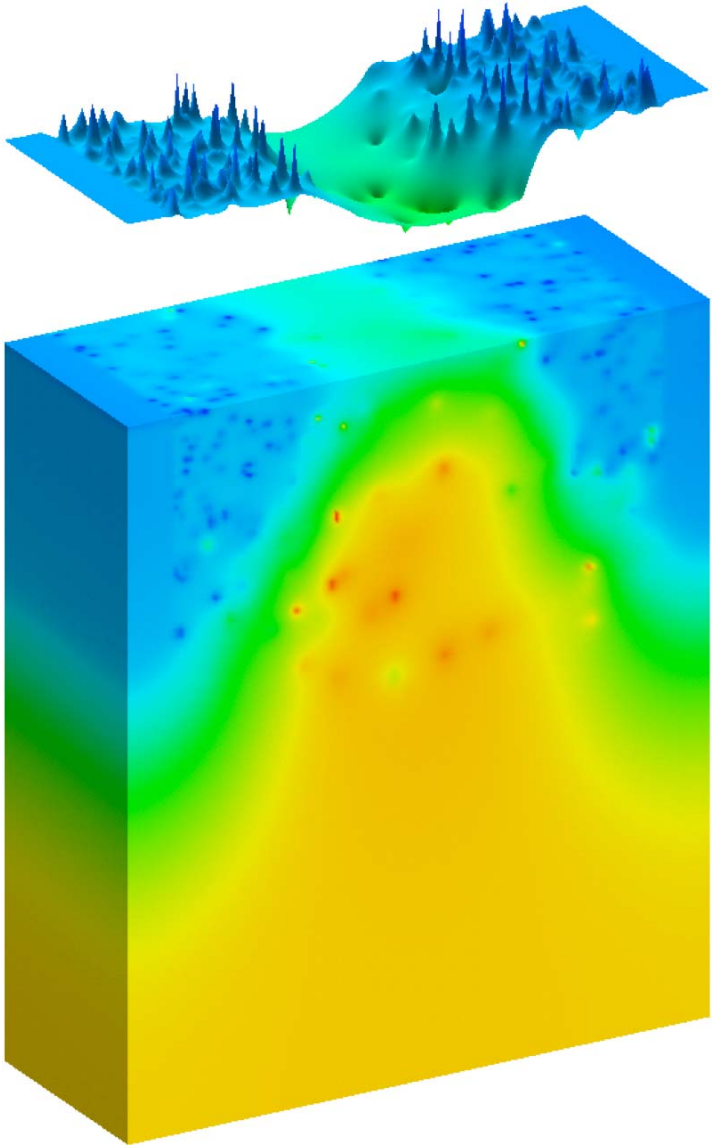
Good agreement with measurements



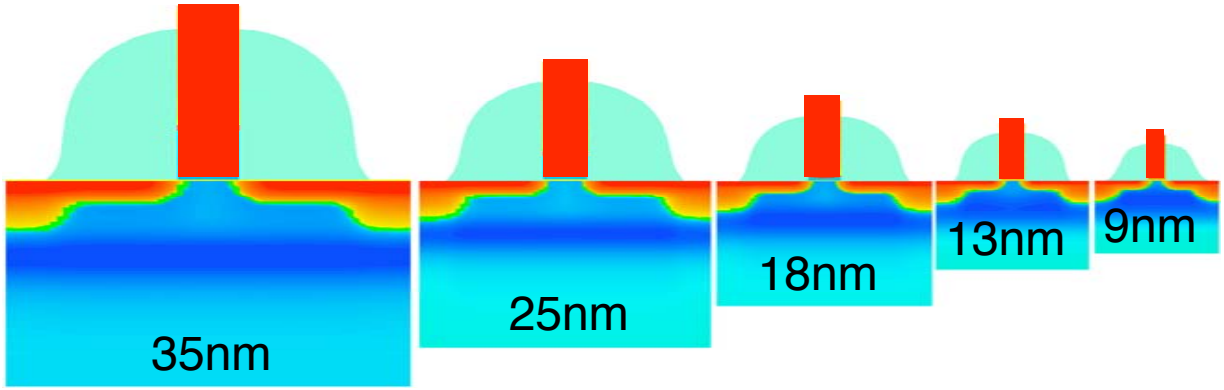
	n-channel MOSFET		*p*-channel MOSFET	
	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)	σV_T [mV] (V_{DS}=0.05 V)	σV_T [mV] (V_{DS}=1.1 V)
RDD	50	52	51	54
LER	20	33	13	22
PSG	30	26	-	-
Combined	62	69	53	59
Experimental	62	67	54	57

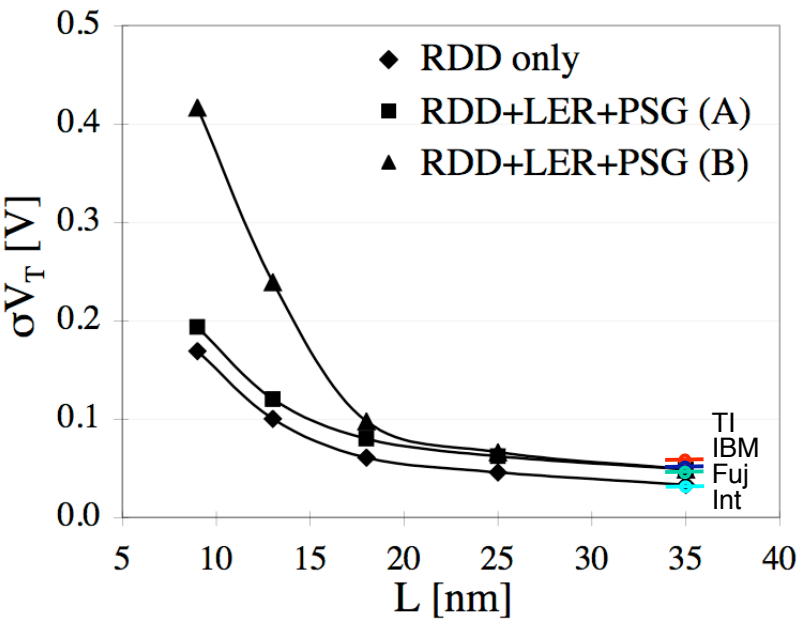
Potential distributions



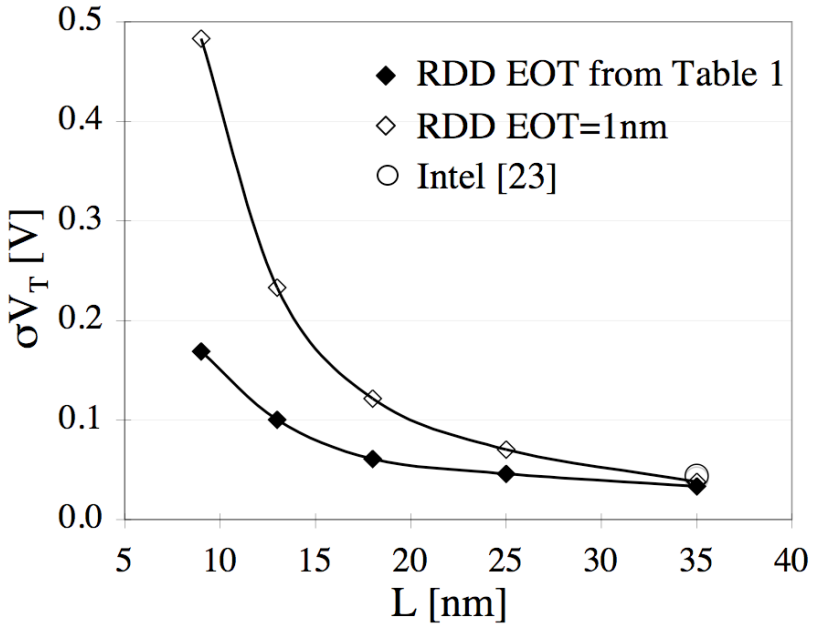


Combined variability in bulk MOSFETs



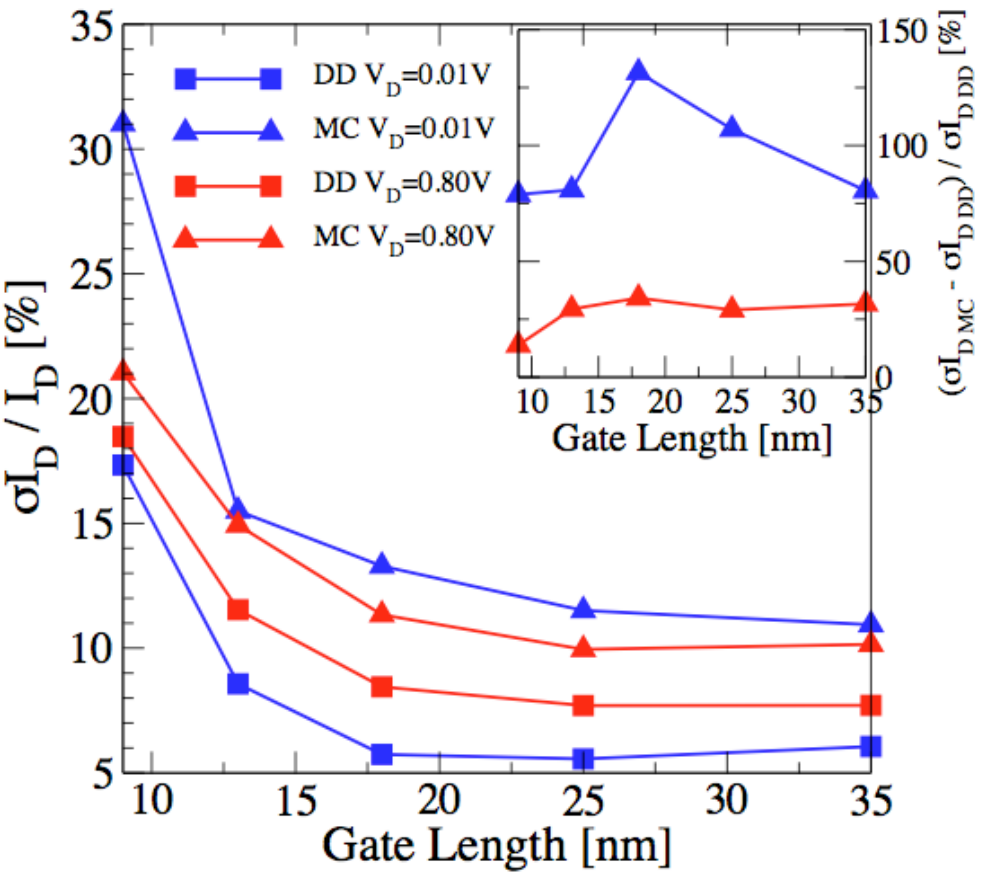


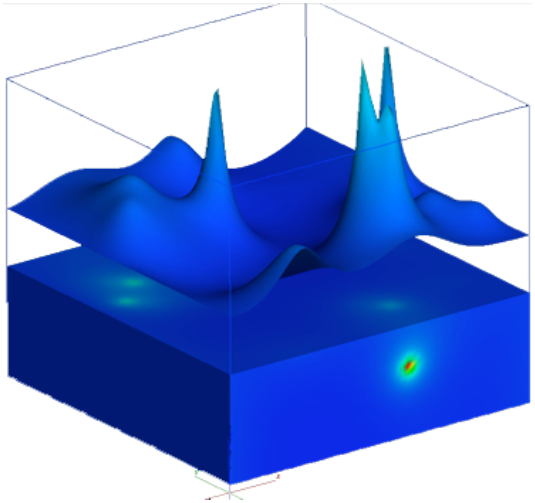
t_{ox} scales according to ITRS

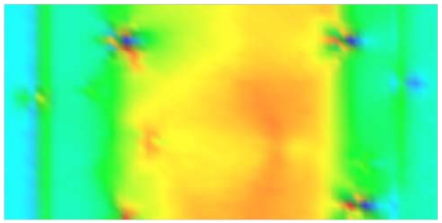


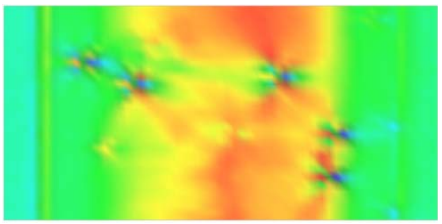
t_{ox} remains constant

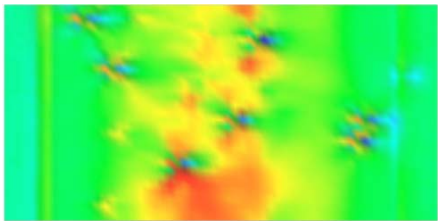
Transport (scattering) related variability



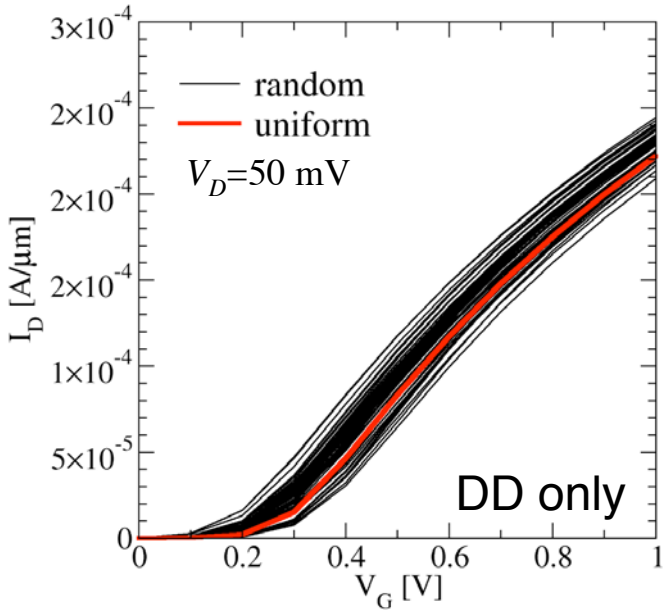


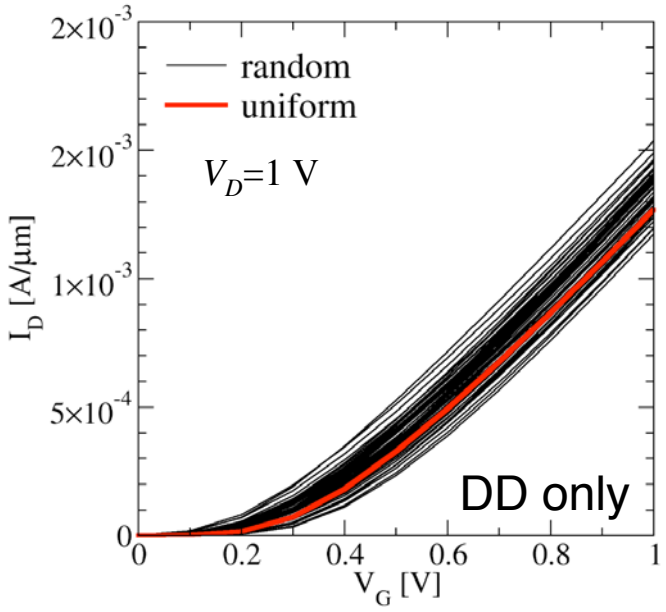


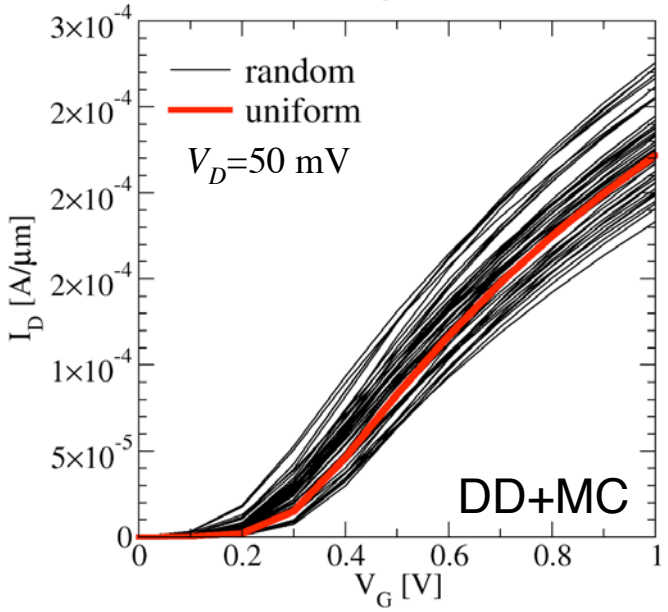


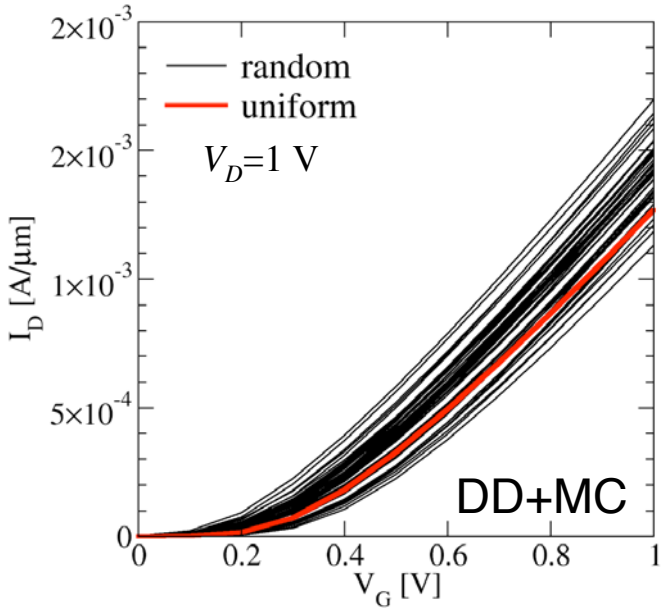


The impact of the transport related variability



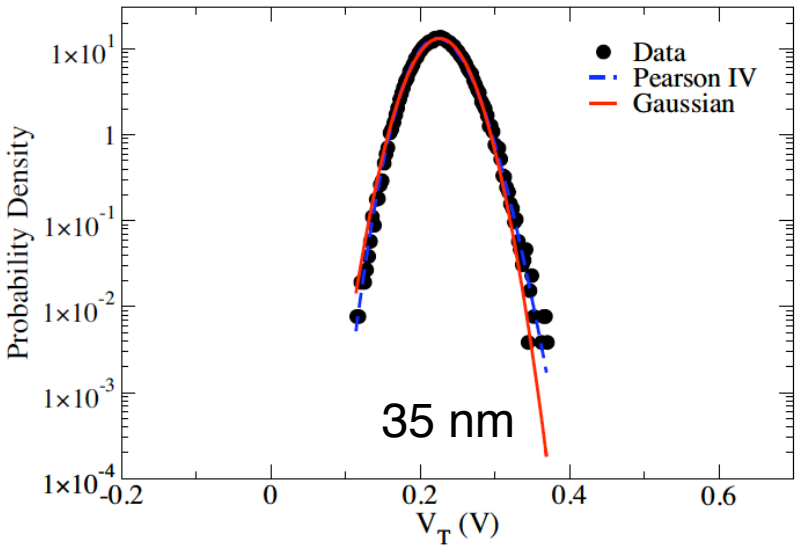


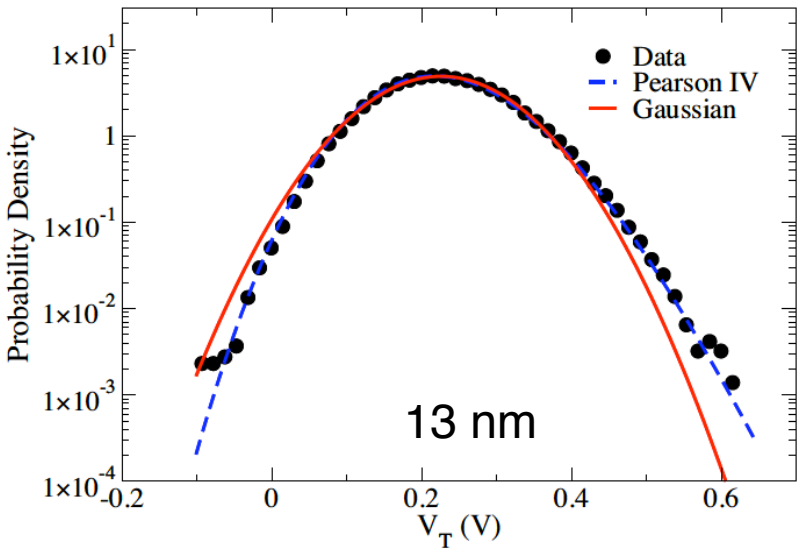


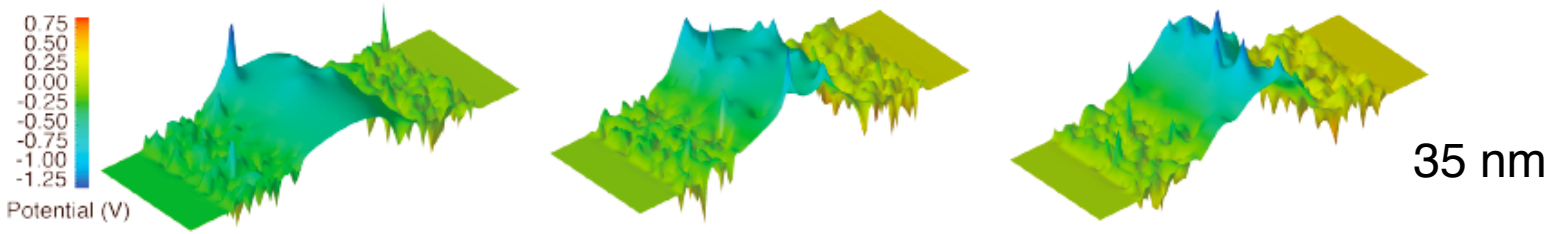


35 nm MOSFET

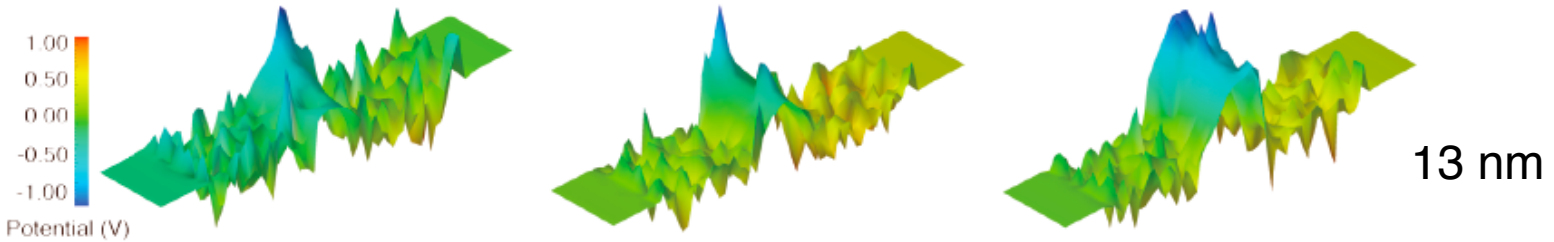
Simulation of 100000 statistical sample







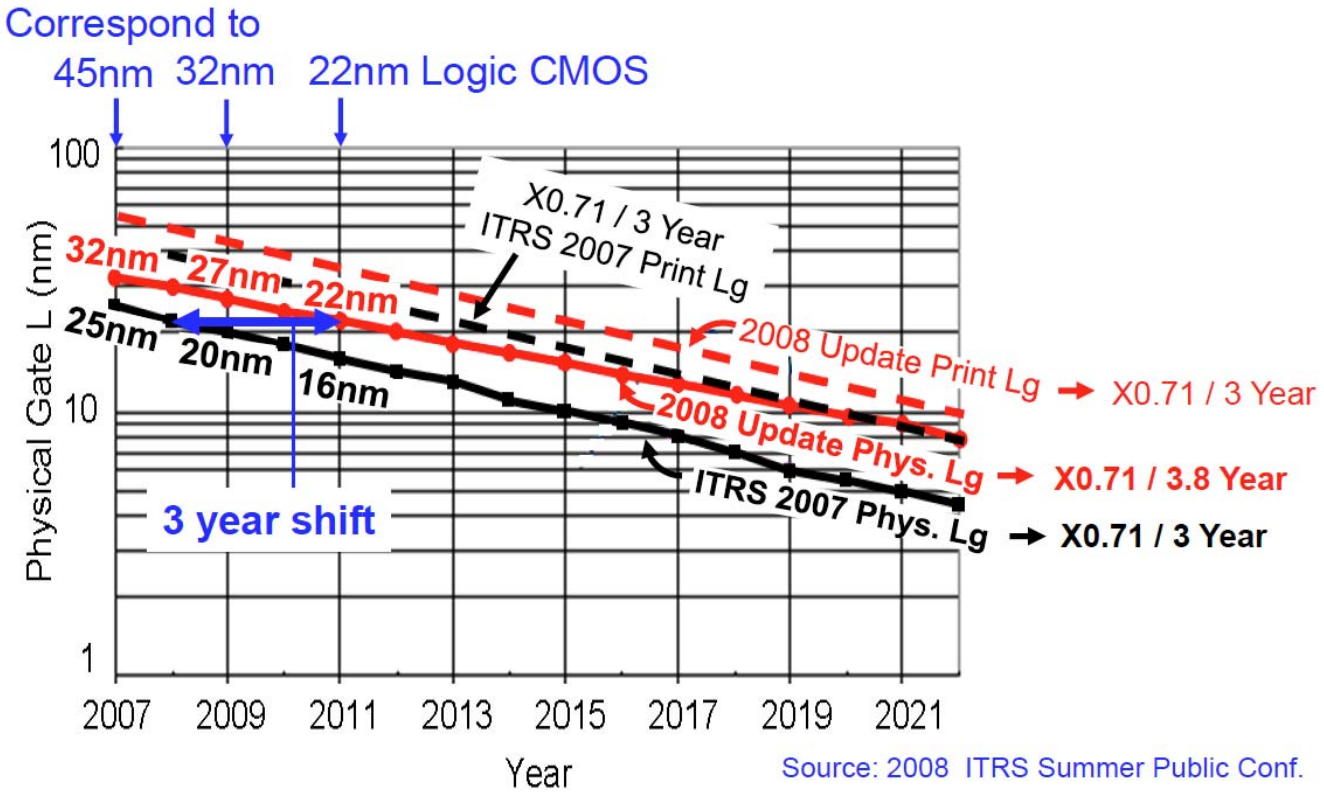
Low V_T Medium V_T High V_T



Bulk MOSFETs are here to stay longer: But they will be longer too

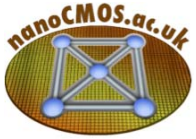
Physical gate length in past ITRS was too aggressive.
The dissociation from commercial product prediction will be adjusted.

Physical gate length of High-Performance logic will shift by 3-5 yrs.



Source: 2008 ITRS Summer Public Conf.

After H. Ivai

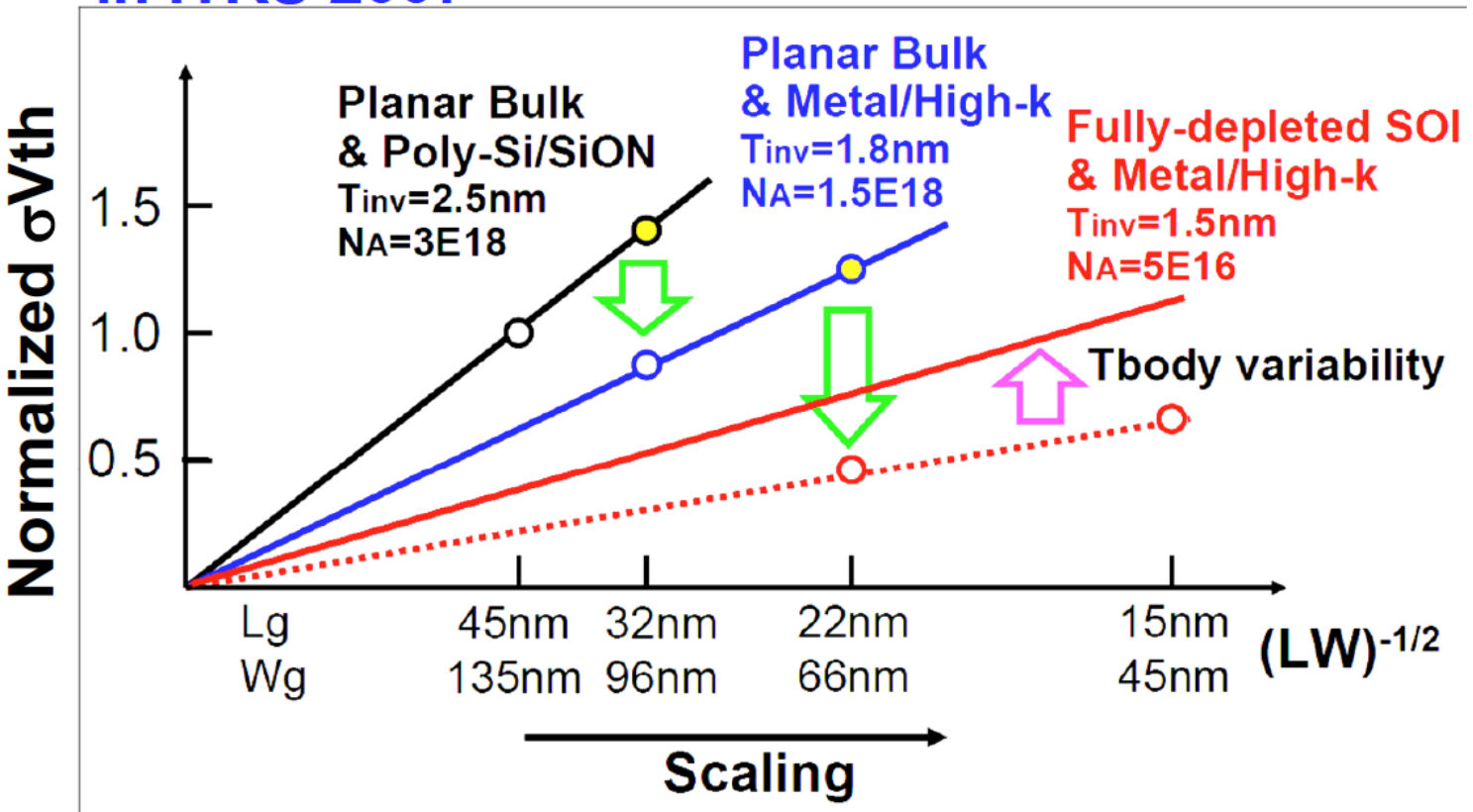


Summary

- Background
- Bulk MOSFETs
- Novel device architectures
- Statistical reliability
- Conclusions

Novel transistors are wanted mainly due to reduced statistical variability

Random Variability Reduction Scenario in ITRS 2007

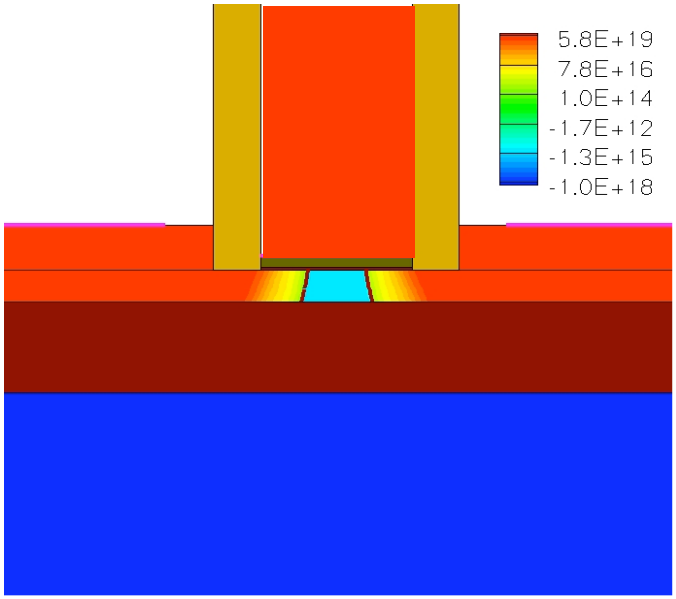


Assumption: Random dopant fluctuation is Main source of Random Variability. Line width roughness of Lg and Wg is not considered in this

After H. Ivai

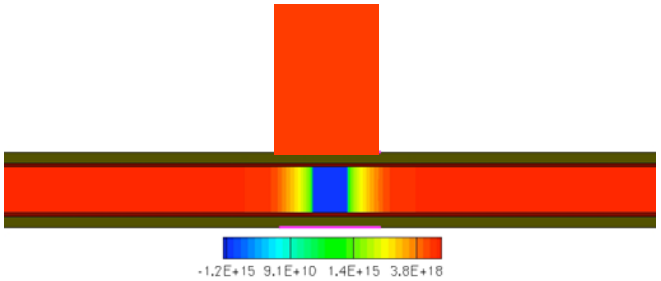
SOI and DG variability in PULLNANO template transistors

32 nm FD SOI



T_{ox}=1.2 nm
T_{Si}=7 nm

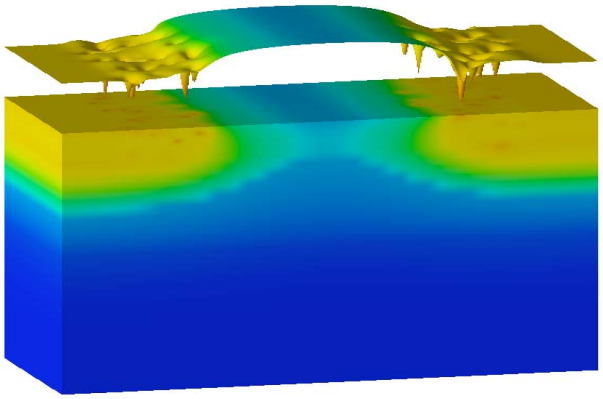
22 nm DG



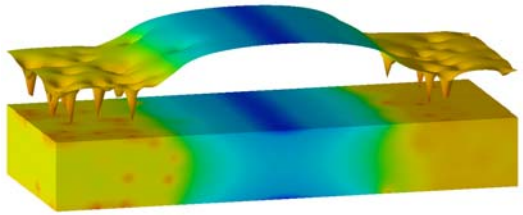
T_{ox}=1.1 nm
T_{Si}=10 nm

SOI and DG variability

32 nm FD SOI

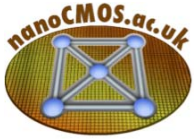


22 nm DG



	32nm σV_T (mV)		22nm σV_T (mV)	
	V_{ds} (50mV)	V_{ds} (1.0V)	V_{ds} (50mV)	V_{ds} (1.0V)
RDD	5.3	6.1	6.4	8.1
LER	3.3	8.6	5.8	13
Trap (1e11)	11	11	5.1	4.8
Combined (1e11)	13	15	10	16

University of Glasgow



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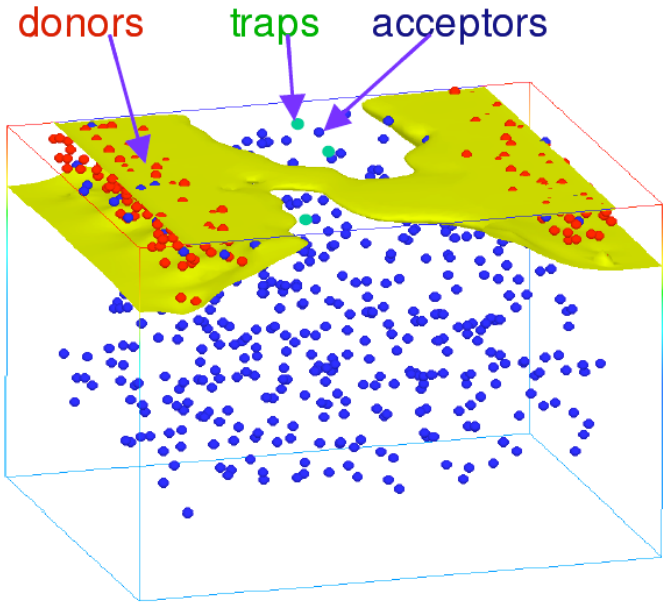
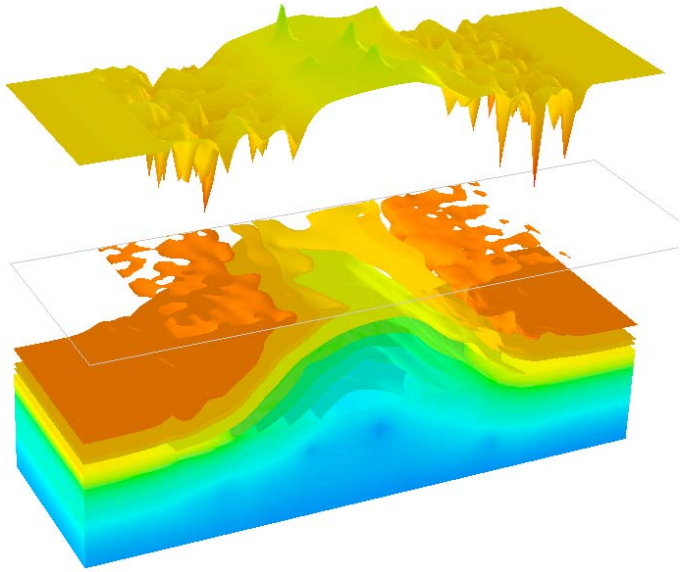
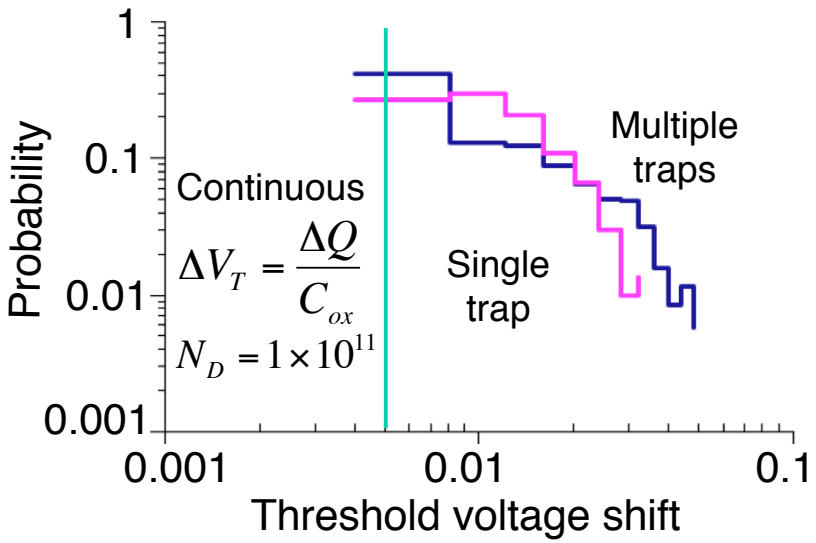
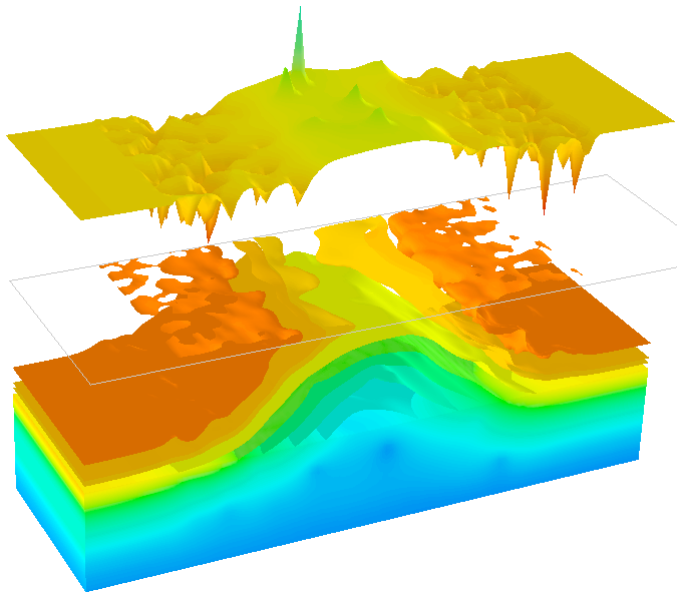
Statistical reliability: electrostatics

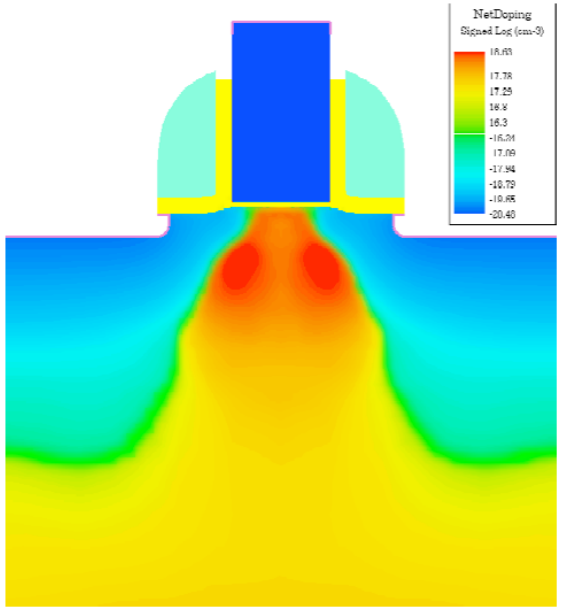


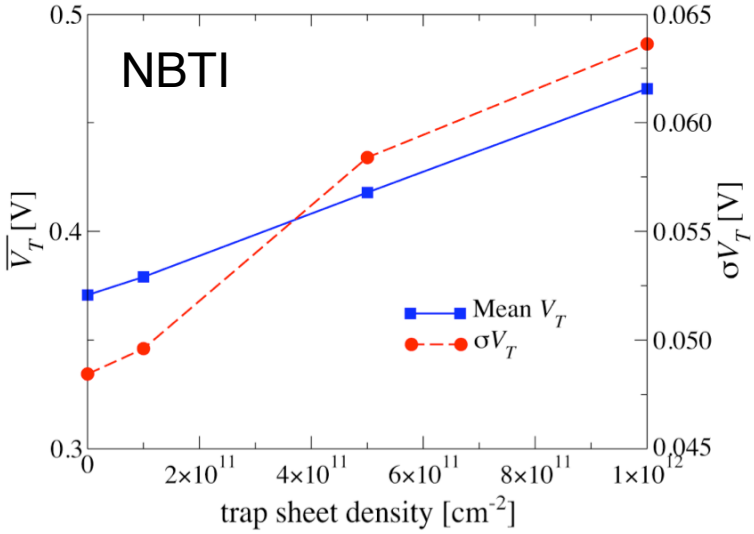


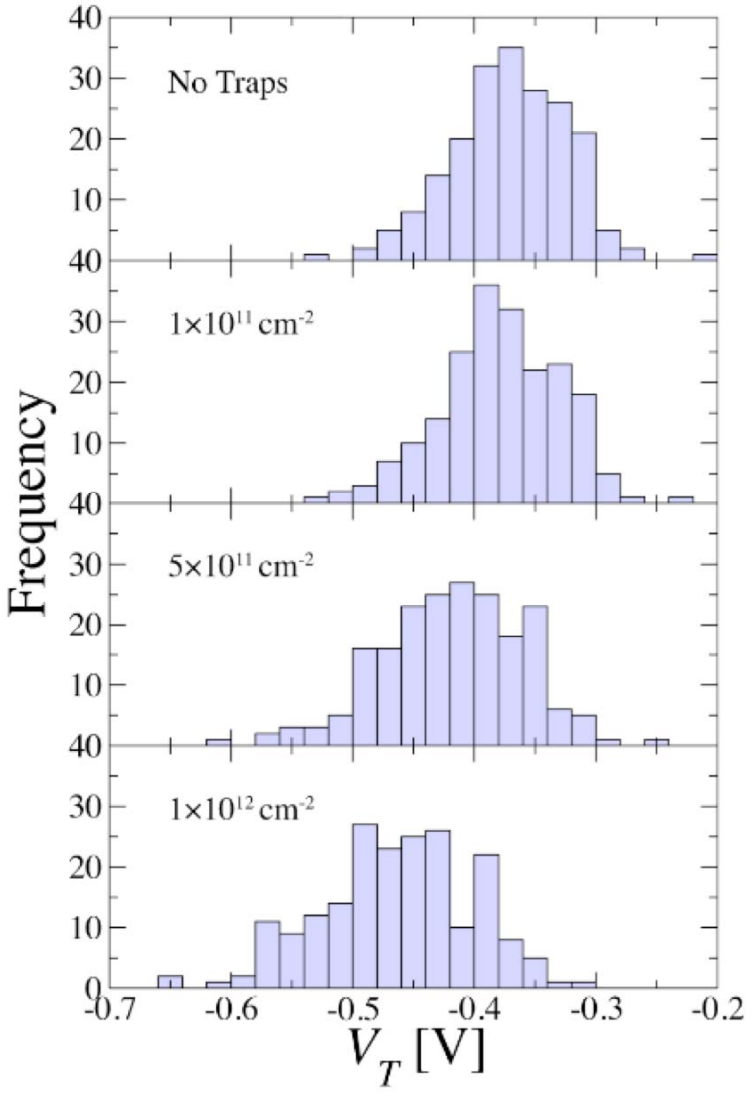




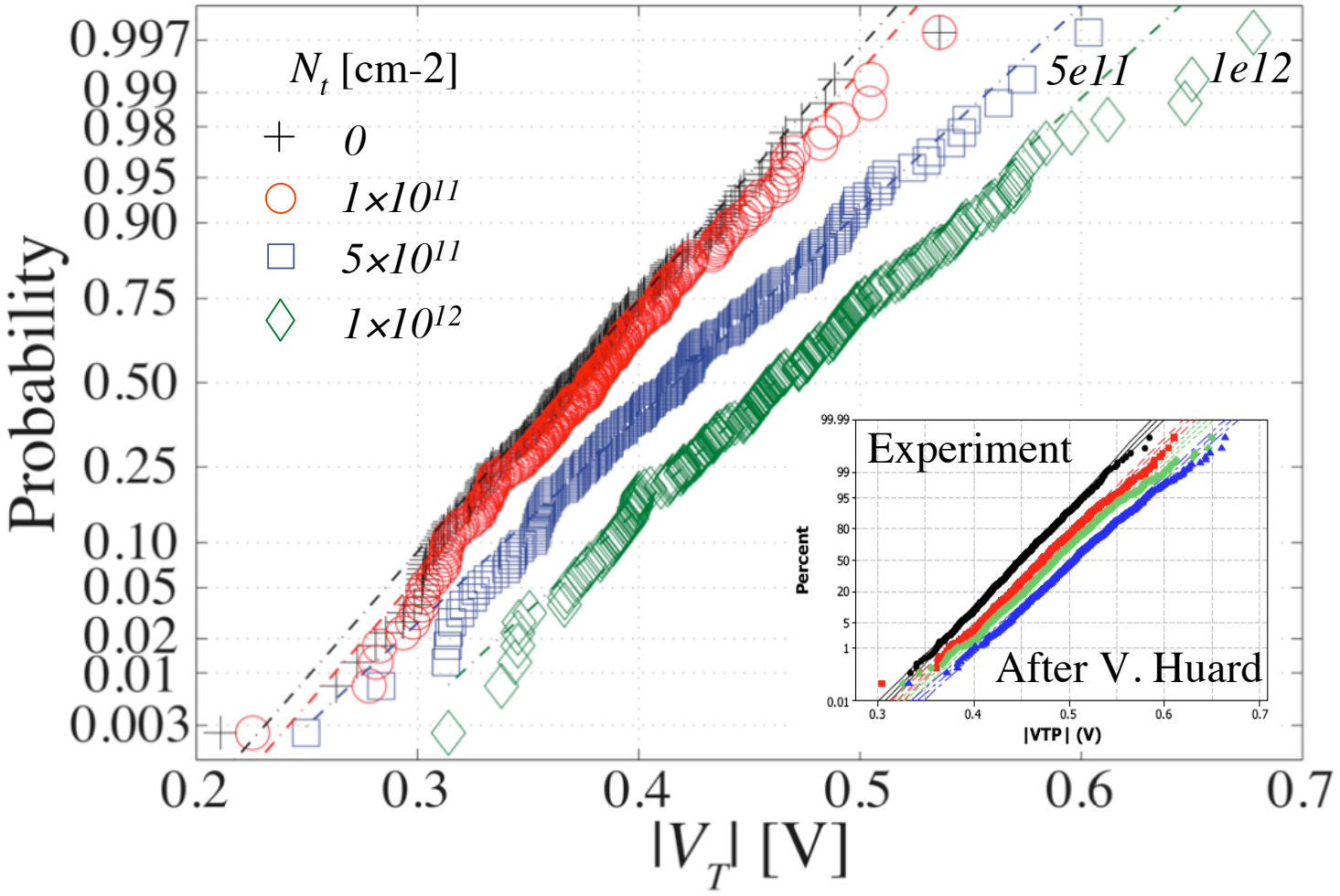
Statistical reliability in 45 nm LP technology



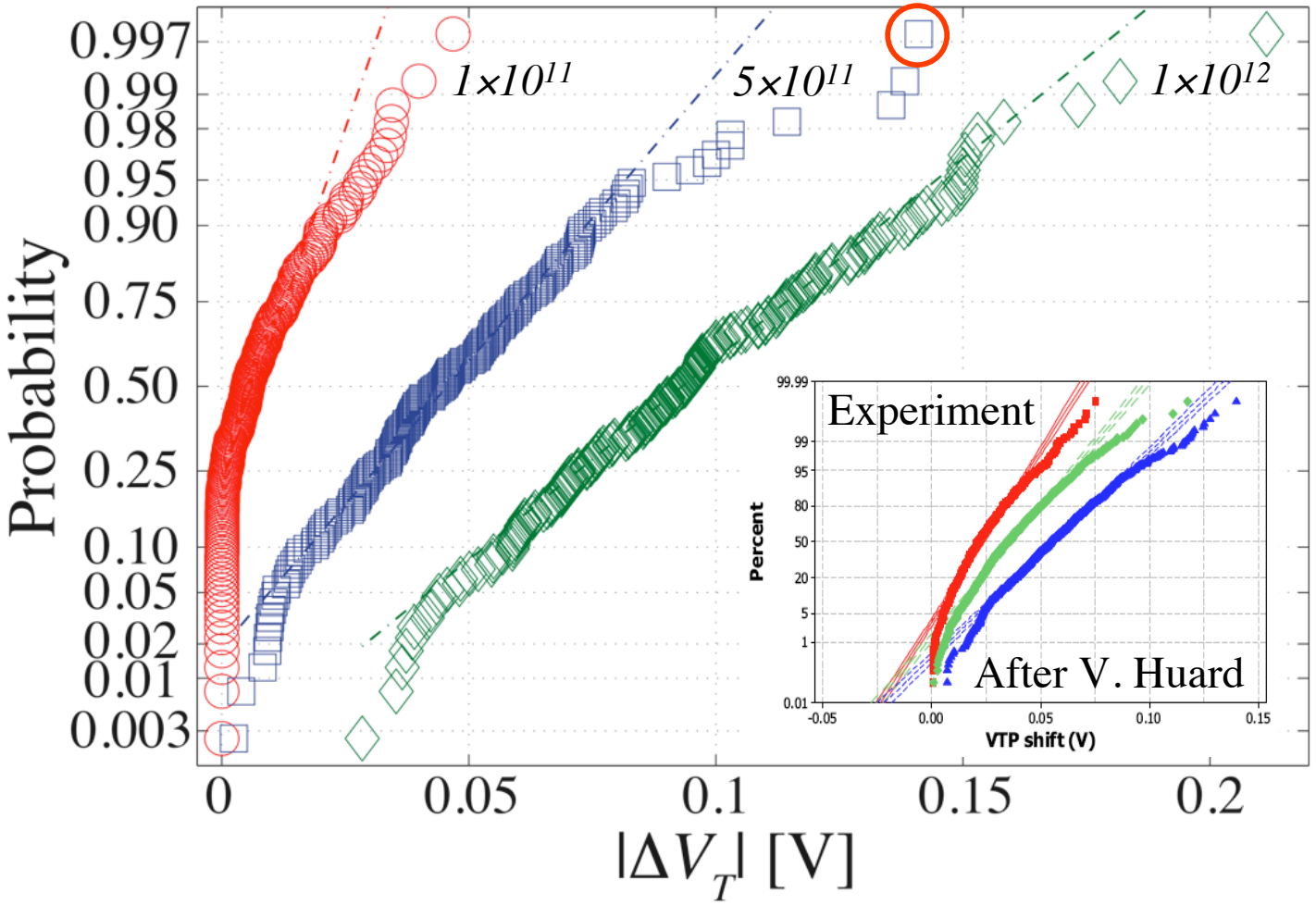




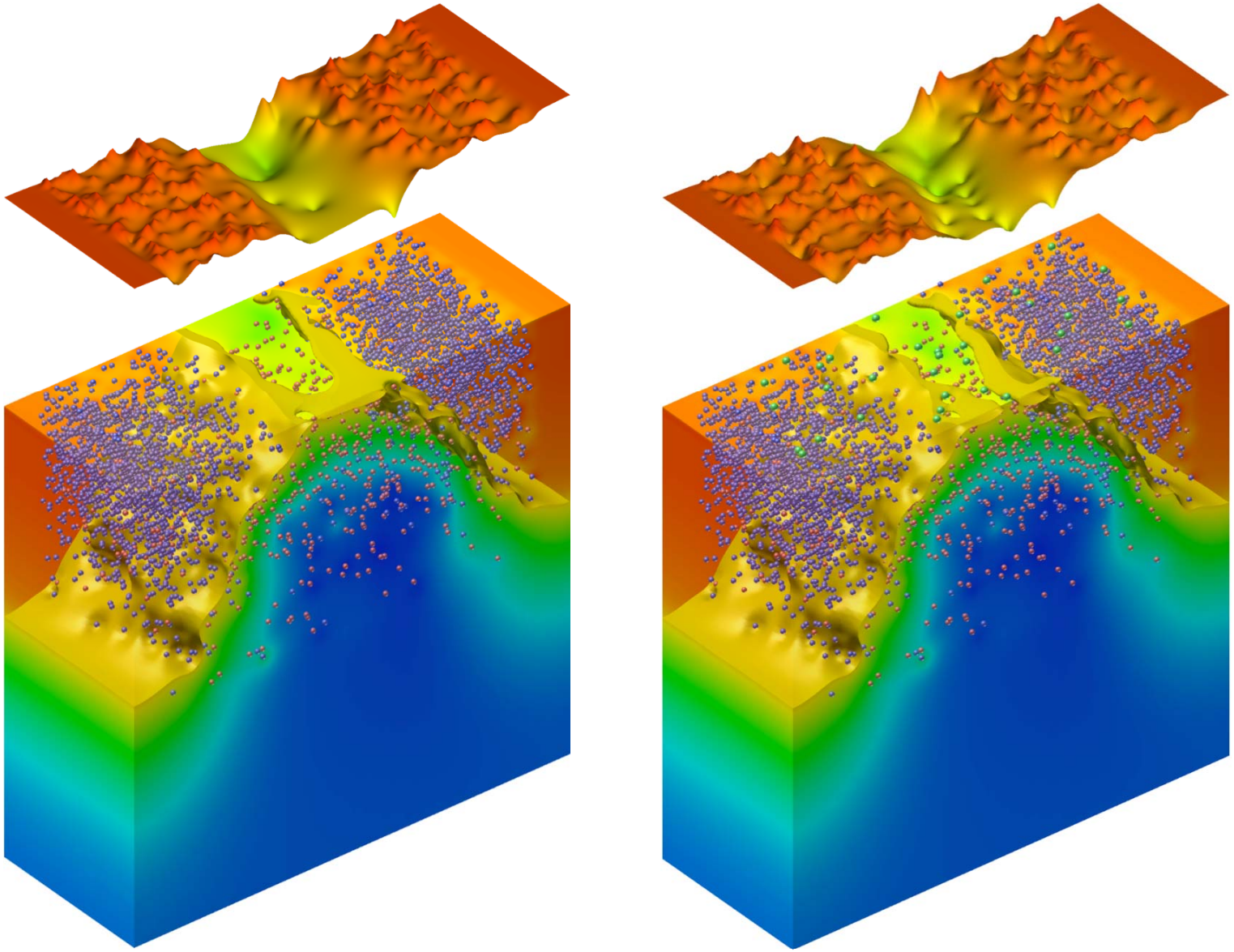
Threshold voltage variability increases with NBTI



Trapping produces ‘anomalously’ large Threshold voltage shifts

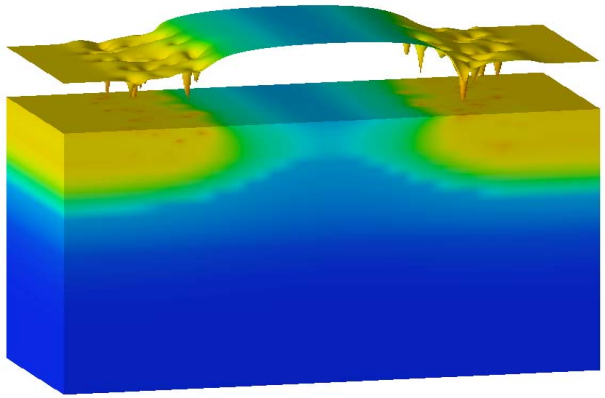


The reason for ‘anomalously’ large threshold voltage shifts

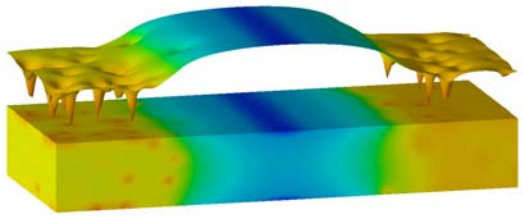


SOI and DG variability

32 nm FD SOI



22 nm DG



	32nm σV_T (mV)		22nm σV_T (mV)	
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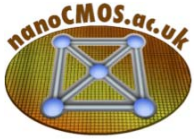
Trap (1e11)	11	11	5.1	4.8
Trap (5e11)	24	25	13	12
Trap (1e12)	36	37	18	17
Combined (1e11)	13	15	10	16
Combined (5e11)	25	27	16	19
Combined (1e12)	37	38	20	23



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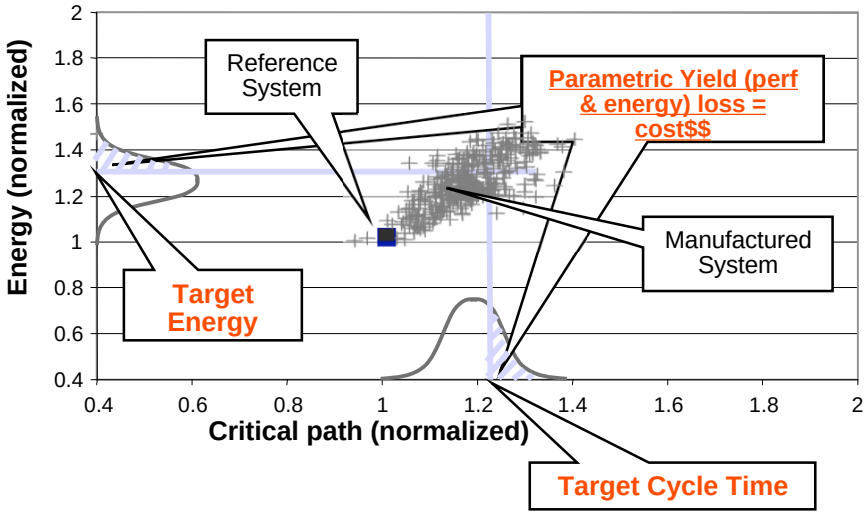
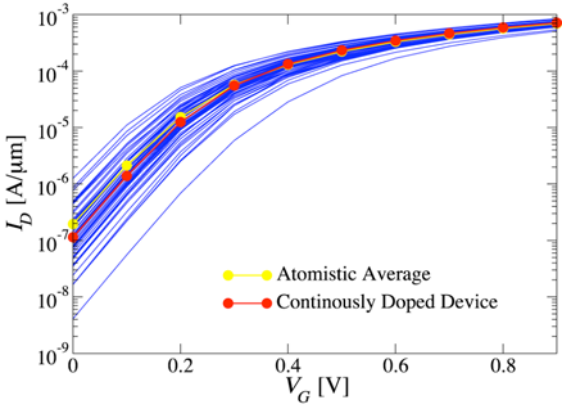
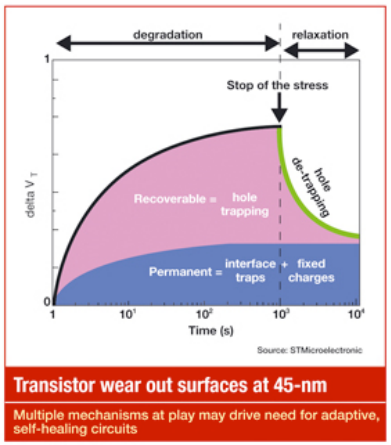
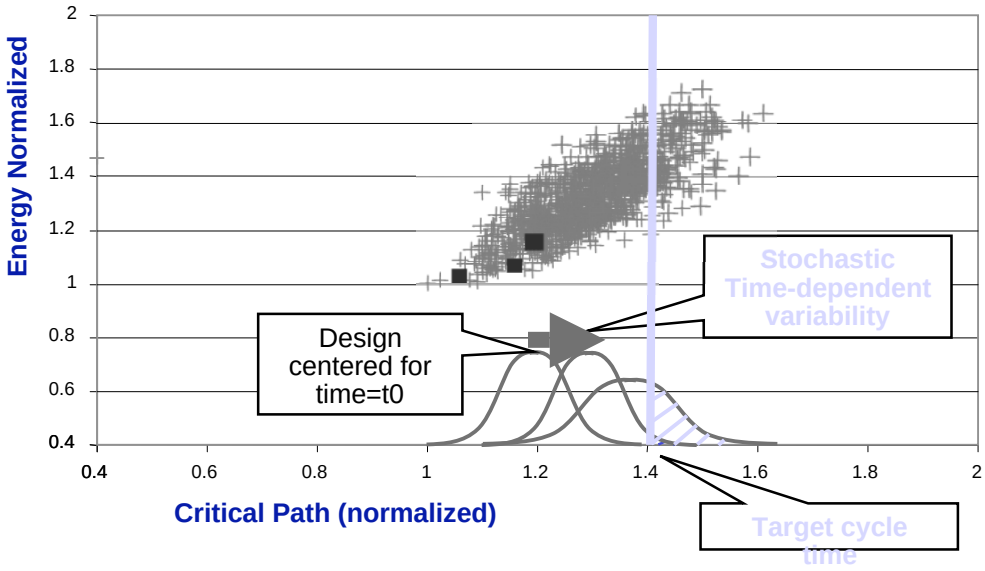
Impact of statistical variability on power, performance and yield









After M. Miranda

Conclusions

- It is likely that the statistical variability in bulk MOSFETs will increase rapidly in the next technology nodes.
- The statistical variability can not be reduced by fine tuning the technology, OPC and regular designs.
- FD SOI and DG devices have significant advantages in terms of variability compared to bulk MOSFETs.
- Statistical variability demands a statistical approach to design and will force fundamental changes in the design paradigm.

Acknowledgement to all members of the Glasgow Device Modelling Group