Managing Variability With Next Generation Design Methods and Tools

ICCV 2009

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Design to Silicon – Mentor Graphics Corporation

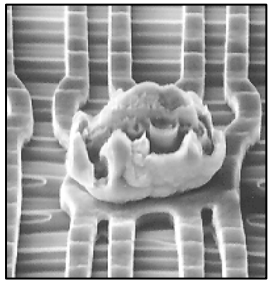
Mentor Graphics®

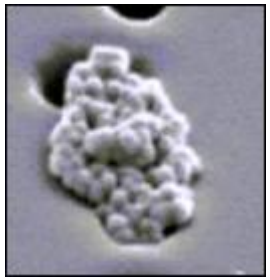
Agenda

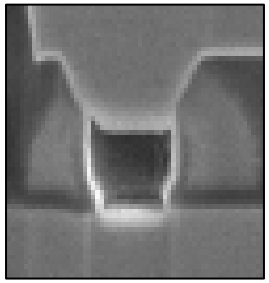
- Issues - Trends
- Current Solutions
  - Customer Case Studies
- Summary
- Q&A

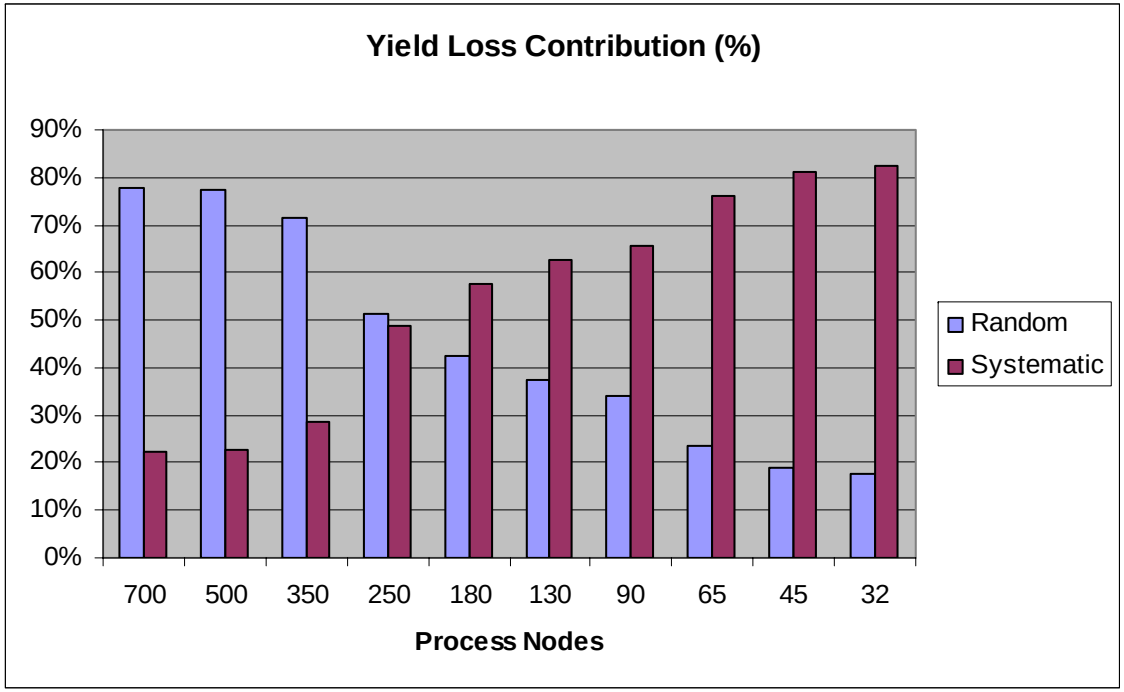
New Issues For Consideration

Random



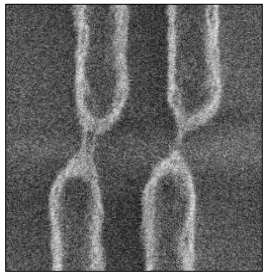


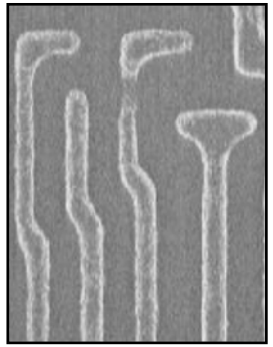


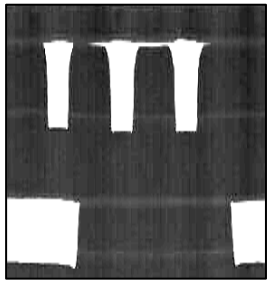


Source : Based on KLA-Tencor, ISSM 2003

Systematic







Systematic effects become more dominant

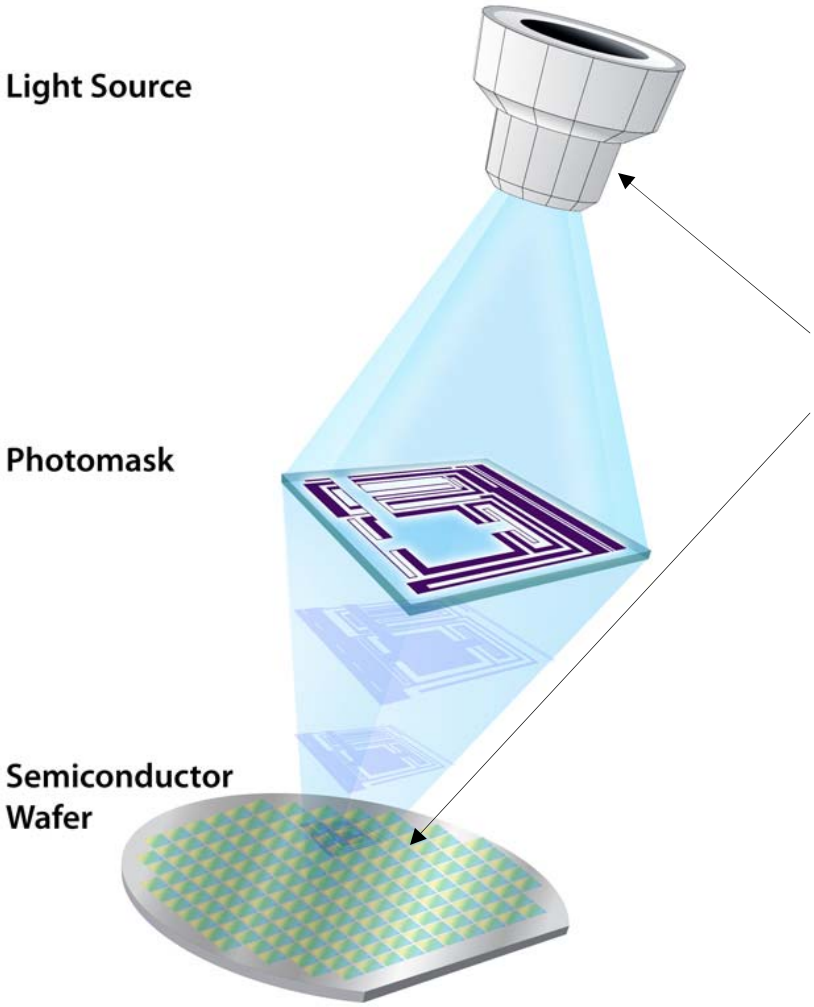
Random Versus Systematic Variability

- **Semiconductor processes are variable by nature, with some variations being random and others systematic**

- **Random:**
  - **Is statistical by nature**
  - **Is always present in the process**

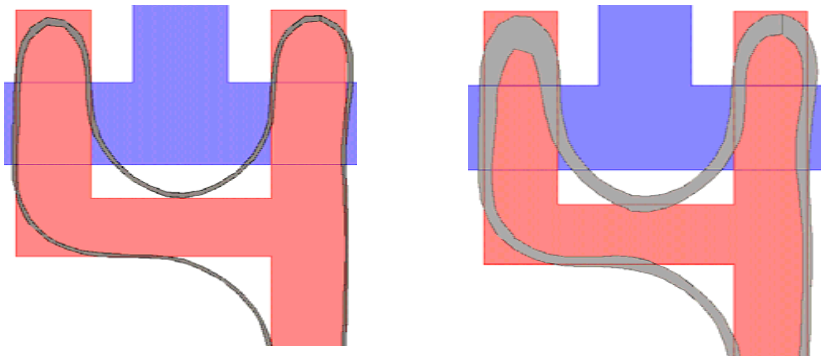
- **Systematic:**
  - **Not random, but a result of specific patterns**
  - **Is difficult to represent with a rule that covers all situations**
  - **Generally requires a model to simulate detailed manufacturing process effects**

Sources of Lithographic Variability

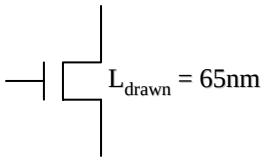


Two main sources of lithographic variability

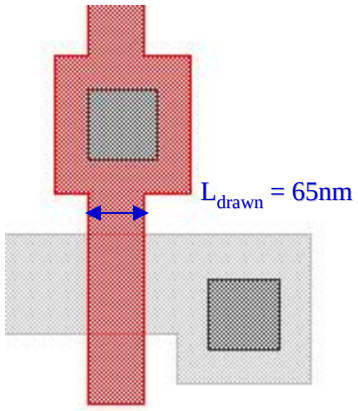
- **Dose: variation in intensity**
- **Focus: variation of wafer in z axis**



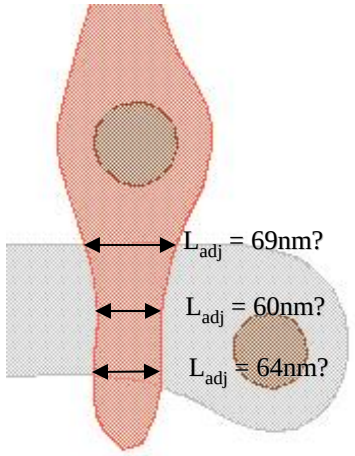
What happens to a transistor?



Schematic



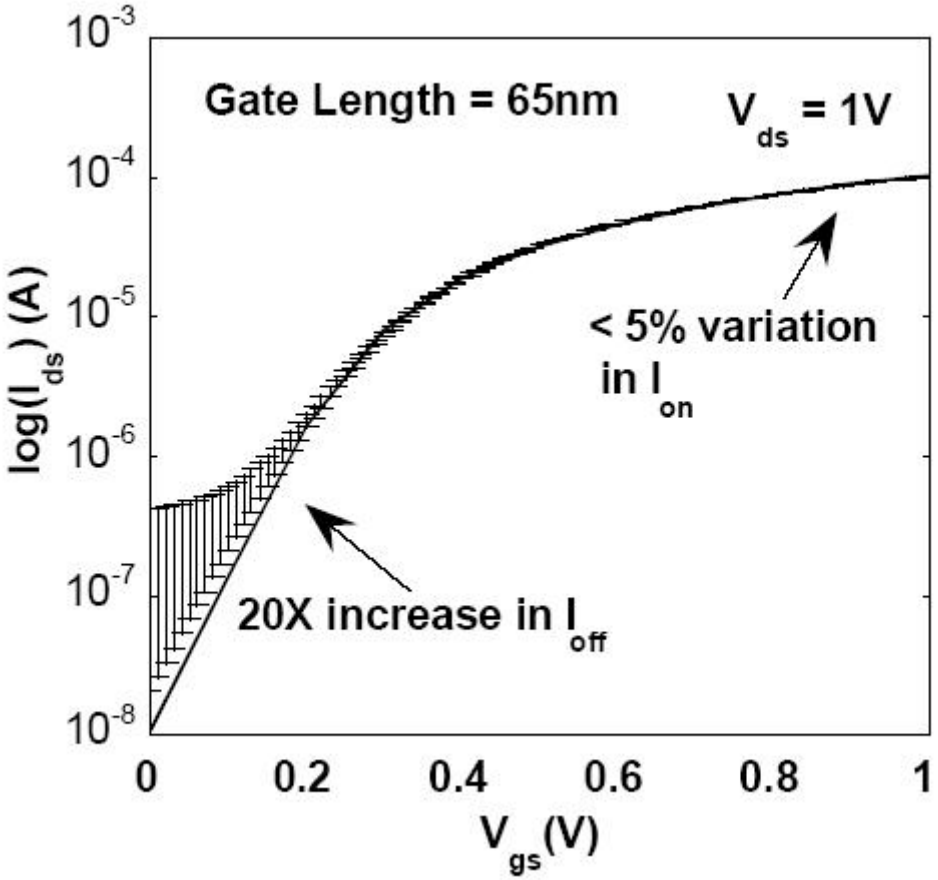
Drawn Layout



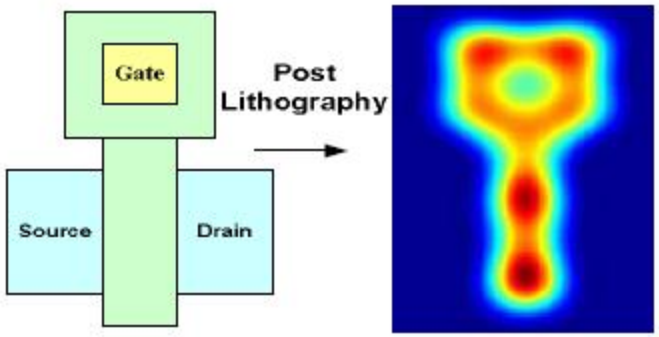
Silicon

- **Significant Gate Variability on Silicon**
- **What is the appropriate L value to use with Spice?**
- **Is this variability insignificant that we can ignore?**

Effect of Non-Rectangular gate

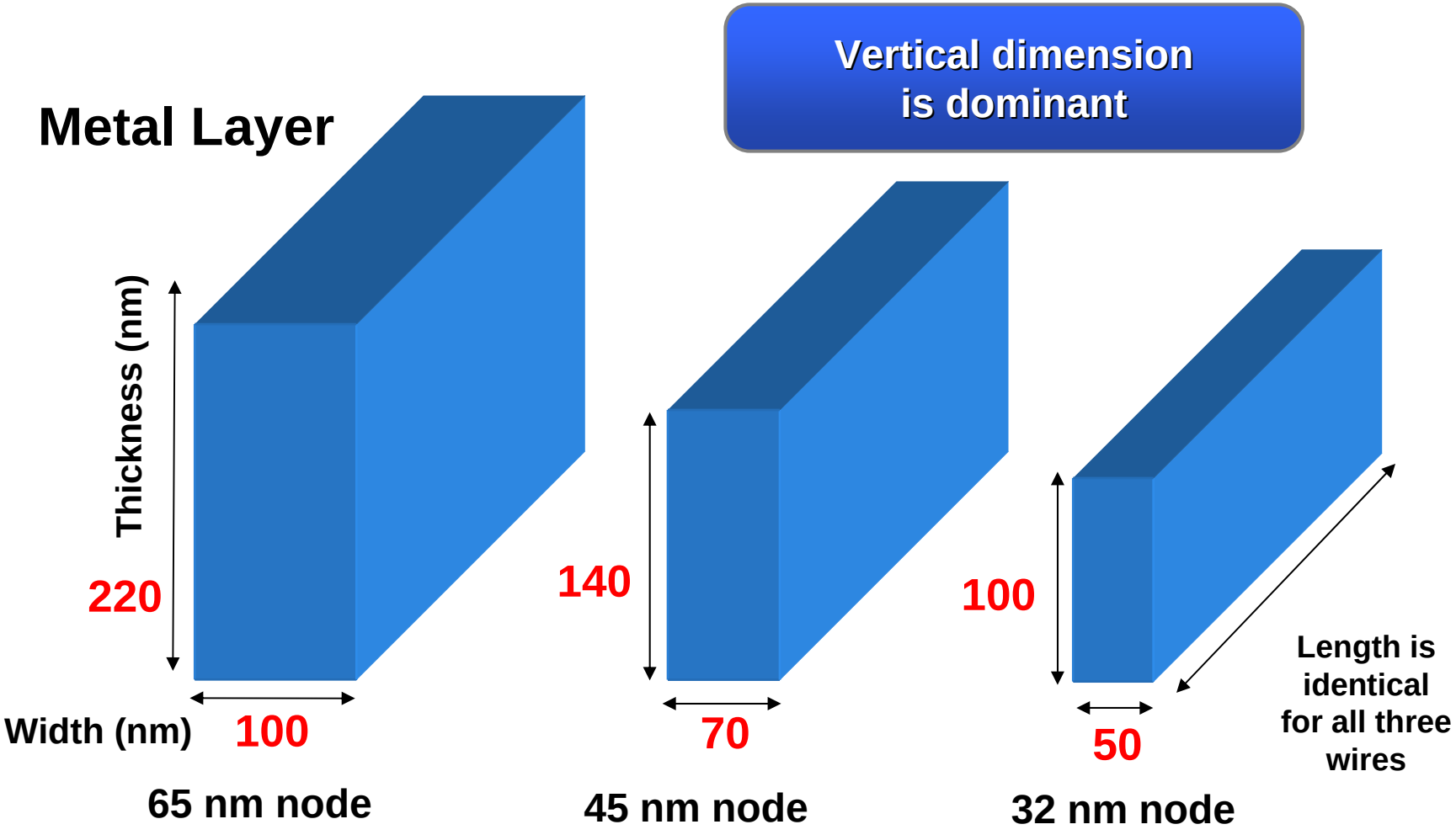


- **Impact of Non-rectangular gate effect in leakage current for 65nm technology node.**



Ritu Singhal, et. al "Modeling and Analysis of Non-rectangular Gate for Post-Lithography Circuit Simulation" DAC 2007 proceedings

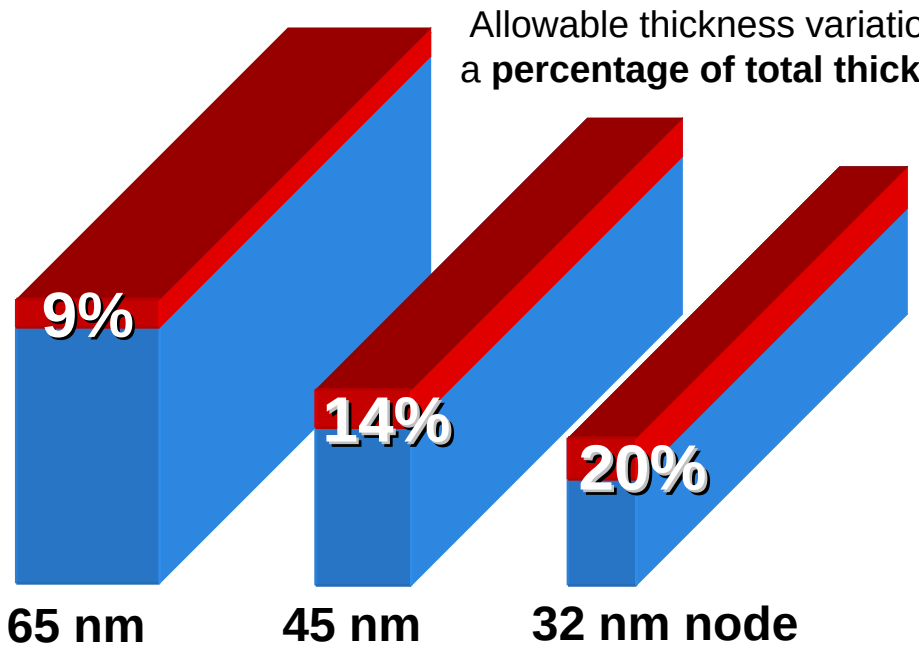
Process Trends Impacting CMP Sensitivity



Source : ITRS Roadmap

Impact of Thickness Variation

Allowable thickness variation has remained **constant** at +/-10 nm



Thickness variations translate to resistance variations

	90nm	65nm	45nm	32nm
Resistance +/- %				
M1	**6**	**8**	**12**	**18**
MX	**4**	**7**	**11**	**17**

Source : ITRS Roadmap

Percentage of total thickness variability has INCREASED at each node…CMP variation is now an issue requiring analysis

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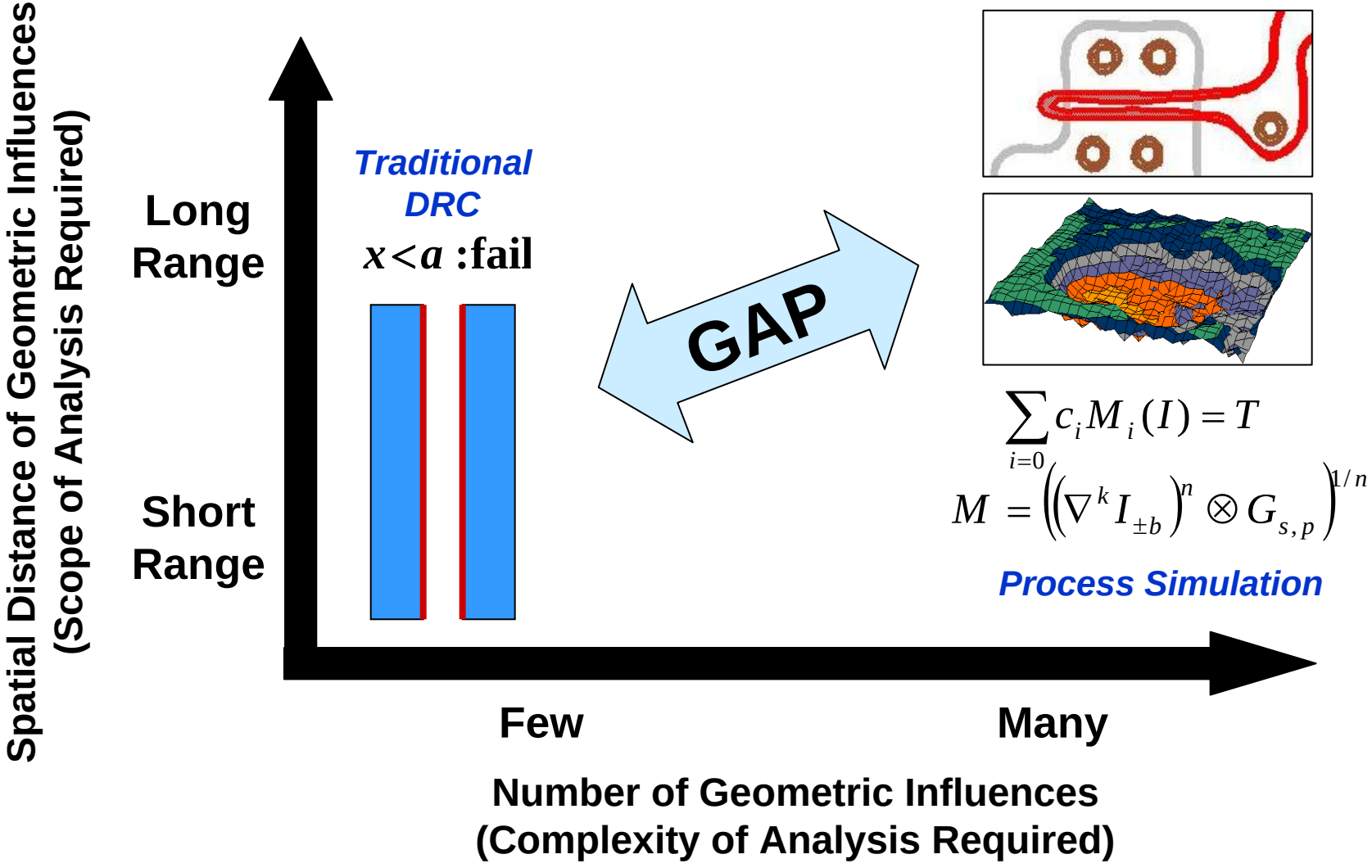
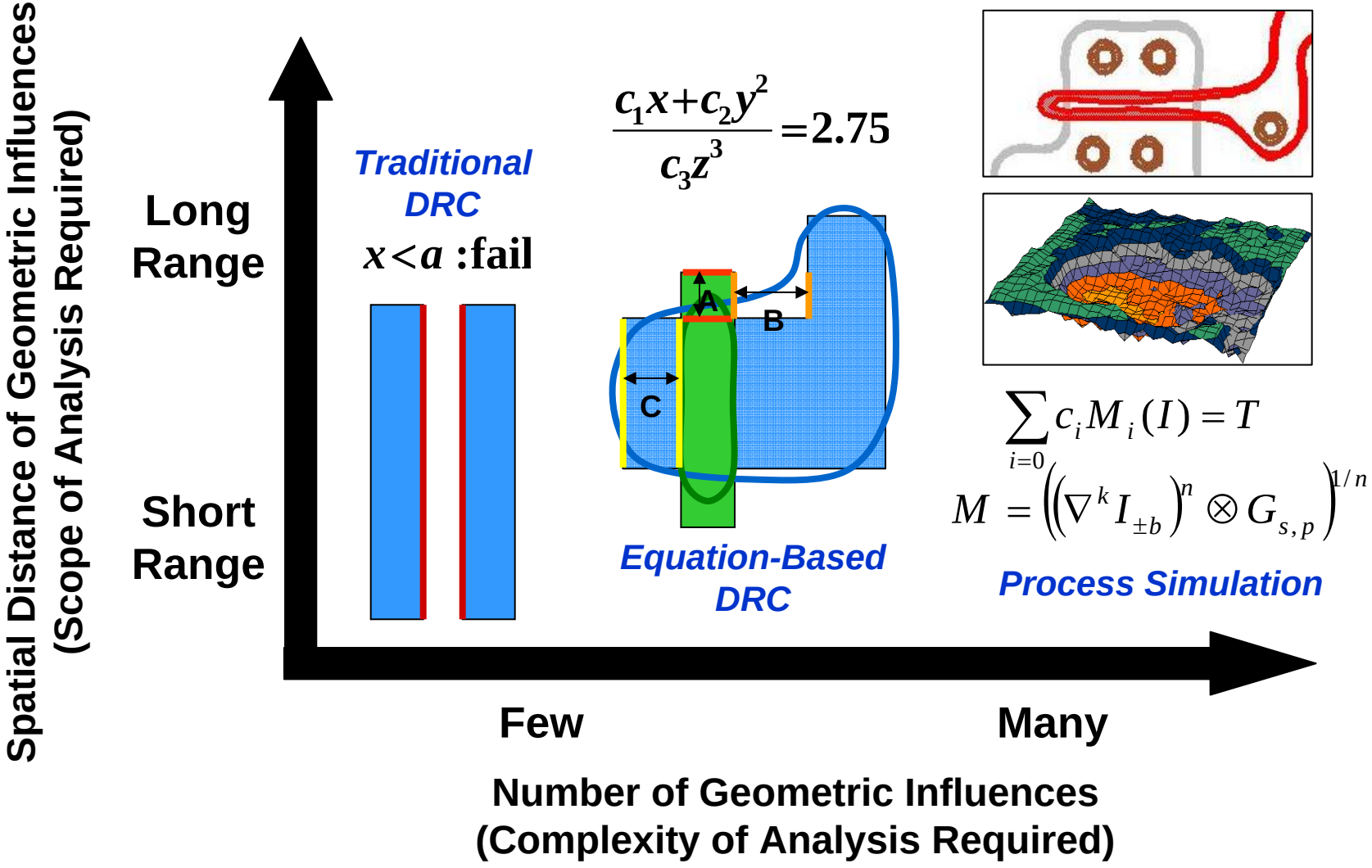
Physical Verification Solution Space

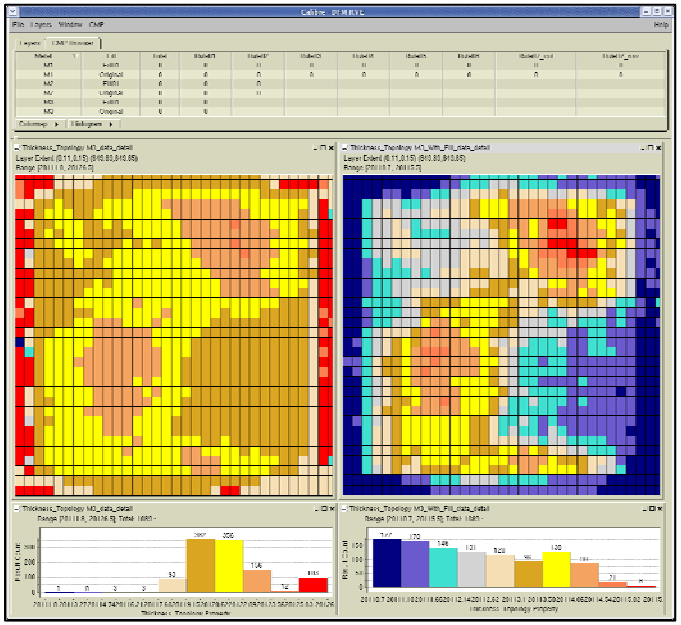


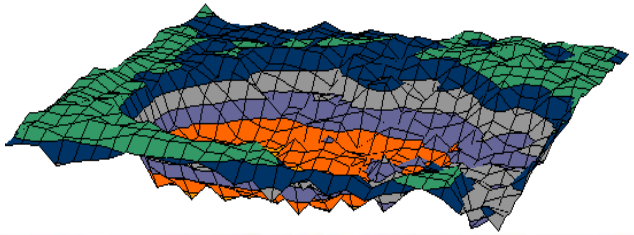
Equation-Based DRC Solution Filling the Gap



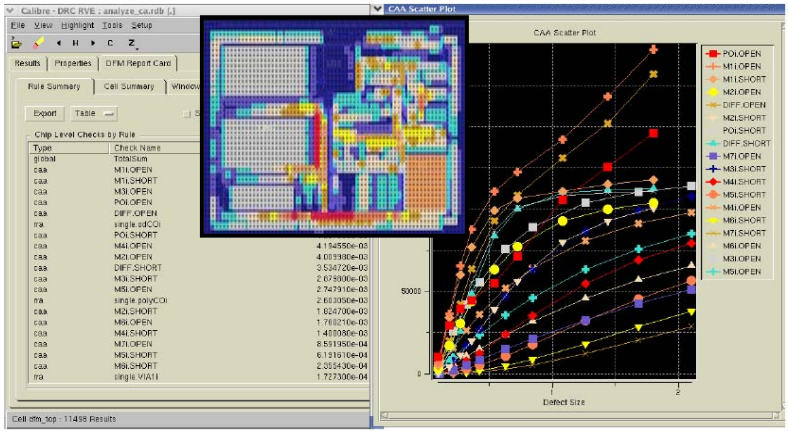
Model Based DFM

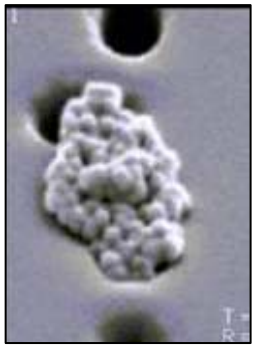
Calibre YieldEnhancer
Next Generation Fill-SmartFill
Calibre CMPAnalyzer
CMP Process Simulation



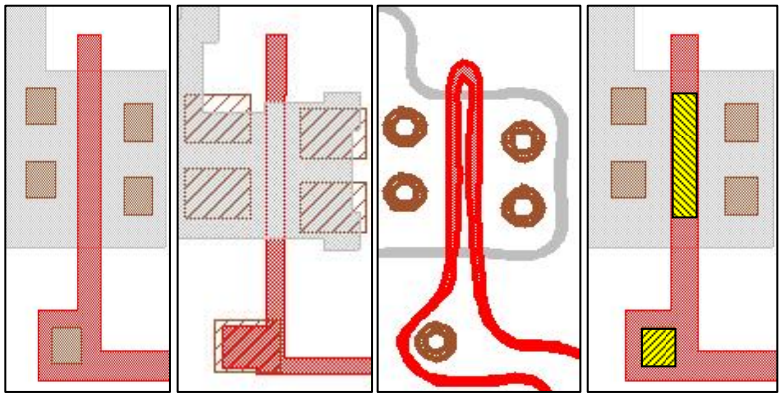


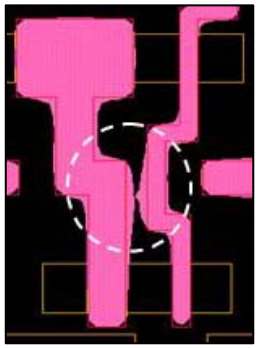
Calibre YieldAnalyzer
Critical Area Defect Simulation



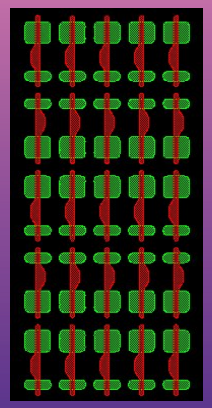


Calibre Litho Friendly Design
Litho Process Simulation





Result of collaboration with ARM at 65nm

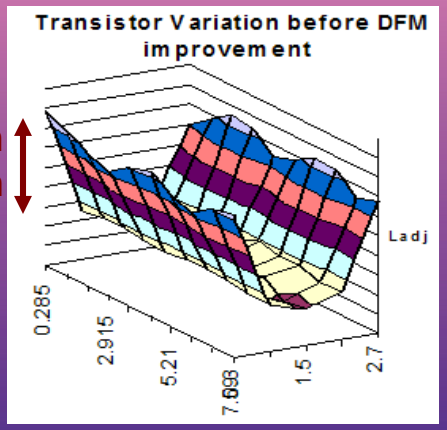


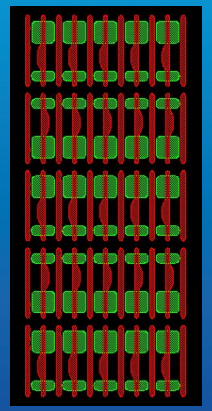
Original ARM Cell - 65nm LP Chartered
NO Context-Sensitivity Improvement

Use Calibre LFD to analyze layout context dependency

Measuring L variations across process windows and location

5nm Variation

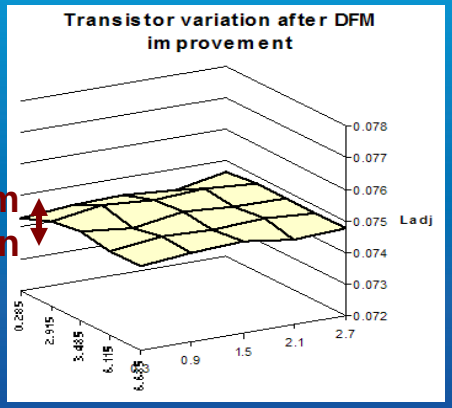




Modified ARM Cell - 65nm LP Chartered
Presented at SPIE 07

Cell is context independent and robust across process windows

<0.5nm Variation



Success Story : Infineon using LFD

- LFD methodologies applied to library cells
- Using Chartered 65nm LFD Kit

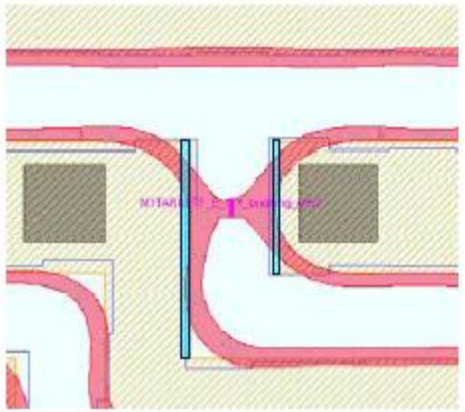


Fig. 8. The PV bands simulated for the post-OPC layout of the original design show a short.

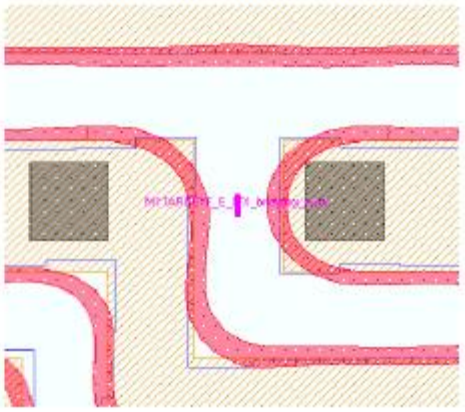


Fig. 9. Removing a 5 nm stripe on each side of the relevant gap (compare Fig. 8) eliminates the short.

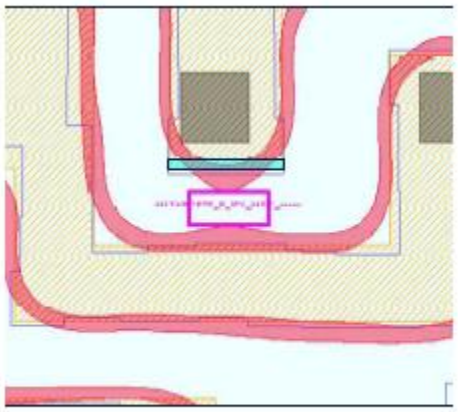


Fig. 10. Regular PV bands simulated for the post-OPC layout of the original design show a spacing violation.

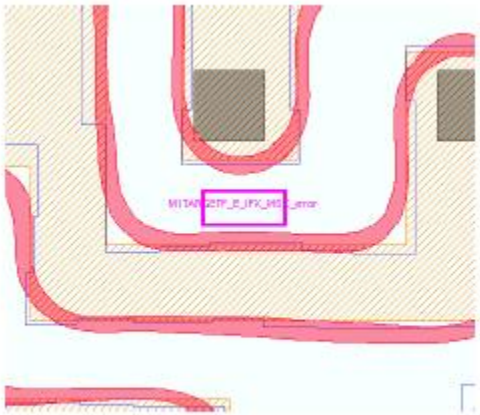
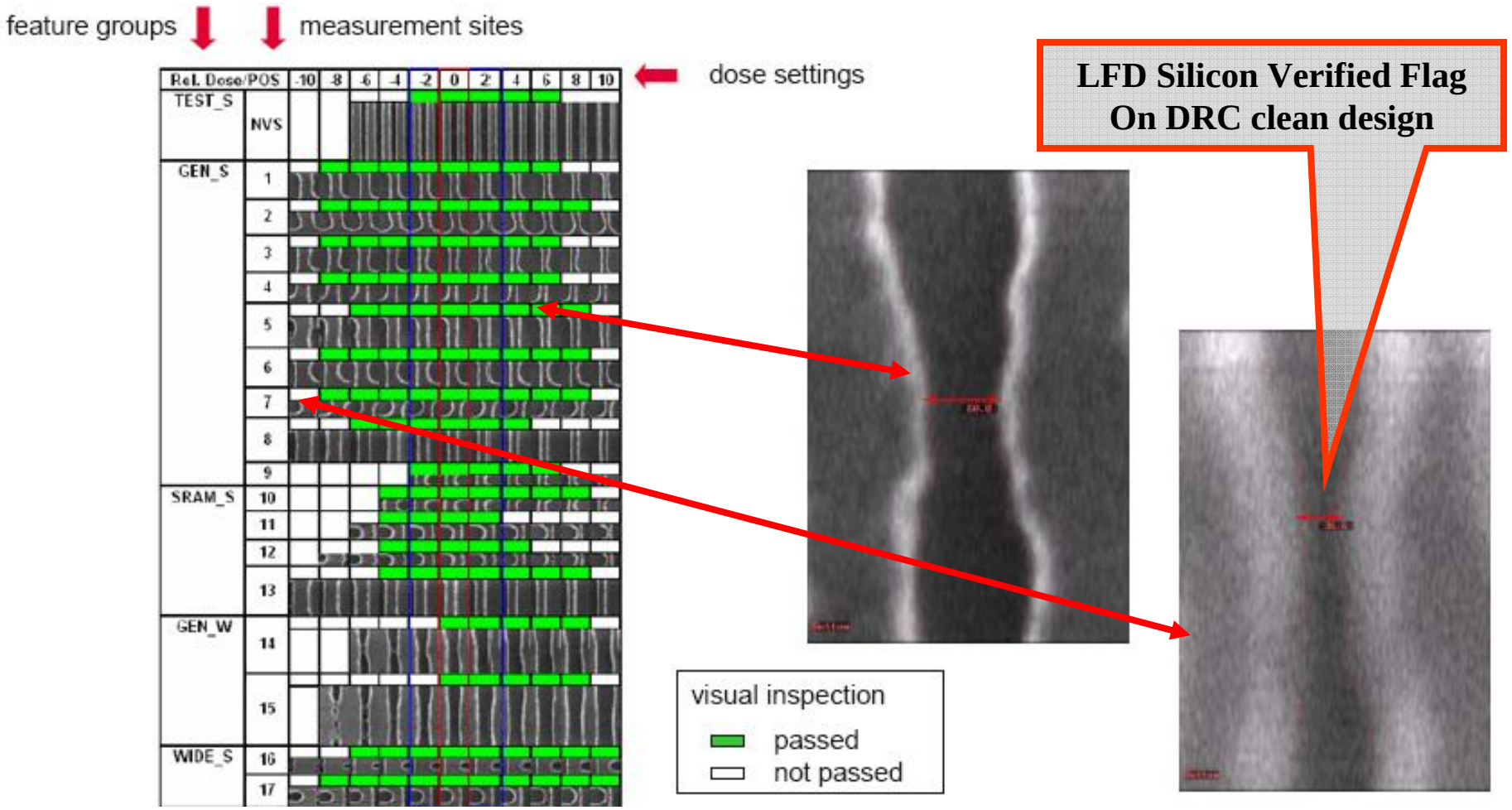


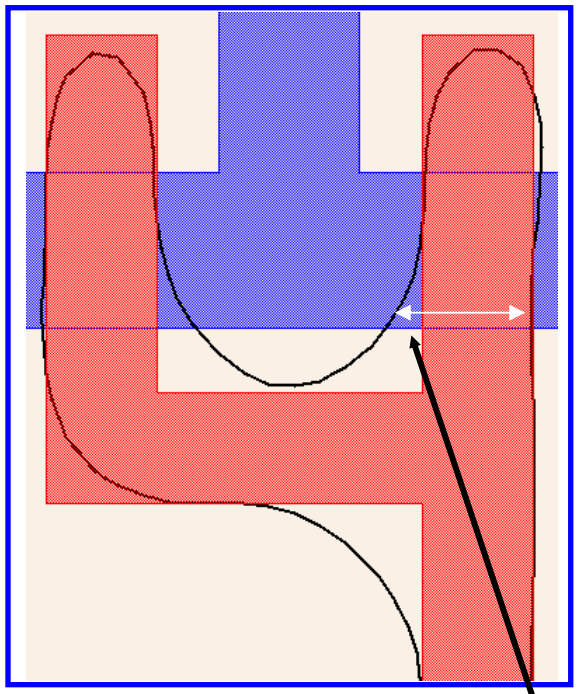
Fig. 11. Removing a 10 nm stripe at the line end (compare Fig. 8) eliminates the violation.

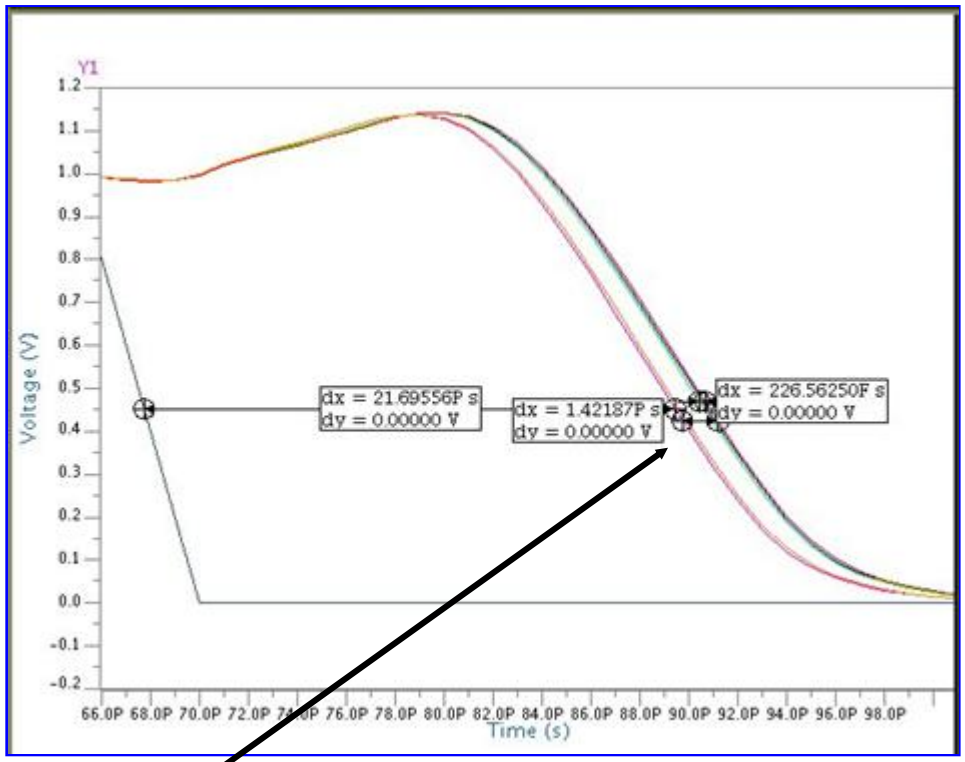
Examples of local Fixing of LFD violations

Success Story : Infineon using LFD



Timing/Power Simulation Matching Silicon

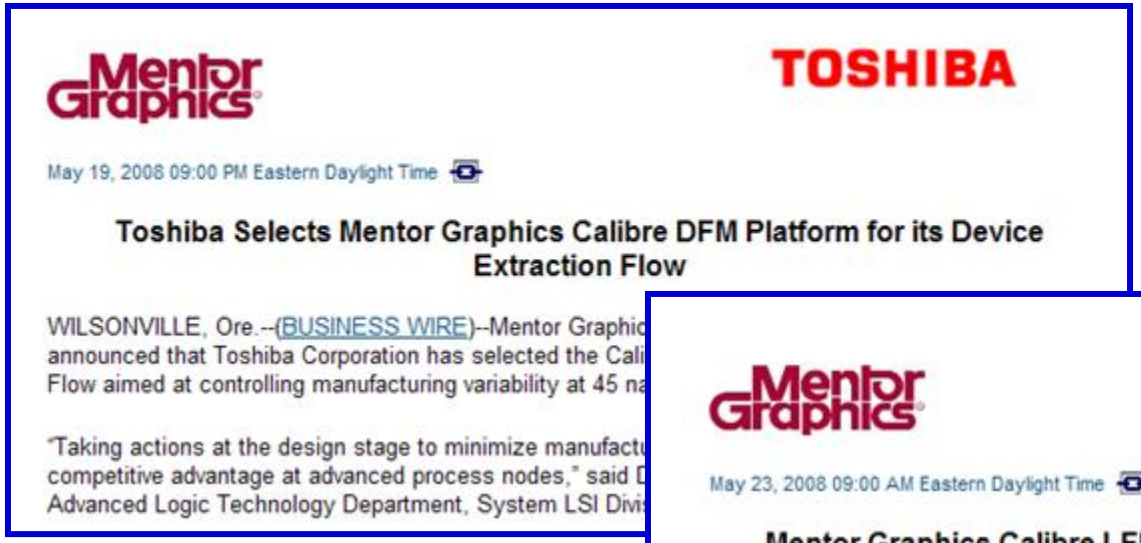




Delta Between

Drawn and Silicon

LFD(CSG)-LVS Customer Adoption



May 19, 2008 09:00 PM Eastern Daylight Time

Toshiba Selects Mentor Graphics Calibre DFM Platform for its Device Extraction Flow

WILSONVILLE, Ore.--(BUSINESS WIRE)--Mentor Graphic
announced that Toshiba Corporation has selected the Cali
Flow aimed at controlling manufacturing variability at 45 na

"Taking actions at the design stage to minimize manufactu
competitive advantage at advanced process nodes," said D
Advanced Logic Technology Department, System LSI Divi

May 23, 2008 09:00 AM Eastern Daylight Time

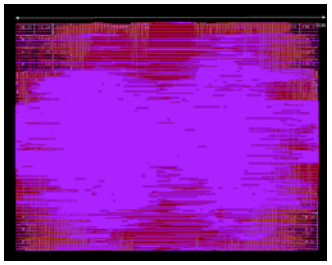
Mentor Graphics Calibre LFD Selected by STMicroelectronics for Litho Variability Analysis at 65 and 45 Nanometers

WILSONVILLE, Ore.--(BUSINESS WIRE)--Mentor Graphics Corporation (Nasdaq: MENT) today announced that STMicroelectronics has selected the Mentor Graphics Calibre® DFM (design for manufacturing) platform with the Calibre LFD™ (Litho-Friendly-Design) system for its Litho Variability Analysis solution aimed at controlling manufacturing variability at 65 nanometer (nm) and beyond. The announcement follows an extensive evaluation of commercially available solutions by STMicroelectronics based on accuracy, speed and ability to integrate with existing design flows. This decision builds on the existing relationship between STMicroelectronics and Mentor, which started with the use of Calibre OPC tools at 130nm, and has continued for all following nodes, including 45nm.

"To analyze variability effectively, the process models need to be very accurate. The models used by the Calibre LFD solution have been measured and proven accurate on silicon for 65nm and 45nm generations," said Joel Hartmann, Silicon Technology Development Director at STMicroelectronics. "In addition, the Calibre solution reduces it cycle to re-calibrate the models when parameters change during

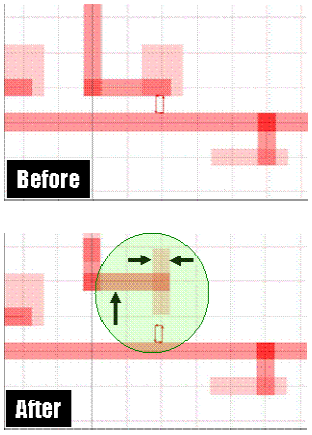
Systematic Solution to Control Variability

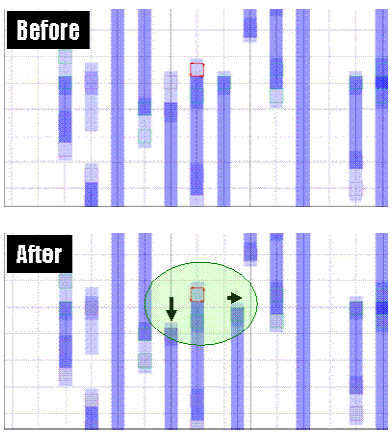
Available Solution
Olympus-LFD Integration



Design Characteristics

Area: 2.1mm x 1.6mm
Utilization: 58.91%

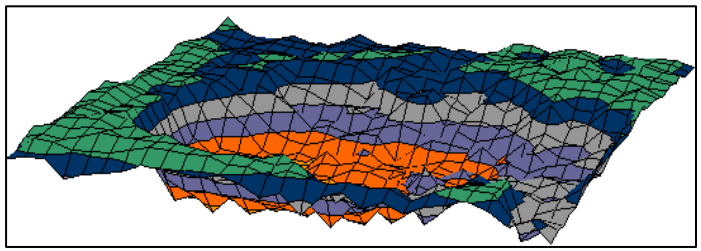




Litho Yield Issues are being addressed automatically within the P&R Platform

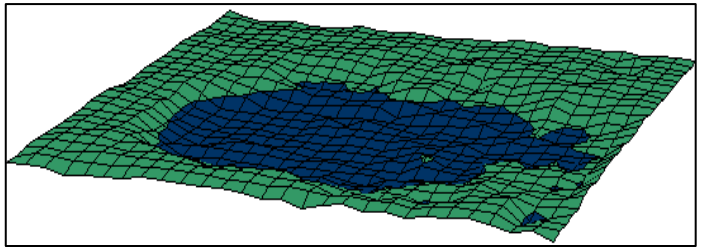
CMP and Fill

CMP Simulation and Advanced Fill Working together



Design Pre-Filling

Thickness Variation is High
Not a good situation

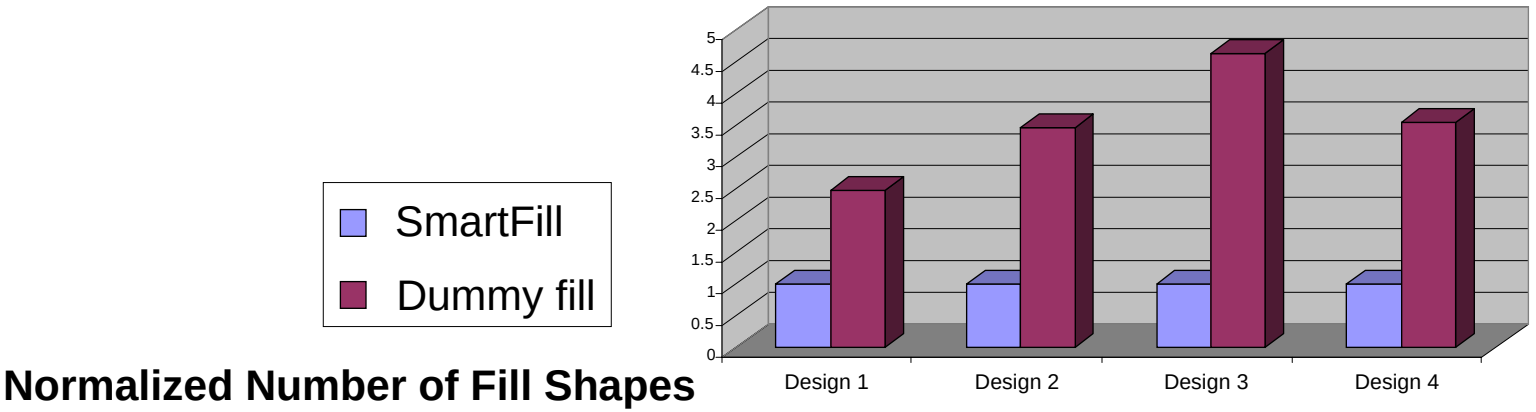


Design Post-Filling

Design is Flat (3D)
Very good situation

SmartFill reduces the amount of fill added

- **Combining analysis with filling operation to reducing the amount of fill added**
  - **Avoiding overfilling**
  - **Considers multiple design objectives**
  - **Stops as soon as design objectives are reached**



Thank You