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Variability Characterization Infrastructure for Nanometer Scale Technologies

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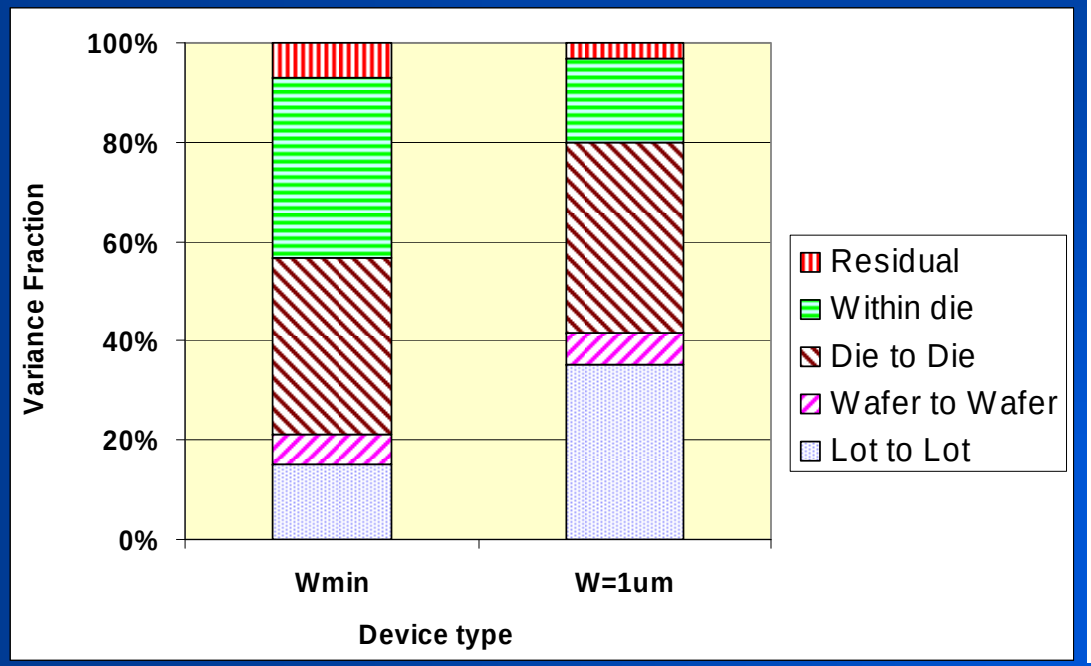
Outline

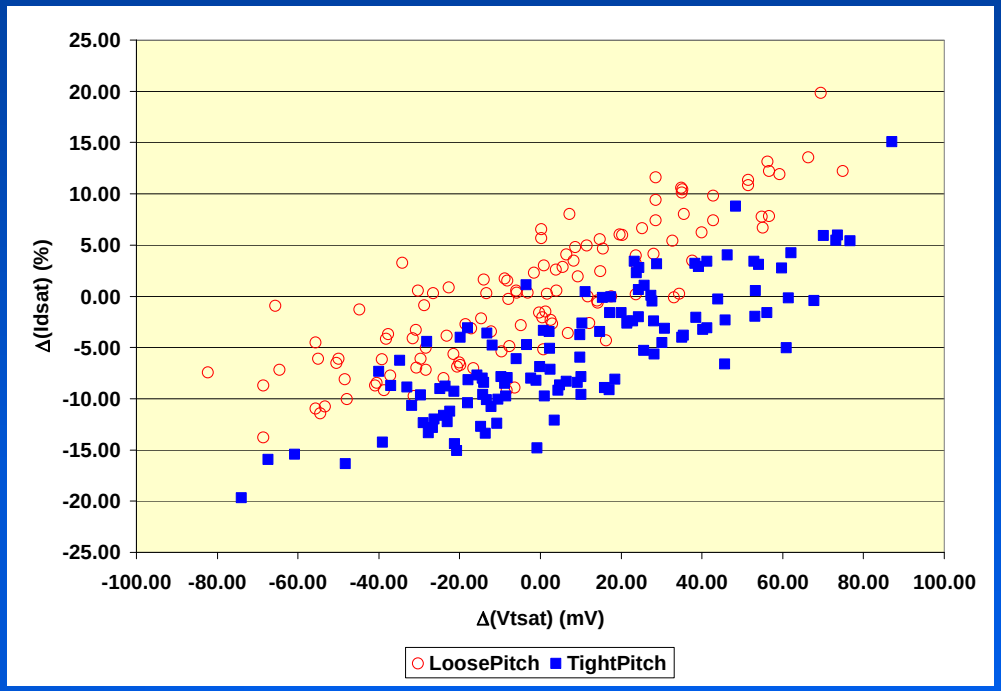
- **Sources of Variation**
- **Components of Variability Characterization Infrastructure**
  - Test structures
  - Fast and efficient testing
  - Data Analysis
  - Modeling and design enablement
- **Sample Results & Applications**

Sources of variation

Decomposition of random variation

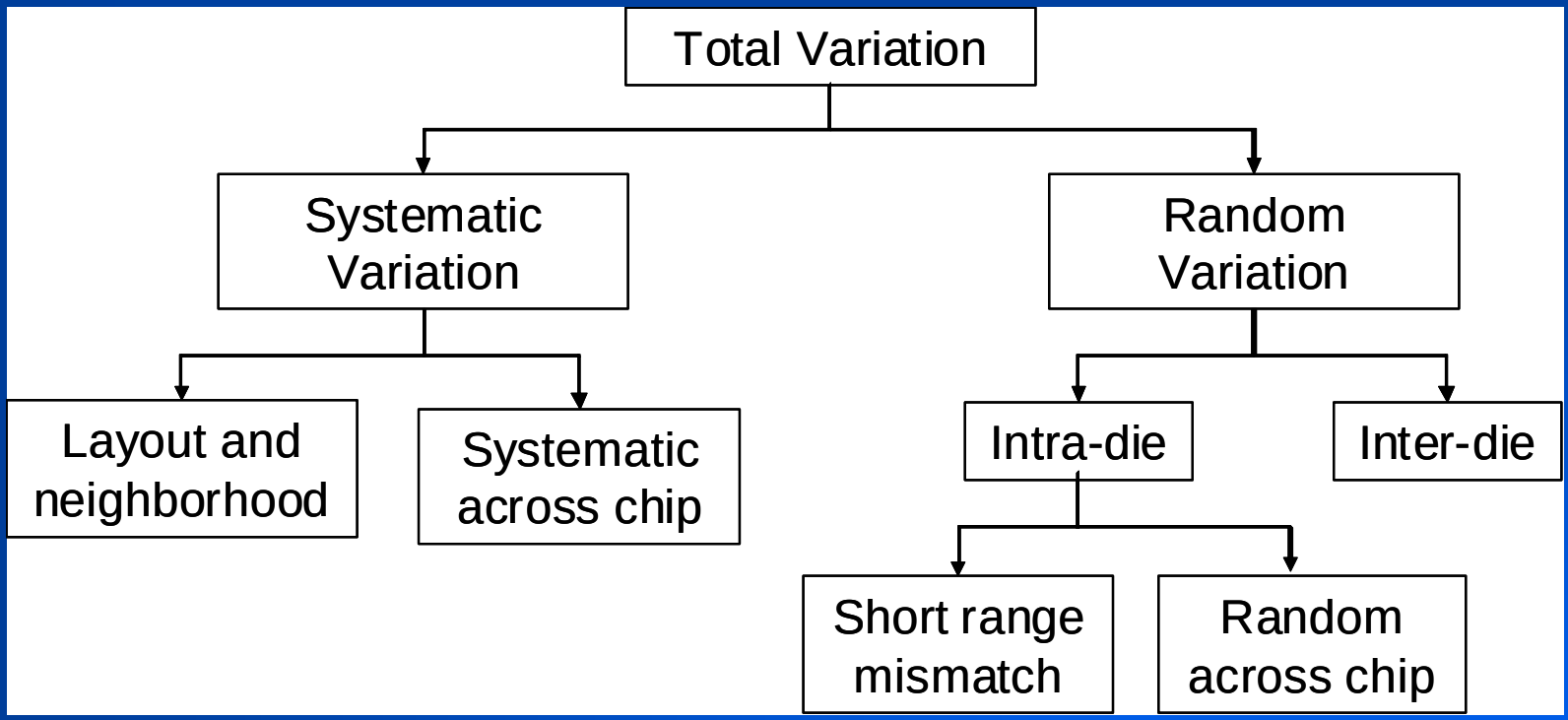


Variation from layout effects



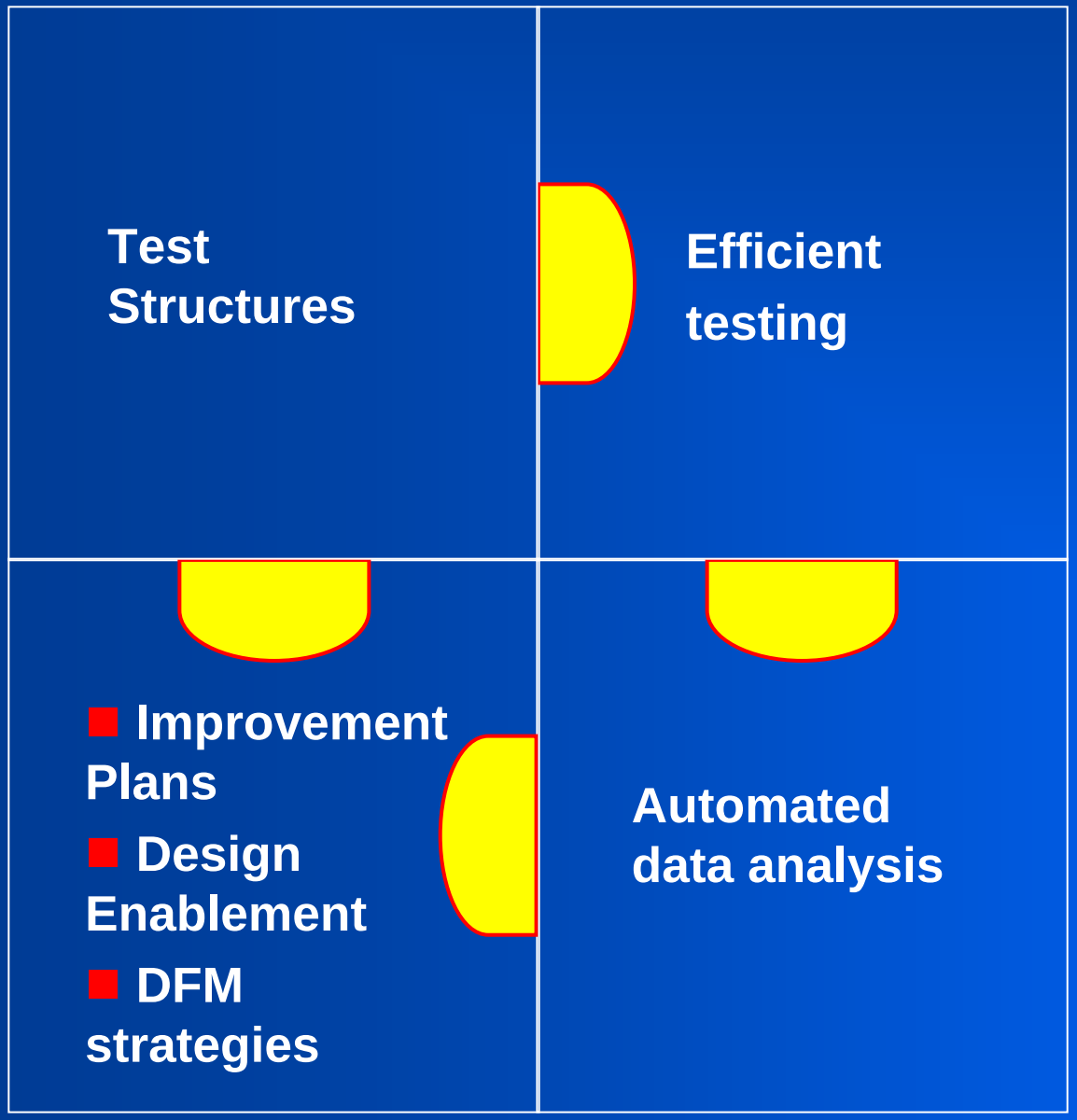
- Many different sources of variation
- Minimizing variability and mitigating its impact requires accurate and efficient characterization of all sources of variation

Classification of Variance



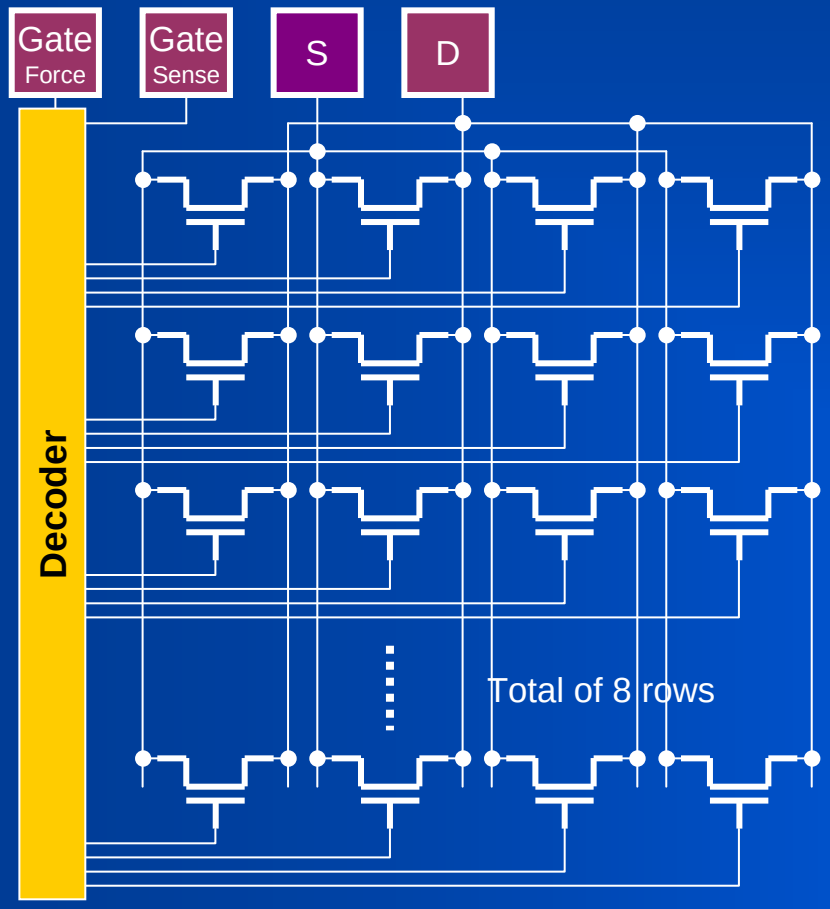
- **Random: variation in characteristics of devices with identical layout and neighborhood**
  - RDF, LER, Across-chip variation, die-to-die variation
- **Systematic: variation in characteristics of devices with identical dimensions (W, L)**
  - Layout and neighborhood effects, deterministic process gradients

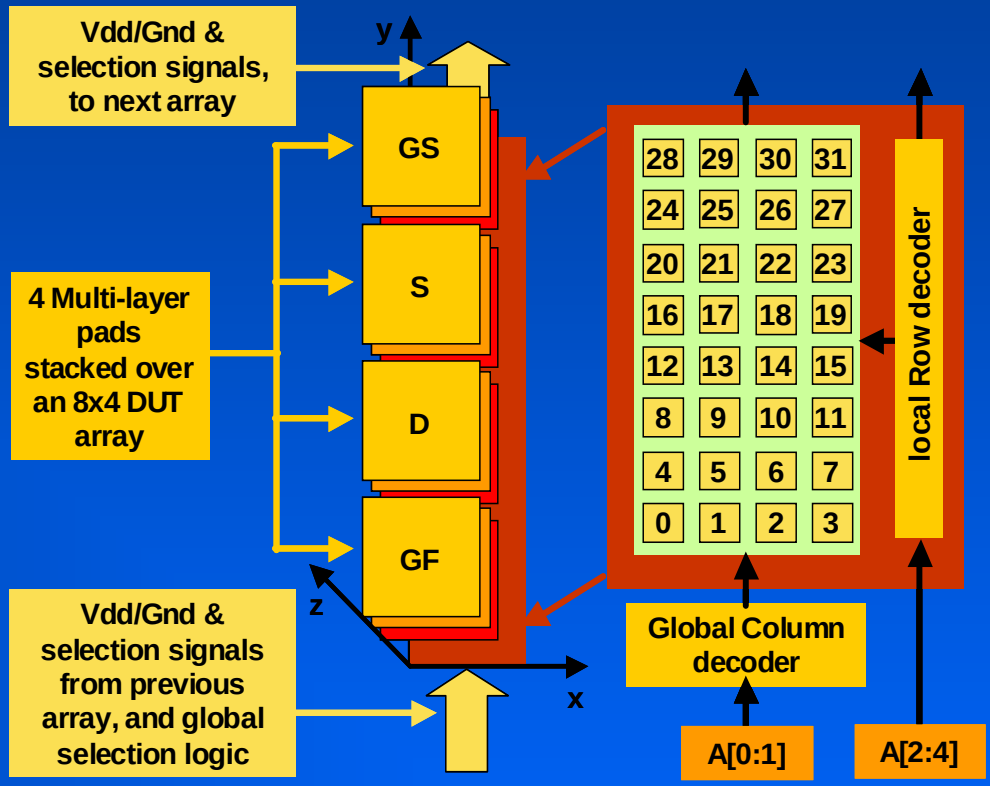
Infrastructure Components



- **Integrated Infrastructure:**
  - Generate
  - Test
  - Manage& analyze
  - Model and apply characterization data

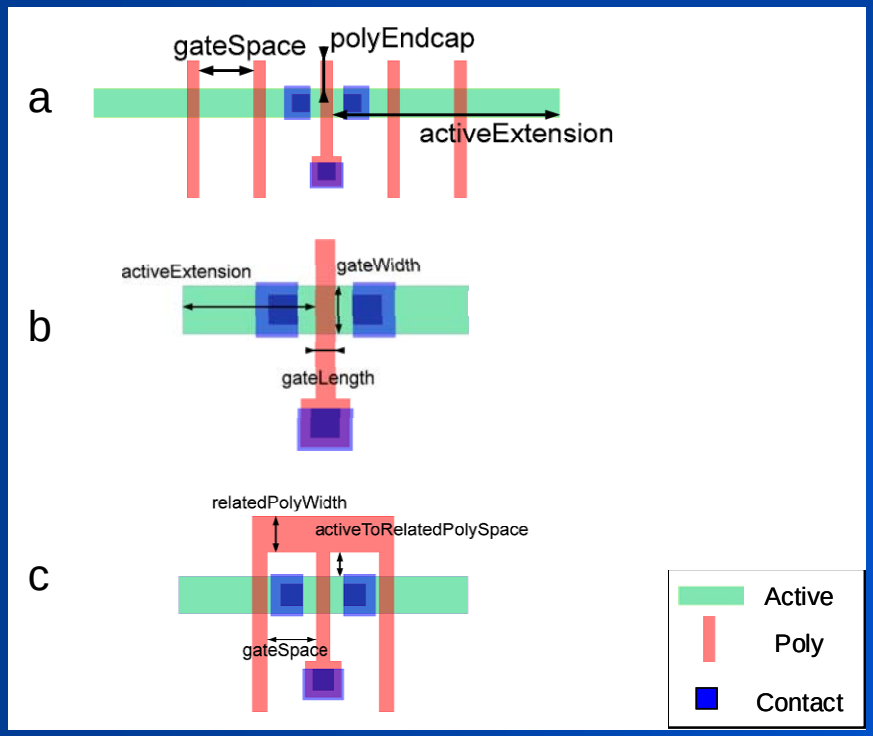
Test Structures (1)

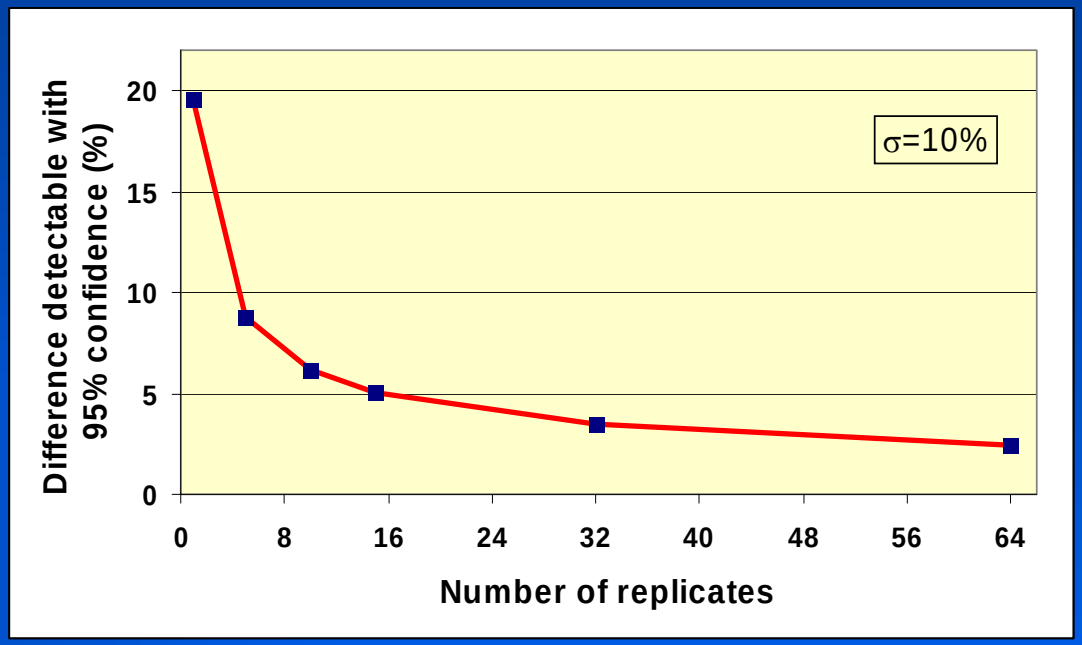




- **Multiplexed arrays provide pad-efficient test-structures**
  - Large number of replicates or layout experiments
- **Array can be placed below pads for even more area-efficiency**
  - Scribe-line applications

Test Structures (2): Experiments

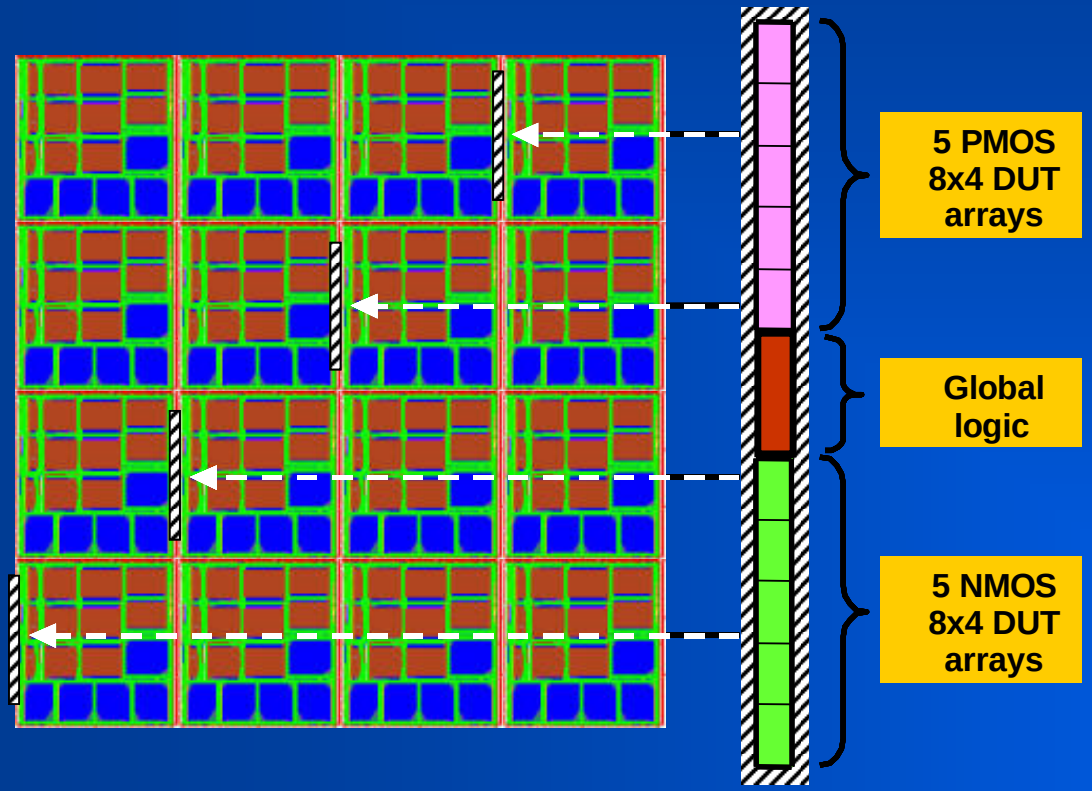




- **Different sizes, layout styles and neighborhood**
- **Characterize systematic variability from layout**

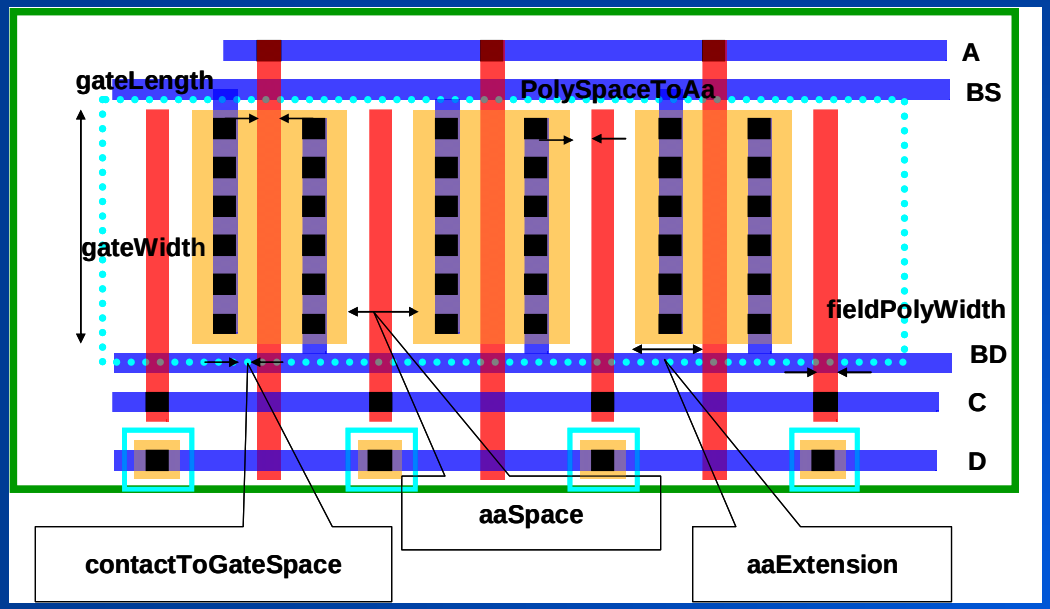
- **Large number of replicates**
  - Detect systematic differences in presence of variability
  - Variance decomposition

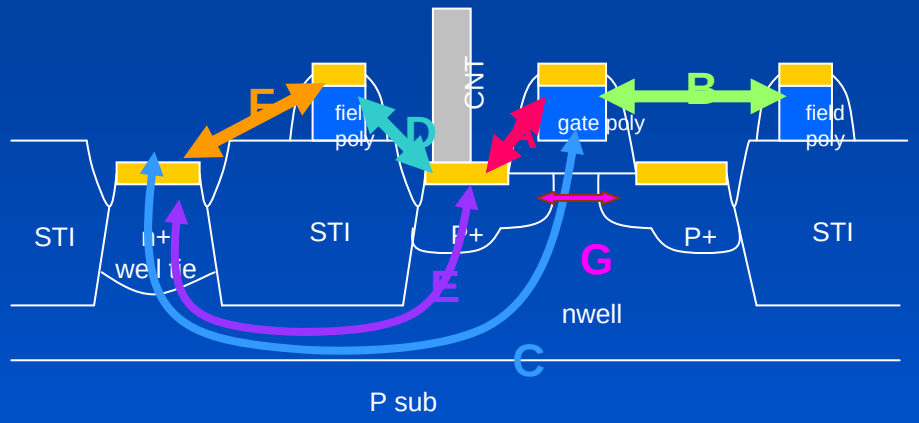
Test Structures (3): Placement



- **Scribe-line placement on products**
  - Yield ramp and production monitoring
- **Across-chip placement**
  - ACV effects
  - Technology development and characterization

Test Structures (4): Leakage Arrays





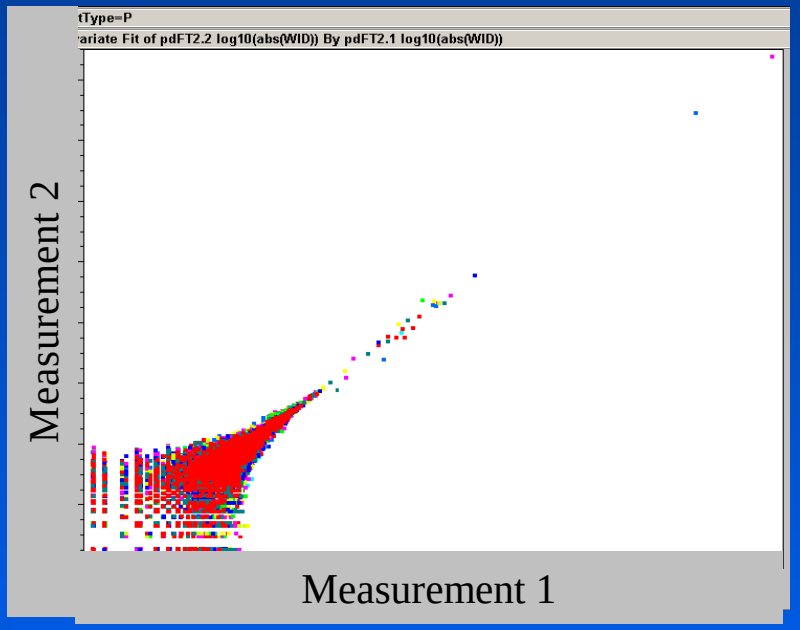
- **Large number of parallel structures for leakage characterization**
  - Experiments on layout and neighborhood
- **Many leakage paths**
  - All need to be characterized and understood
  - Trade-off between leakage and variability

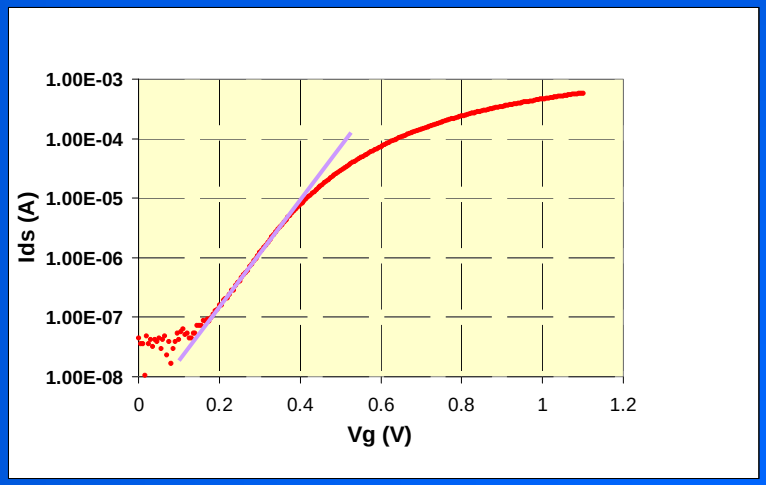
Fast Testing

- **Variability characterization ➔ large sample sizes, multiple placement, many experiments**
- **How can all the measurements be made in reasonable time?**
- **Parallel testing: many devices at the same time**
- **Low-resolution “inexpensive” measurement units**
- **Co-optimization of test-structures and testing**
  - E.g. pdFastTest-II, pdFastTest-III
  - 72 analog test channels
  - > 60X improvement in test speed
- **Recently extended to include Ioff (source)**

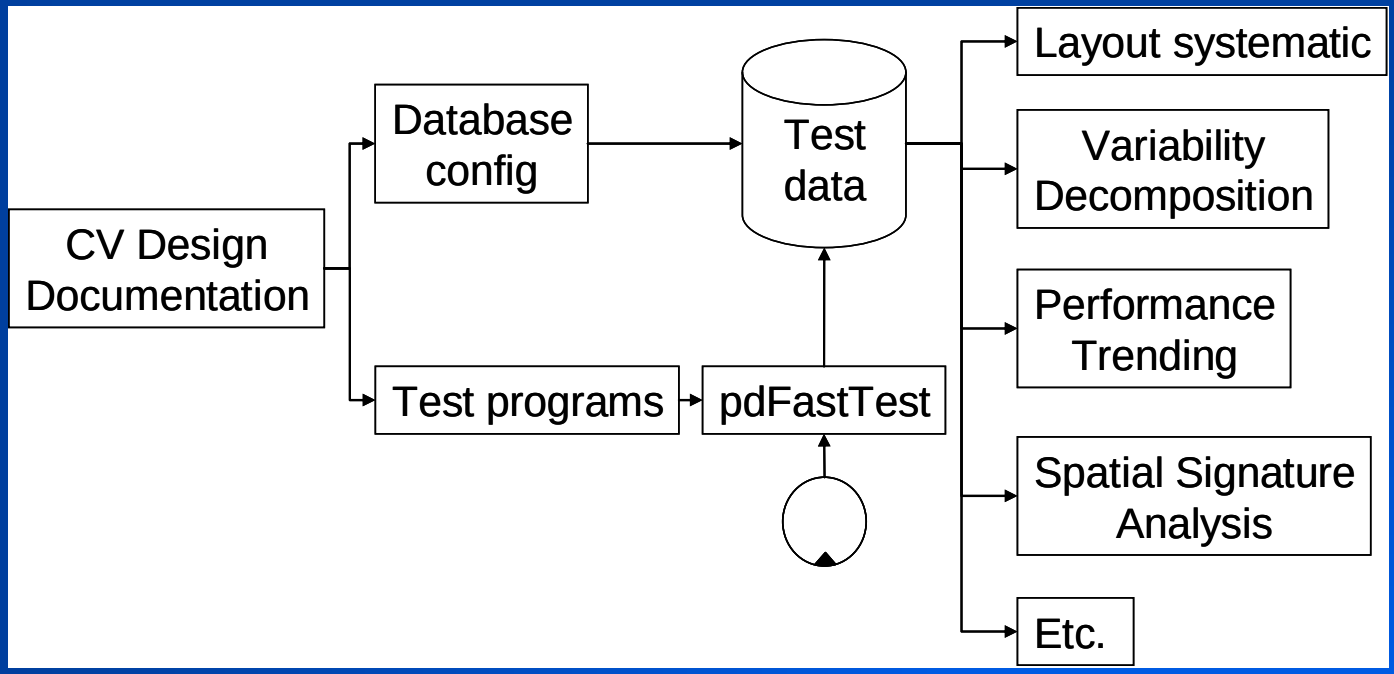
Challenges of Cost-effective Parallel Test

- **Low-resolution units to contain costs of parallel testers**
- **Short integration times**
- **What about leakage and leakage variation?**
- **<u>Three solutions</u>**
  1. Small number of high resolution units
  2. Large array structures to characterize mean leakage at die level
  3. Extraction from device characteristics above noise floor





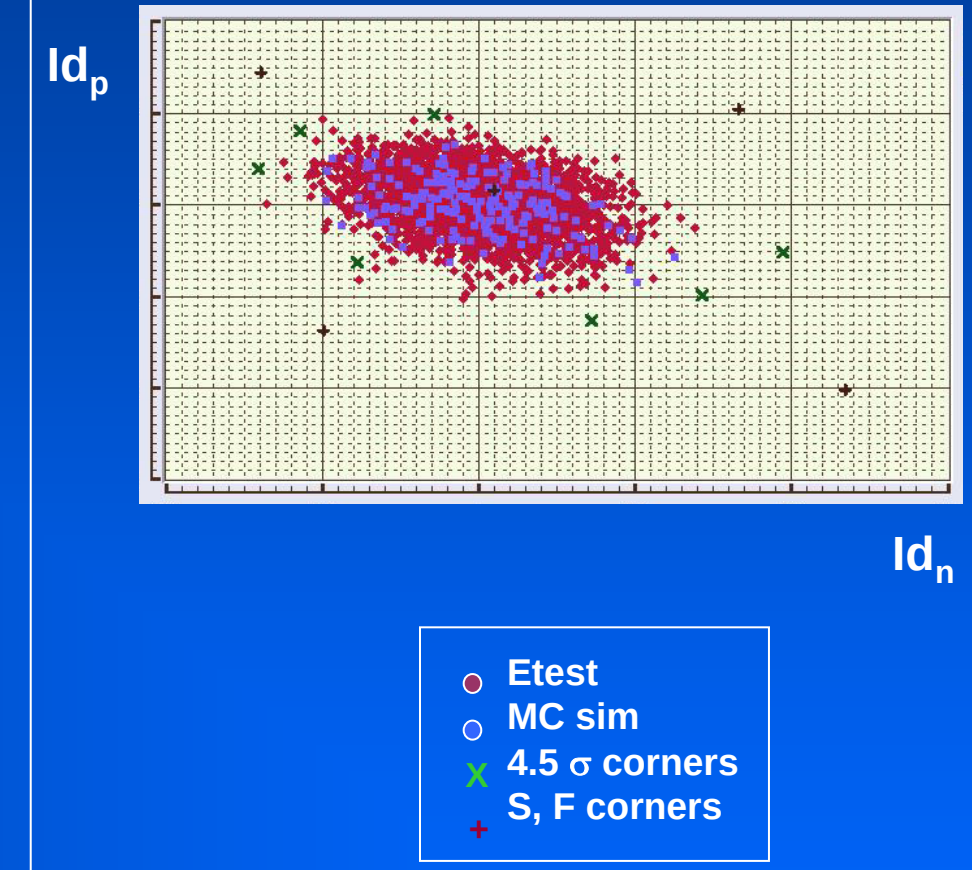
Efficient Automated Analysis



- **Robust Software infrastructure capable of:**
  - Efficient handling of large data volumes
  - Flexible data sub-setting and extraction
  - Advanced analyses
- **E.g. ours is built on top of dataPower YMS software**

Modeling & Design Enablement

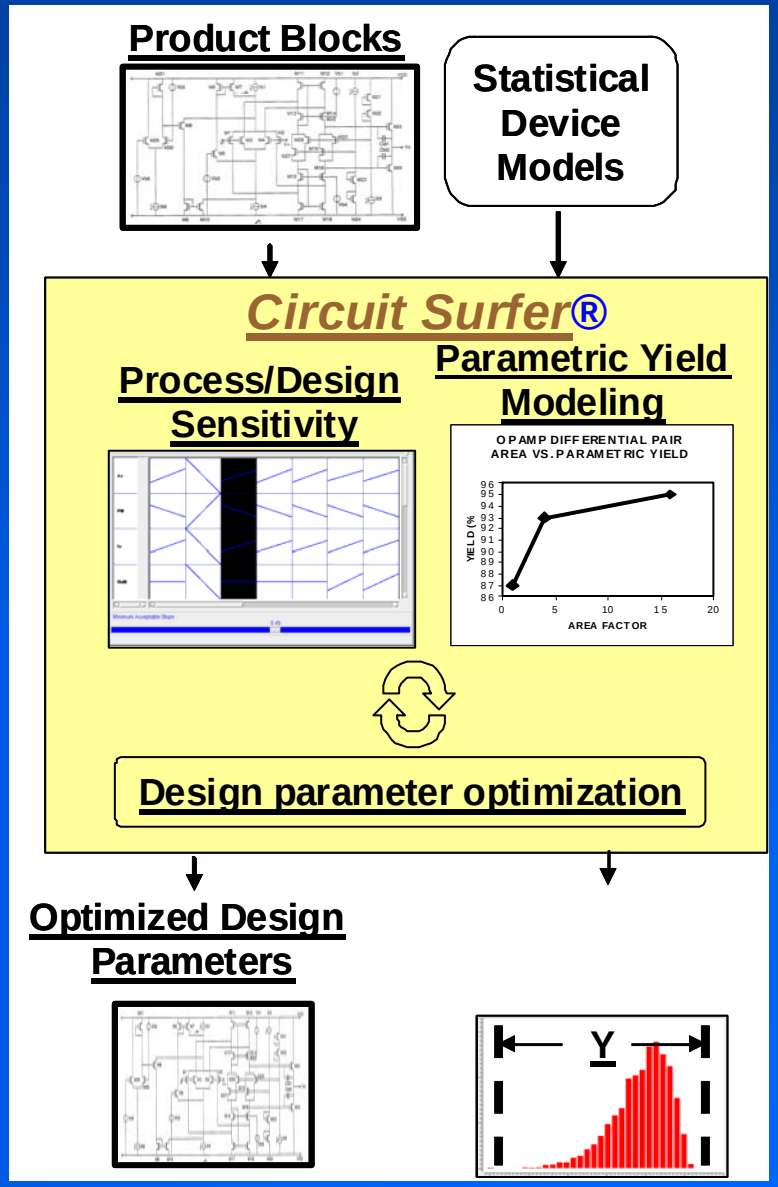
- **Statistical SPICE models**
- **Design tools for transistor level design**
  - Monte-Carlo Simulation
  - Design of experiments
  - Response surface methodology
  - Application-specific worst-case corners
- **SPICE models with switches for layout effects**
- **Statistical static timing analysis (SSTA)**
- **Tools and capabilities continue to be limited**



Block Level Statistical Design Tools and Flows

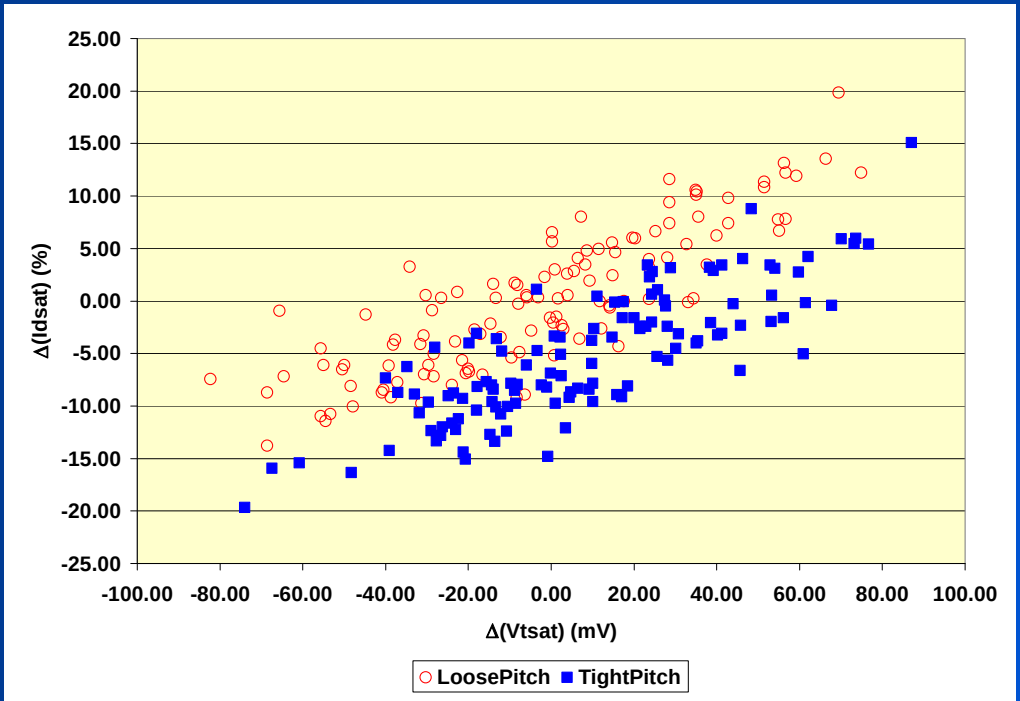
- **Suitable for: Analog, RF, Standard Cell design, SRAM**

- **Requirements/Features**
  - Monte-Carlo
  - DOE/RSM methodology
  - Efficient mismatch simulation
  - Sensitivity analysis: process and design variables
  - Application specific worst-case corner extraction

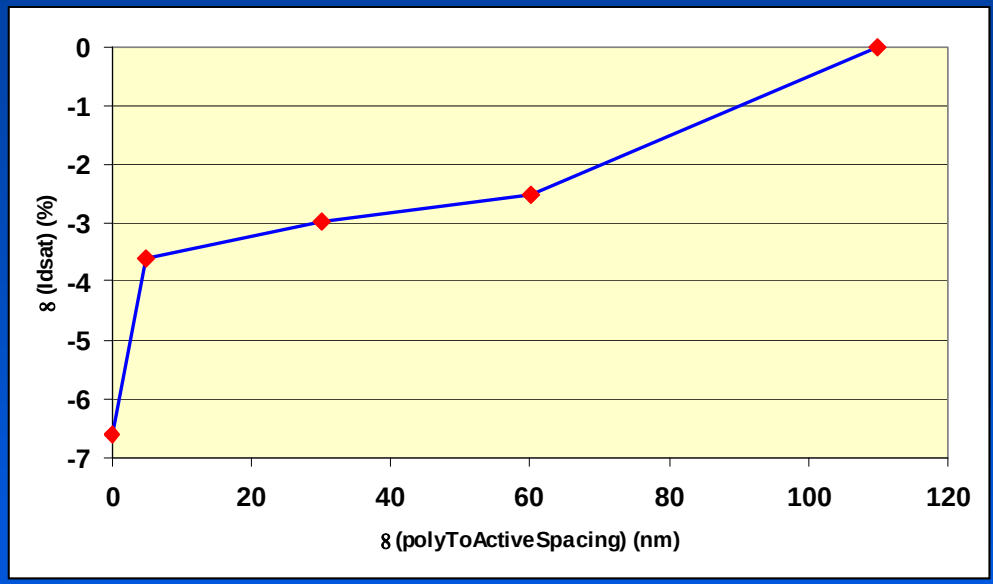


Applications: Systematic variation

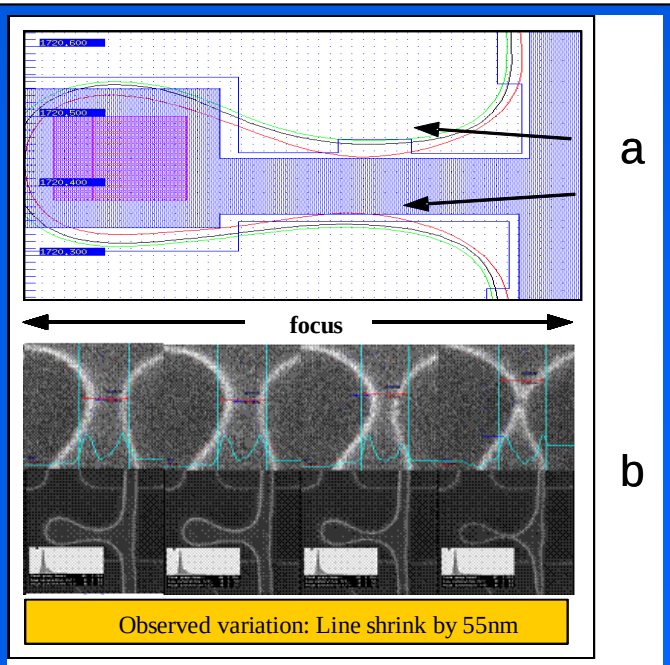
Gate pitch



Gate corner rounding



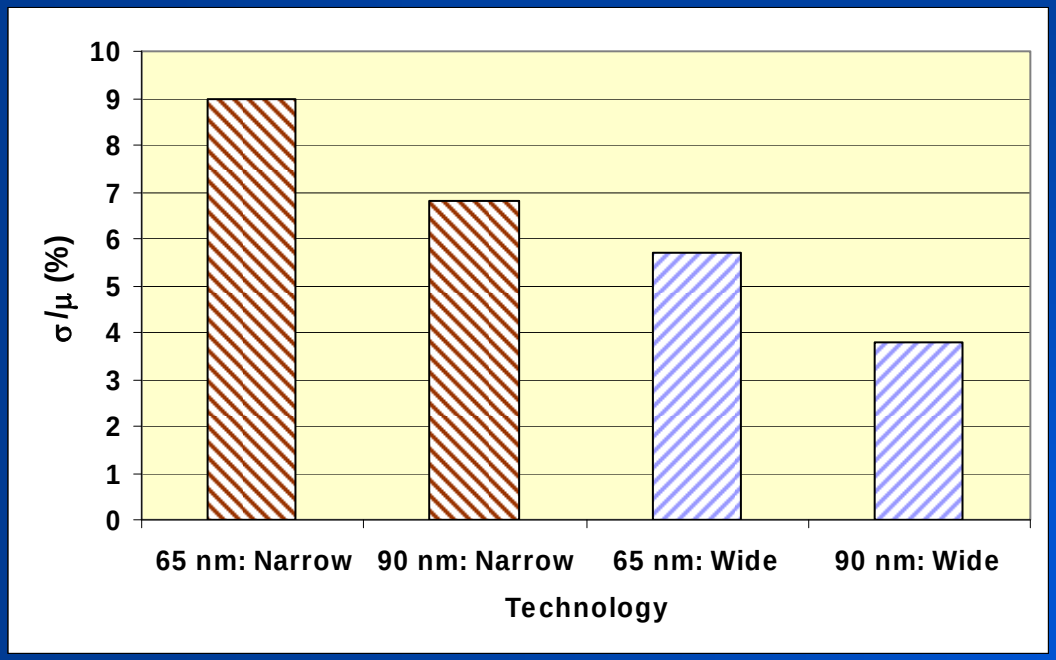
- **Infrastructure enables:**
  - Characterization of layout effects
  - Characterization of process window

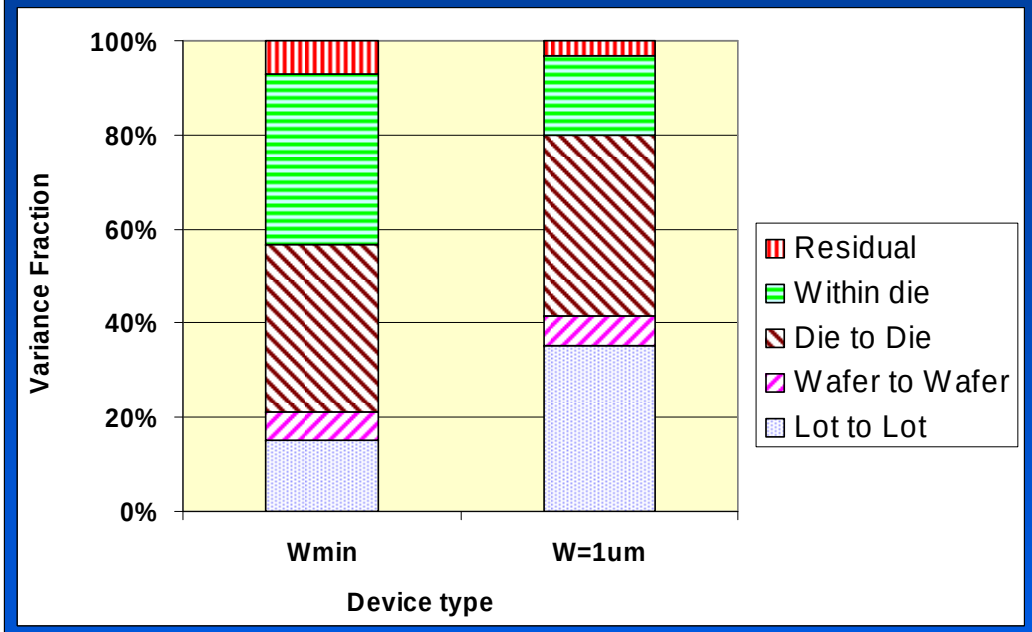


Systematic variation: Sample phenomena

Layout effect	Typical impact at 65 nm
Poly pitch: printability	3-5% change between pitches
Poly pitch: stress	5-10% change in Idrive
Poly orientation	2%-7% change in Idrive
Poly local neighborhood; e.g. center vs. edge gate	1-10% difference between center and edge gates (depends on OPC)
Poly corner rounding	2-7% decrease in Idrive for worst case
STI Stress	PMOS Idrive: 5-8% NMOS Idrive: 12-18%
Active corner rounding	1-5% Idrive increase for worst case
Gate counter-doping	6-10% decrease in PMOS Idrive
Contact density	3-5% Idrive decrease between dense and spare contacts

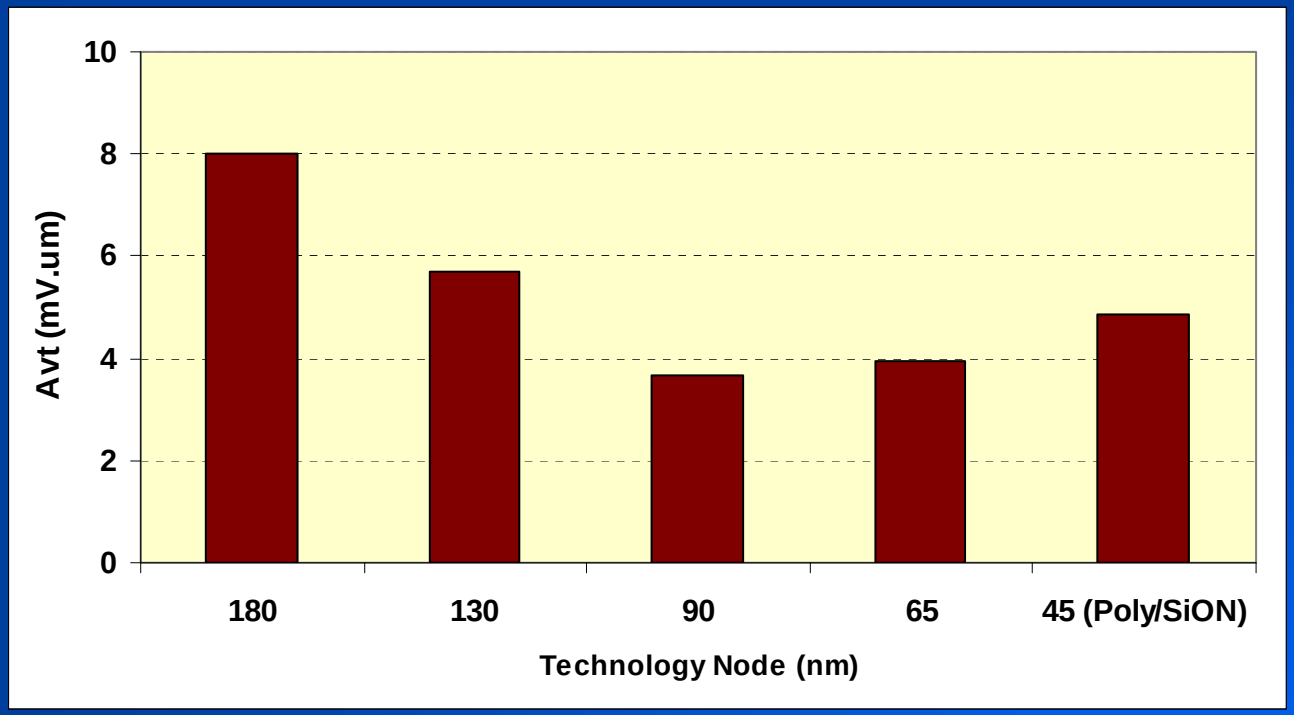
Applications: Total Variation





- Variability characterization for modeling and design enablement
- Variance decomposition to identify root causes and improvement

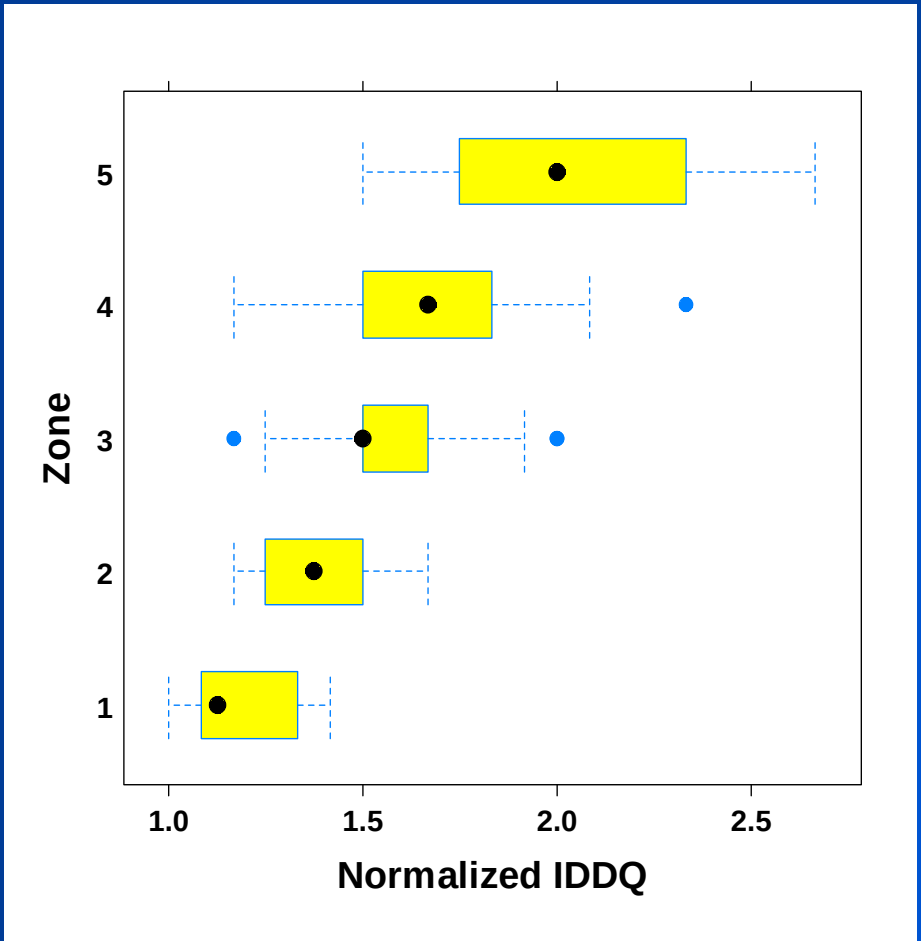
Applications: Local Variation

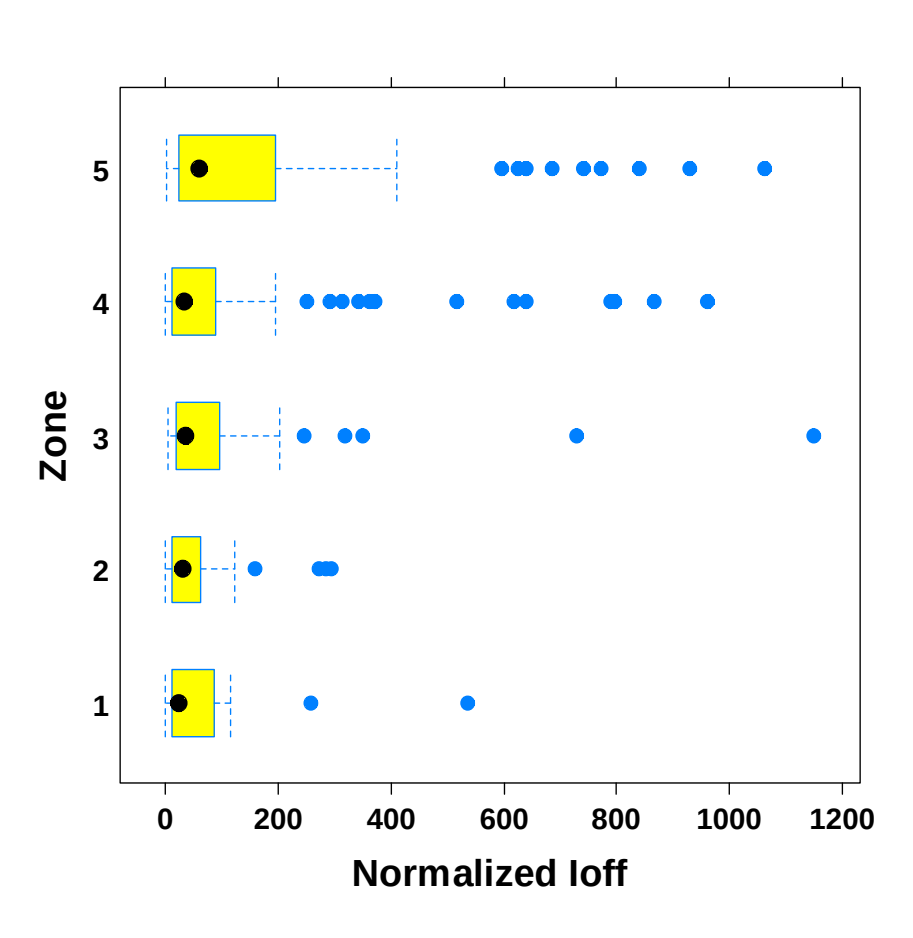


$$\sigma(\Delta(Vth)) = \frac{A_{VT}}{\sqrt{WL}}$$

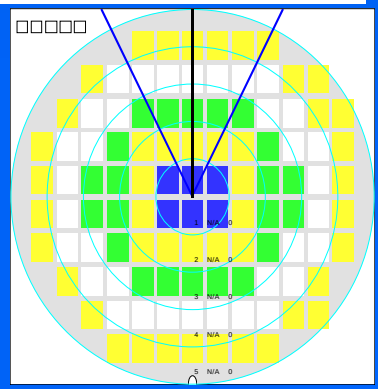
- Lack of T_{ox} scaling with SiON places severe restrictions on local variation (mismatch) improvement
  - SRAM Vmin
- Efficient infrastructure facilitates technology optimization for local variation minimization

Application: Yield Improvement





- Spatial correlation between product and transistor measurements allows isolation of root-causes of IDDQ LY



Summary

- Variability increase is a major challenge to the cost-effective utilization of nanometer scale technologies
- Meeting this challenge requires a comprehensive and accurate characterization of variability
- This presentation described an efficient infrastructure for characterizing the various components of transistor variation
- This infrastructure has been applied during technology development, optimization, modeling and design enablement and yield ramp from 90nm-32nm technology nodes

Further Information

1. S. Saxena, C. Hess et al., “Variation in transistor performance and leakage in nanometer-scale technologies”, IEEE Trans. ED, vol 55. no 1, pp. 131-144, 2008.

2. S. Saxena, T. Uezono et. al., “Estimating MOSFET leakage from low-cost, low-resolution fast parametric test”, Proc. IEEE ICMTS, pp. 119-123, 2009.

3. C. Hess, S. Saxena, et. al, “Device array scribe characterization vehicle test-chip for ultra-fast product variability monitoring”, Proc. IEEE ICMTS, pp 145-149, 2007.