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DESIGN AUTOMATION

Design for Variability in Analog / Mixed-Signal Circuits

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Outline

- Design Loss / Opportunity Cost
- Problem with Global Process Corners
- True Corners
- Epistemic Uncertainty
- Proximity Effects
- Conclusions

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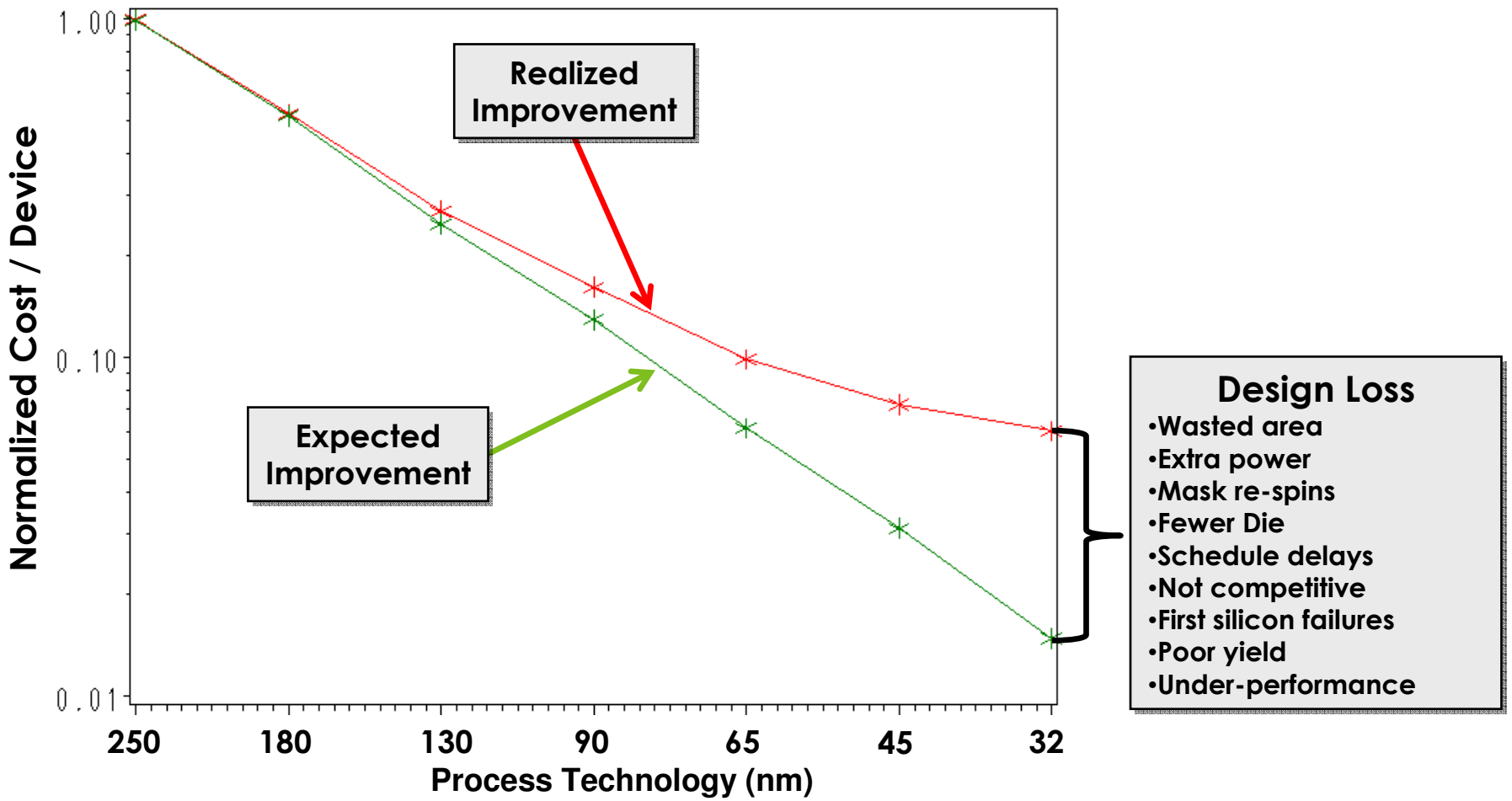
Process Variation causes Design Loss



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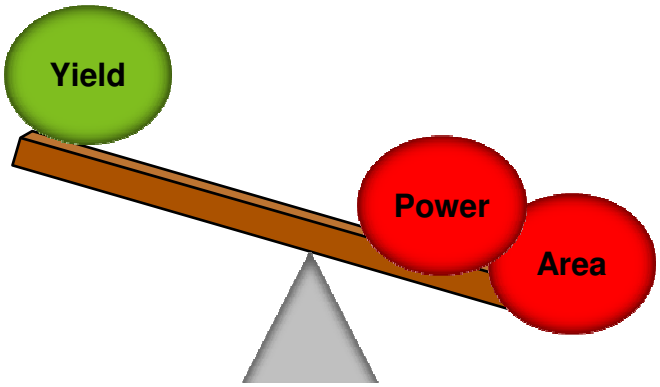
What causes Design Loss?

Over Design

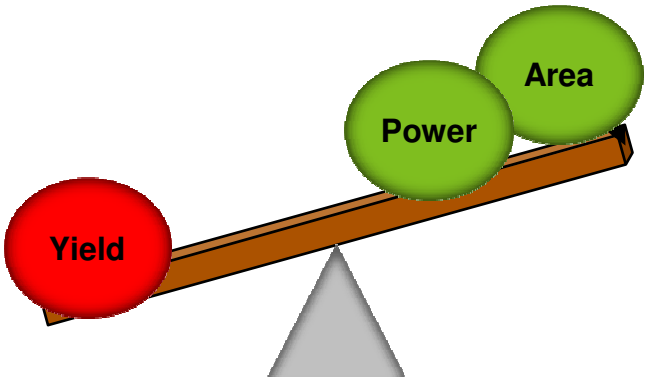
Ex: Excessive Guard-band to Spec



- Meets performance specs
- Consumes too much power
- Wastes area – higher die cost
- Product not competitive

Under Design

Ex: Insufficient Margin to Spec



- Fails performance specs
- Yield loss – higher die cost
- Causes mask re-spins
- Slow ramp to production

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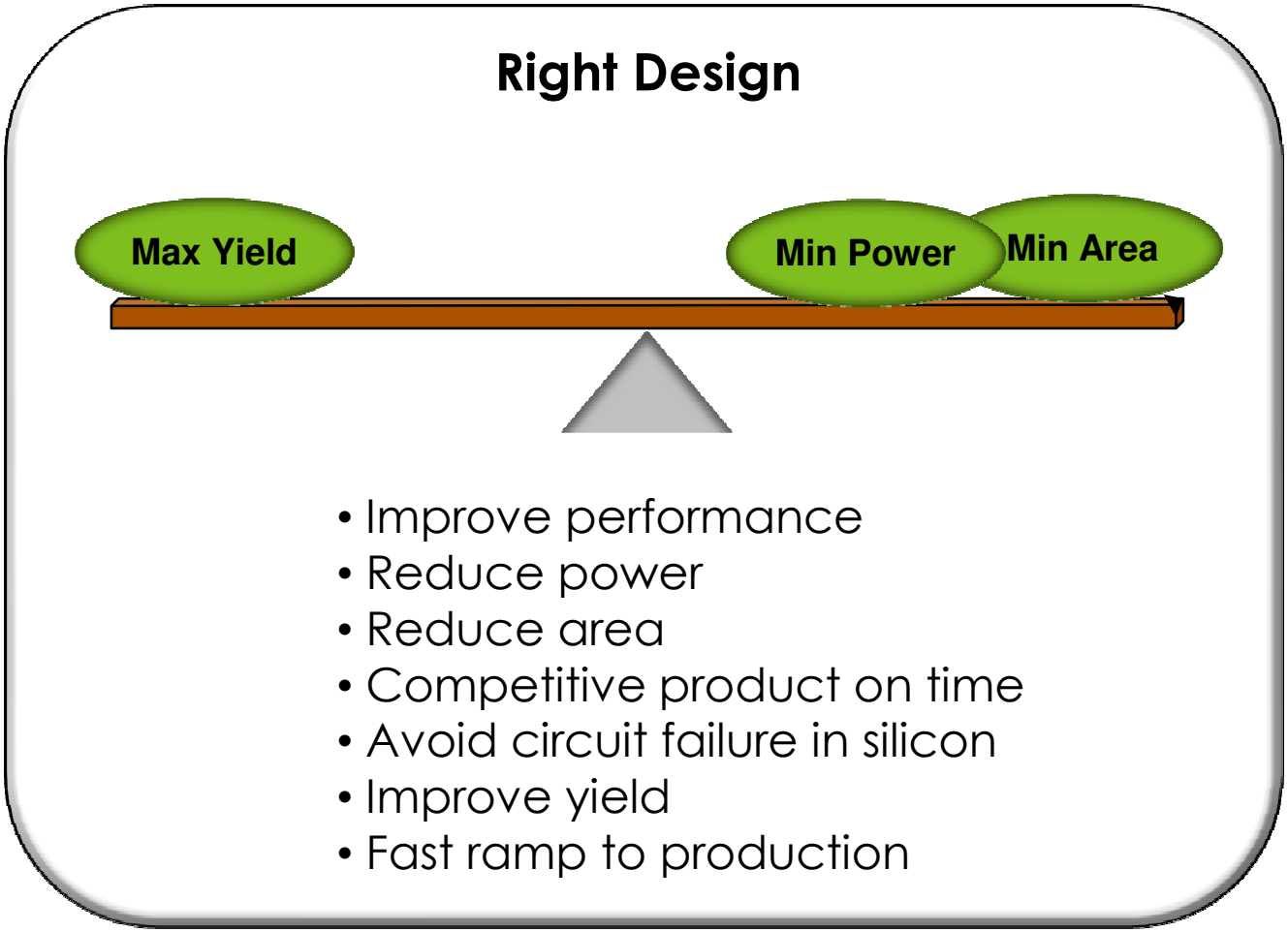
Solido: Eliminate Design Loss
Right Design, Fast



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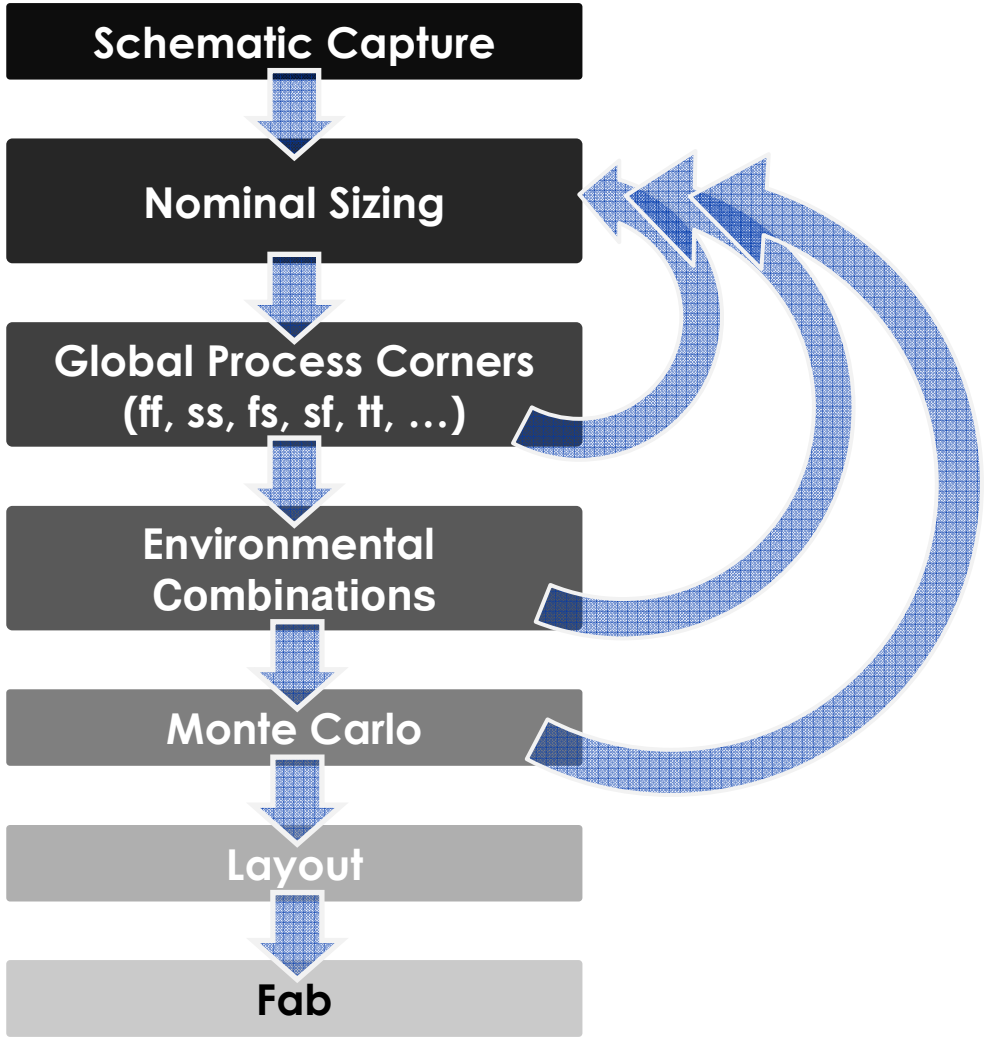
Traditional Statistical Variation Design
Design to Global Process Corners, Verify with Monte Carlo



Many iterations
due to inadequate
statistical coverage
during design sizing

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Problems with Global Process Corners

- Do not include local variation
  - Local variation is geometry dependent
  - Devices *must* "wiggle" independently
- Do not include environmental conditions
  - Supply voltage
  - Temperature
- Are derived for digital application
  - Geometries
    - Digital uses min-L, ~min-W
    - A/MS and RF design spans the entire geometry space
  - Bias
    - digital cares about Ion / Ioff
    - A/MS and RF care about C's and g's
    - Voltage driven definition but current driven application

Model files include Process Variation Effects

Process variation data is already available in models
BUT data is typically not utilized fully

Foundry

tsmc

UMC

common platform

→

Digital corners (TT,FF,SS,FS,SF)

≤ 180 nm
Statistical variation parameters:
Global variation (*e.g. dvth_g, du0_g*)
Local variation (*e.g. dvth_l, du0_l*)

≤ 90 nm
Well Proximity Effect Parameters
(*e.g. sca, scb, scc*)

≤ 65 nm
Foundry-Defined Stress Parameters

→

designer

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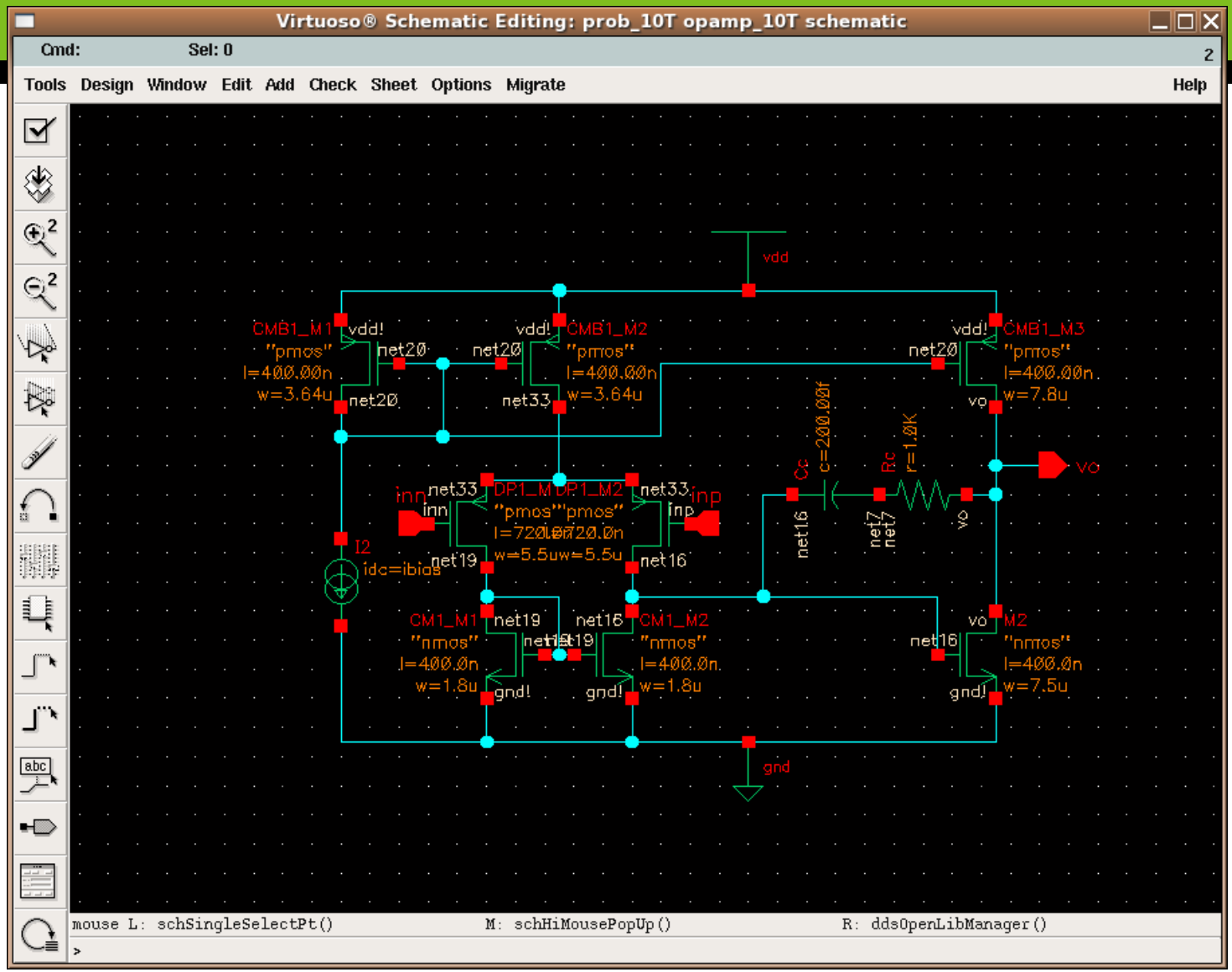
8 Transistor Amplifier Example



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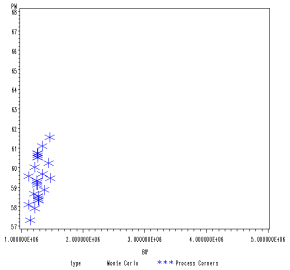
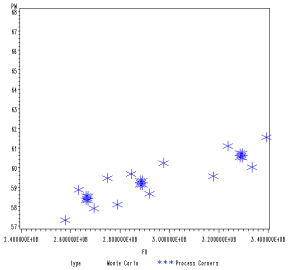
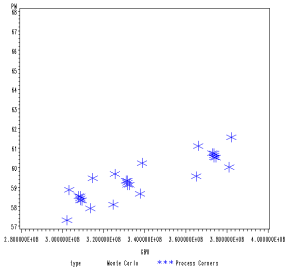
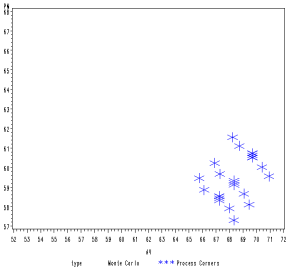
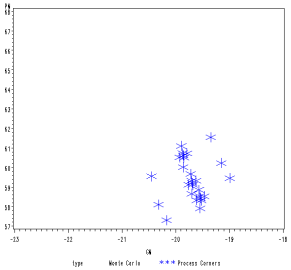
Global Process Corners



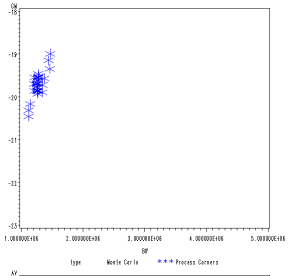


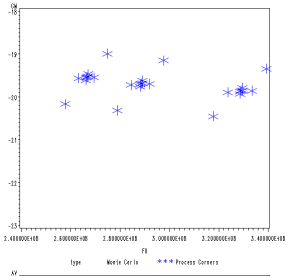


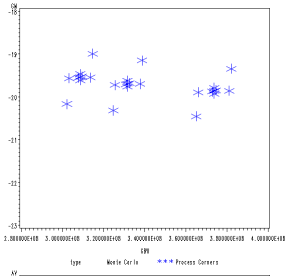


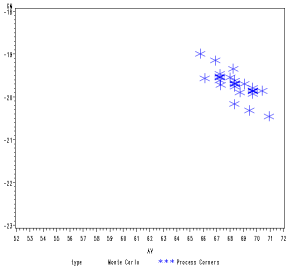


Phase Margin

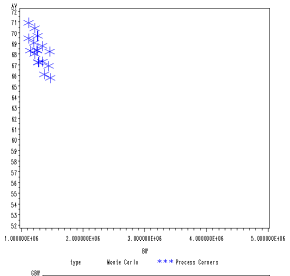


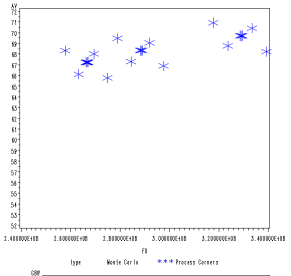


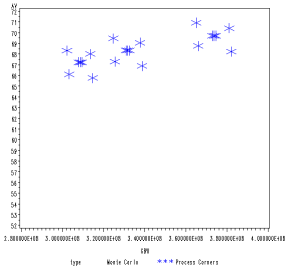




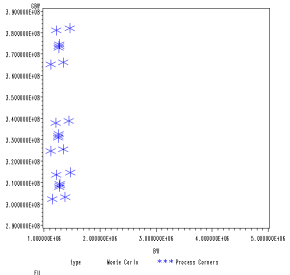
Gain Margin

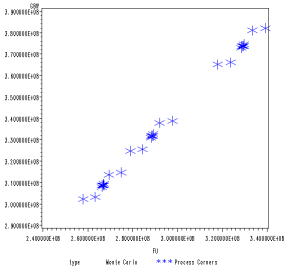




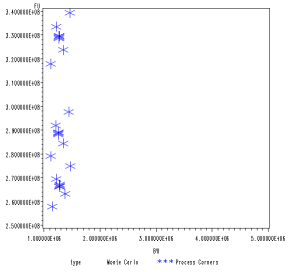


Gain





Gain Bandwidth



Unity Gain Frequency

Bandwidth

Statistical results

✳ = process corners
(best, worst case, etc.)

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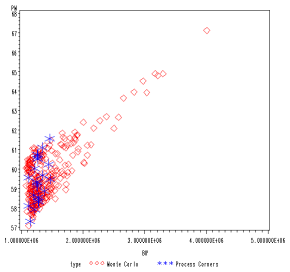
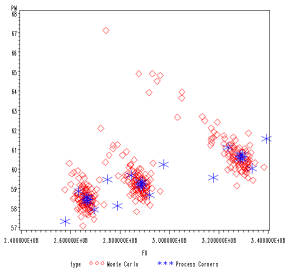
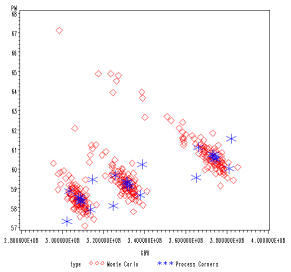
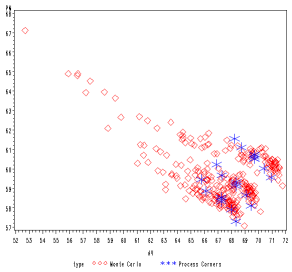
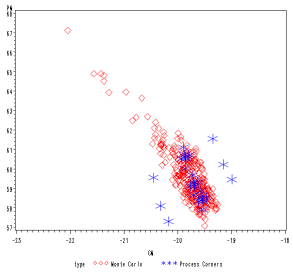
Full Statistical Simulation



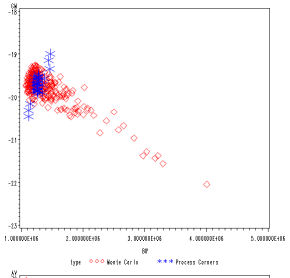


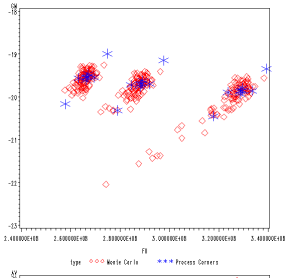


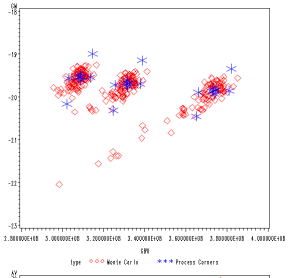


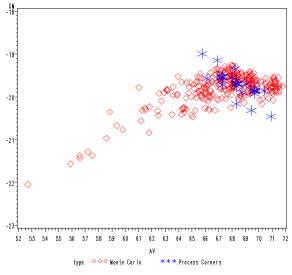


Phase Margin

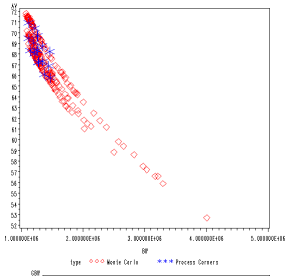


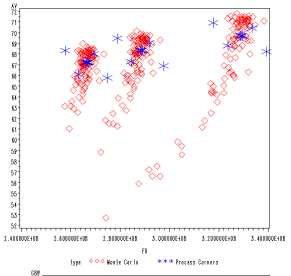


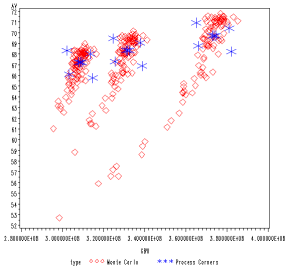




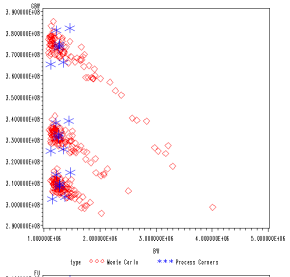
Gain Margin

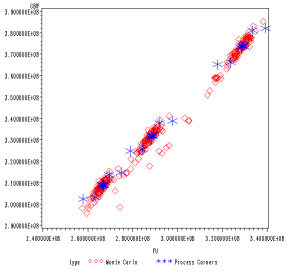




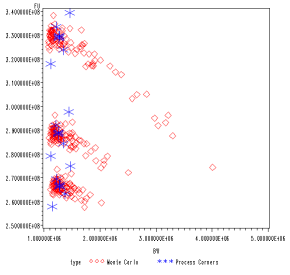


Gain





Gain Bandwidth



Unity Gain Frequency

Bandwidth

Statistical results

✳ = process corners (best, worst case, etc.)

◊ = All sources of statistical variation

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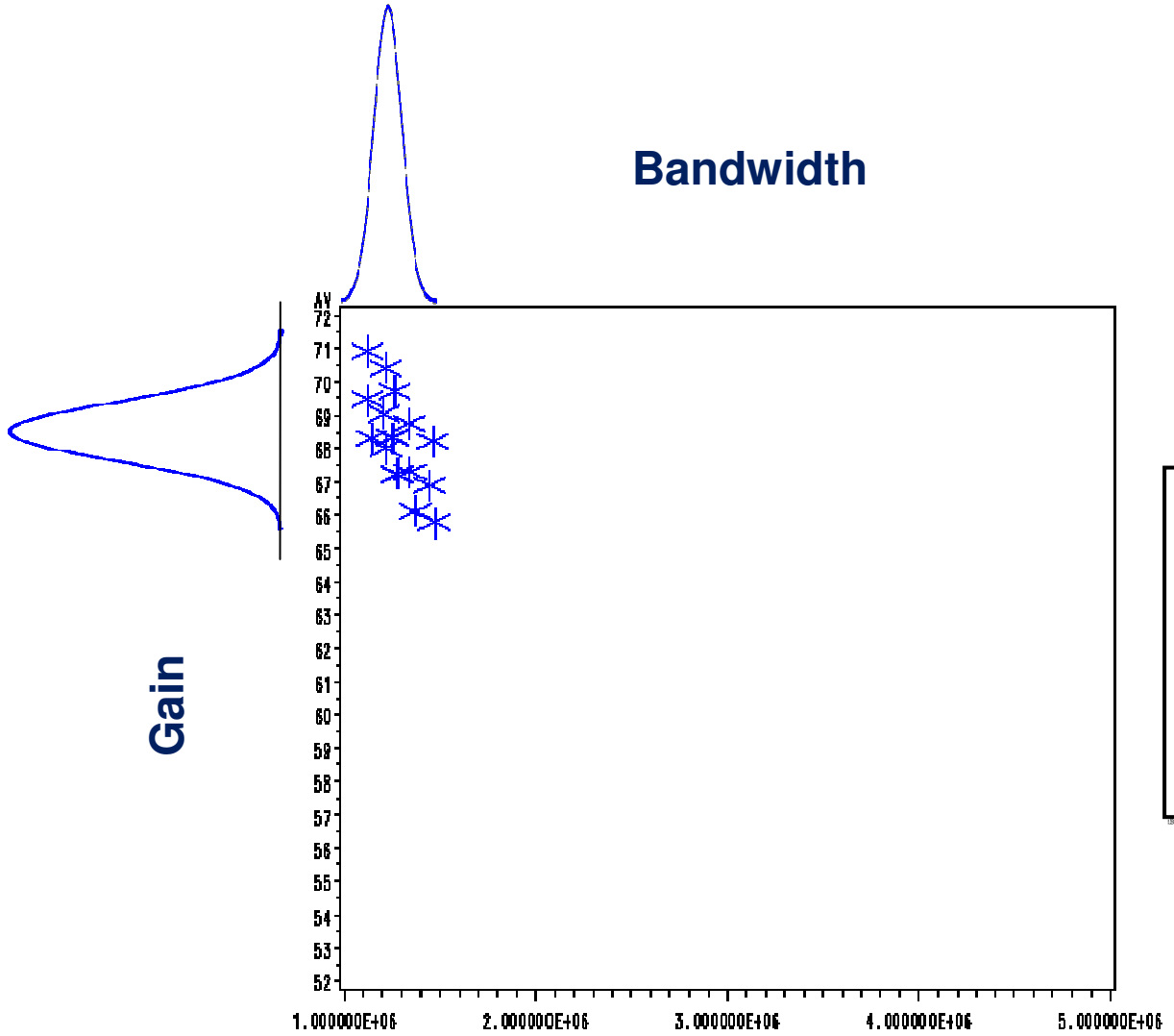
Global Process Corners



Statistical results

✳ = process corners
(best, worst case, etc.)

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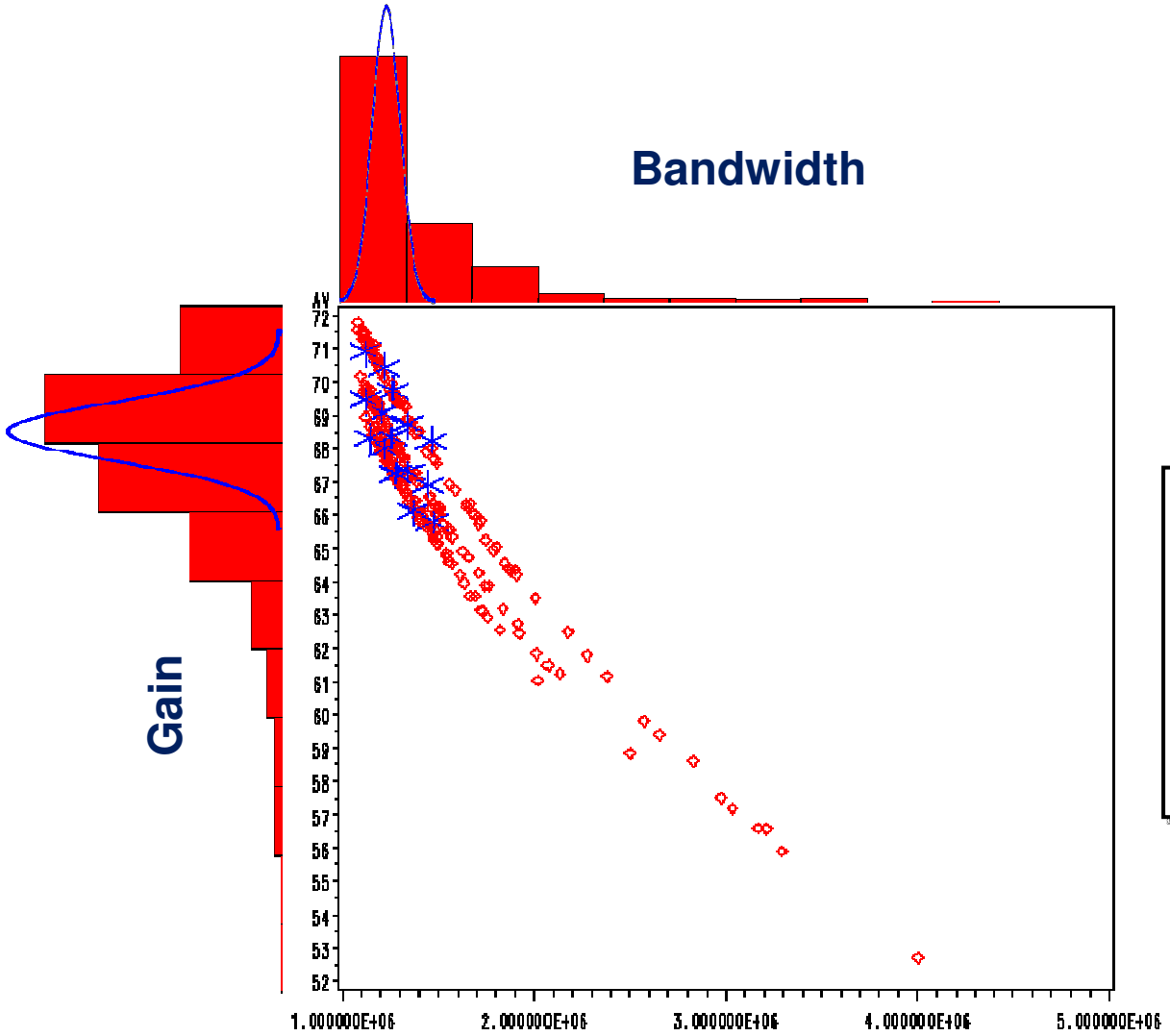
Full Statistical Simulation versus Global Process Corners



Statistical results

✳ = process corners (best, worst case, etc.)

◊ = All sources of statistical variation

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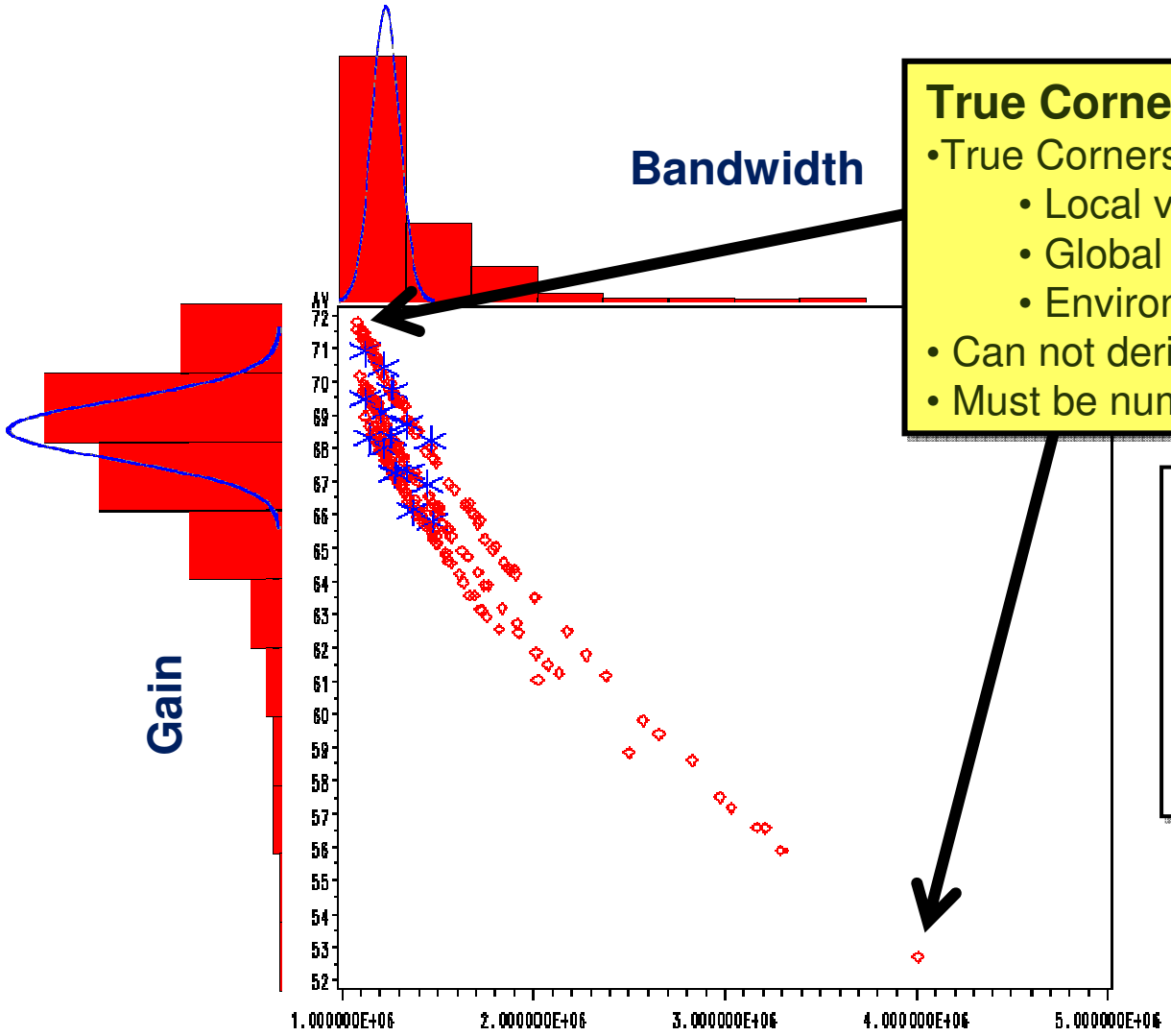
True Corners



True Corners

- True Corners include:
  - Local variation
  - Global variation
  - Environmental parameters
- Can not derive analytic dependency
- Must be numerically evaluated

Statistical results

✳ = process corners (best, worst case, etc.)

◊ = All sources of statistical variation

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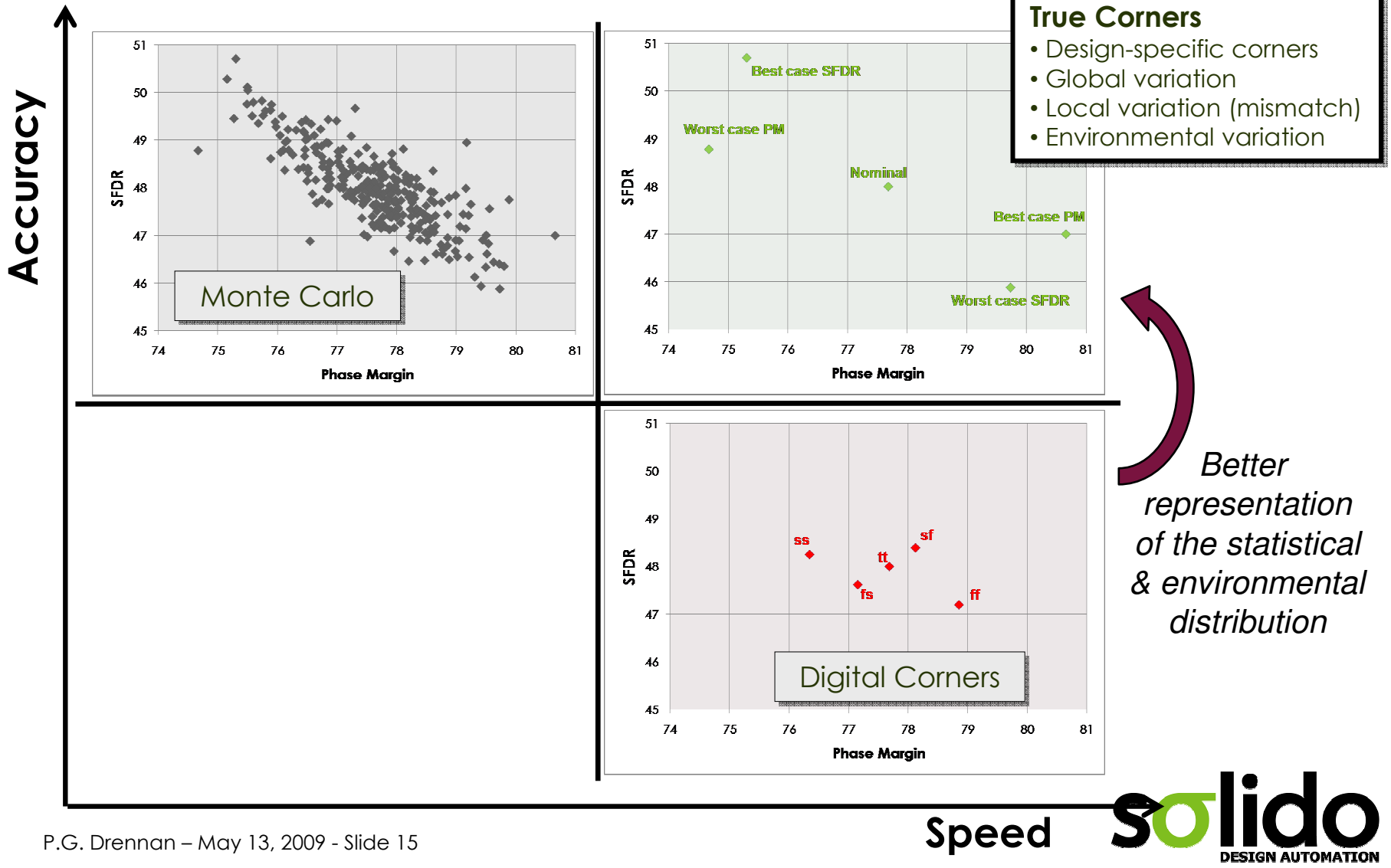
True Corners
Monte Carlo accuracy in Digital Corner time



True Corners
- Design-specific corners
- Global variation
- Local variation (mismatch)
- Environmental variation

Better representation of the statistical & environmental distribution

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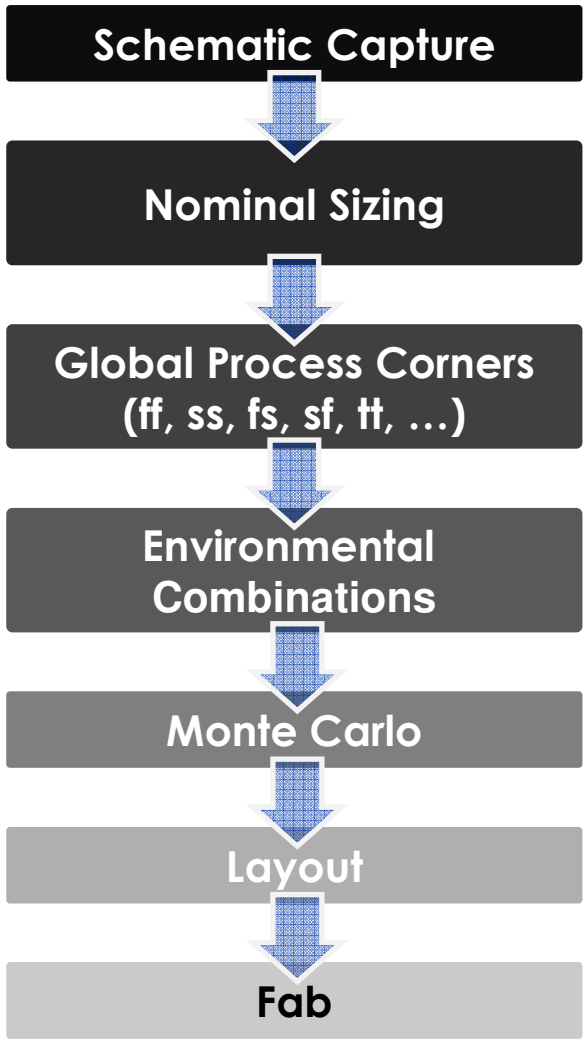
Statistical Variation Design Evolution

Digital Corner Flow

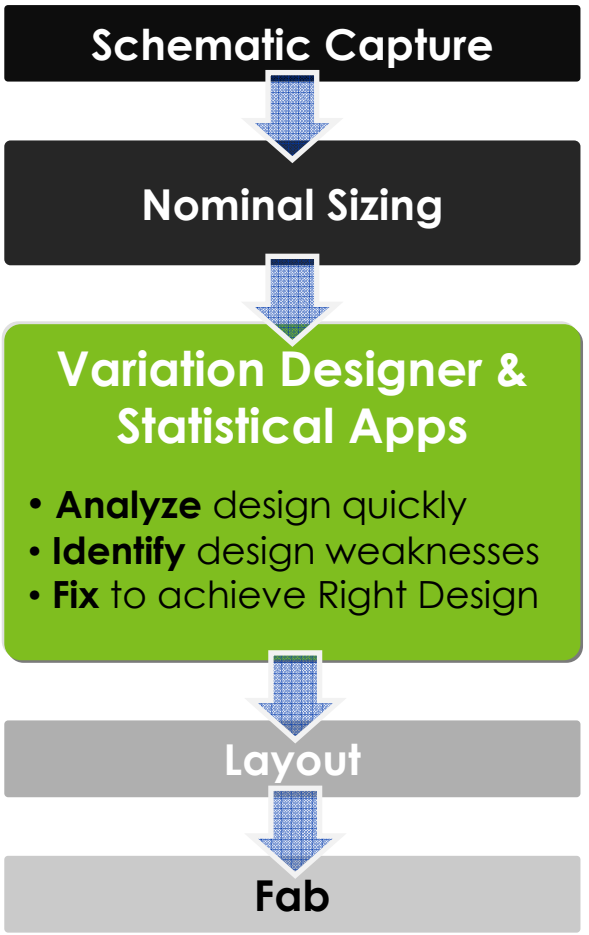


Fast

Familiar

Accurate

True Corner Flow



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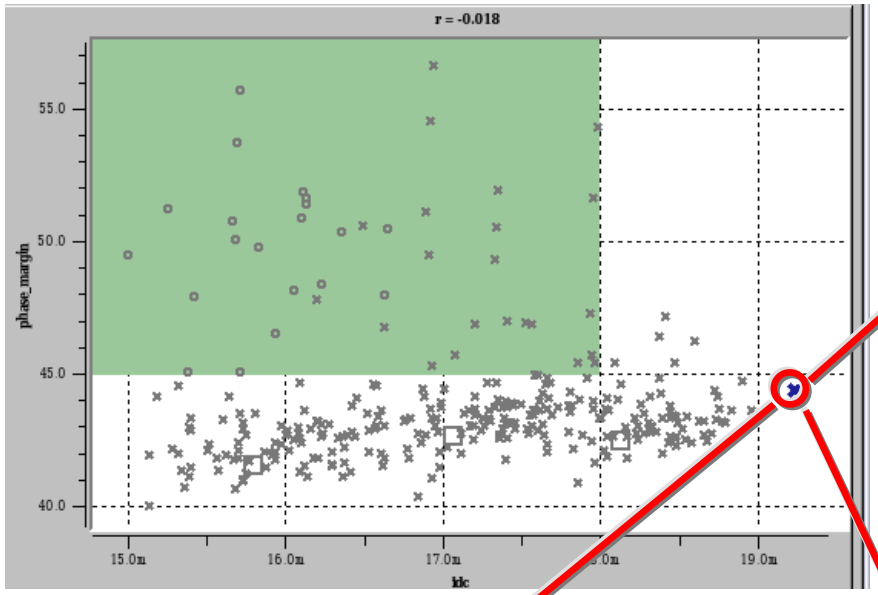
True Corner-driven design: Anatomy of a True Corner



Environmental corner settings

```
modify_ibias alter param=ibias value=1.05e-05
modify_vdda alter param=vdda value=1.58
modify_vcm alter param=vcm value=0.81
modify_Temperature alter param=temp
value=45.0
```

Local variations

```
modify_I2_I5_MN26_dvton alter sub=I2.I5.MN26
param=dvton value=1.11158768808
modify_I2_I5_MN26_xbon alter sub=I2.I5.MN26
param=xbon value=-0.328789341698
modify_I2_I5_MN25_dvton alter sub=I2.I5.MN25
param=dvton value=0.500116216138
modify_I2_I5_MN25_xbon alter sub=I2.I5.MN25
param=xbon value=-0.726111824424
modify_I2_I5_MN24_dvton alter sub=I2.I5.MN24
param=dvton value=2.66805858619
...
```

Global variations

```
global_parameters_alter altergroup{
parameters
+ devtoxn=-0.894507450271
+ slfacnan=-0.343906959091
+ slfacnap=0.163598578623
+ swfacnan=1.44464459729
+ cjunvarp=-0.0600889154501
+ devdelwn=1.47641587117
+ rshpo=-0.0218030379434
+ swfacnap=1.24062694315
+ rshno=0.619034146098
+ devtoxp=0.237537397475
...
```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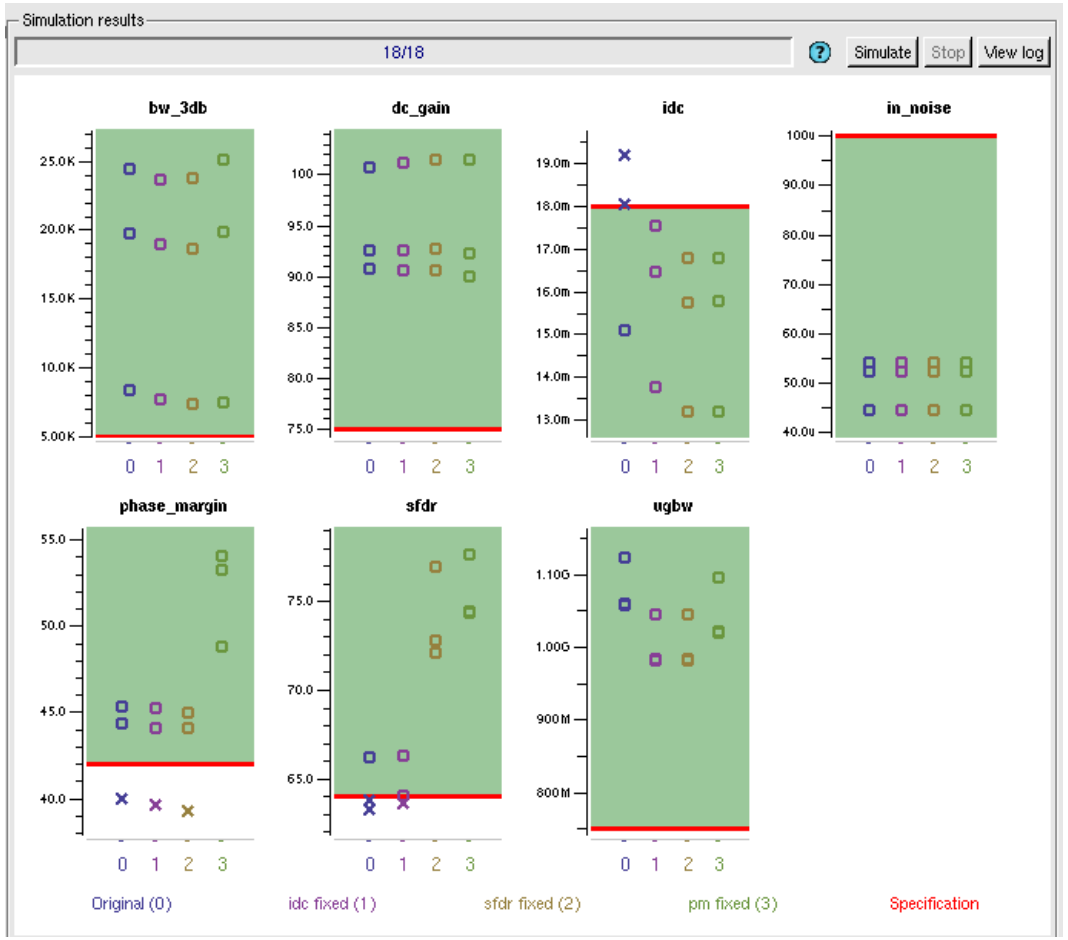
Designing With True Corners



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Epistemic Uncertainty, Explained

"... there are known knowns; there are things we know we know. We also know there are known unknowns; that is to say we know there are some things we do not know. But there are also unknown unknowns - the ones we don't know we don't know."

Epistemic Uncertainty ➔ know your unknowns

Proximity Effects: The MOSFET electrical performance (V_t, μ_o, etc.) is significantly affected by surrounding features in layout

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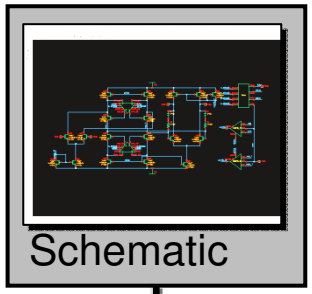
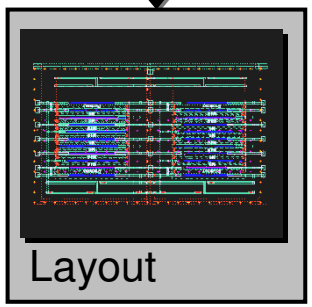
The Proximity Effect Problem



SPICE sim



You need to know proximity effects values at schematic

But you do not know the proximity values until layout

Epistemic Uncertainty

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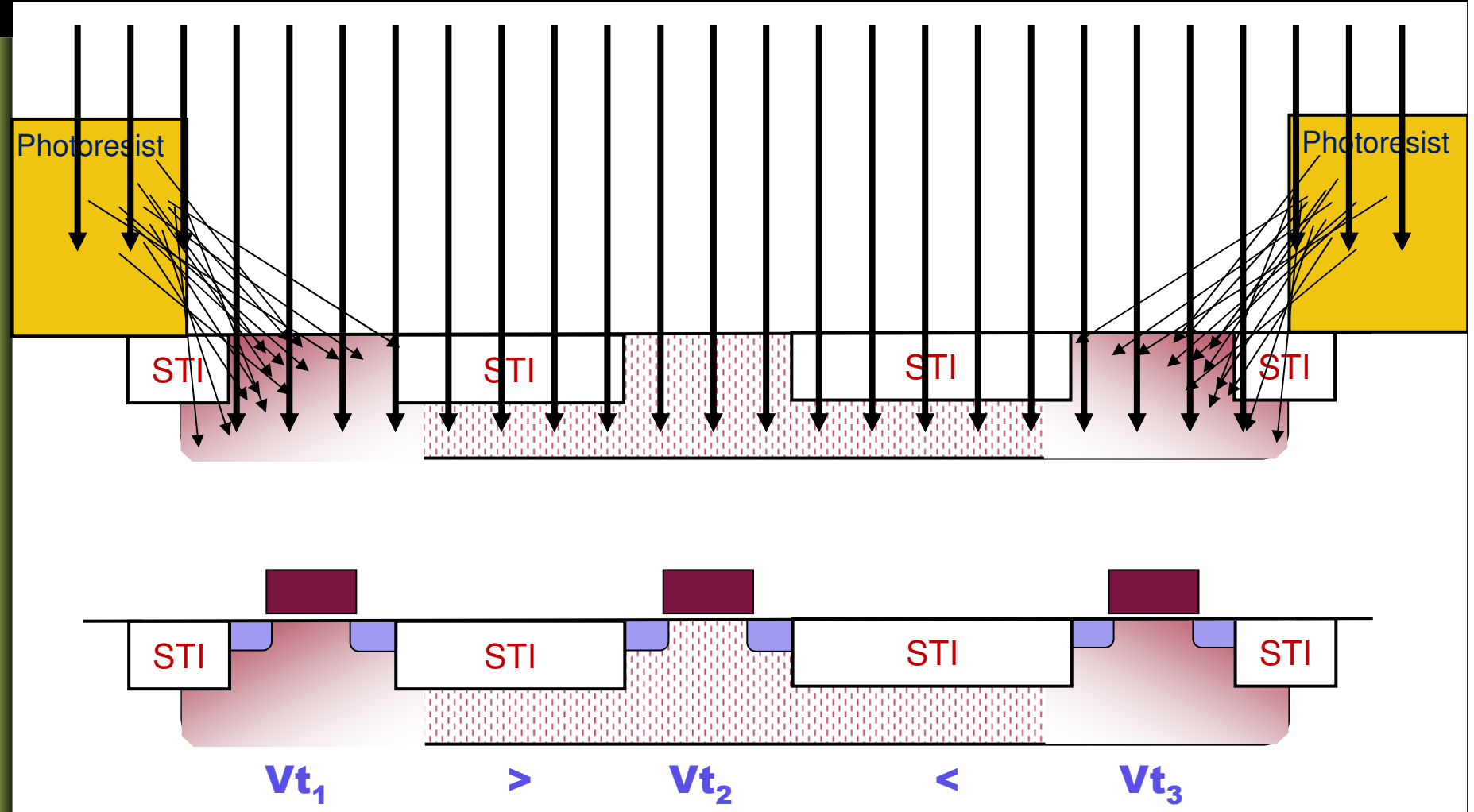
Well Proximity Effect (WPE)



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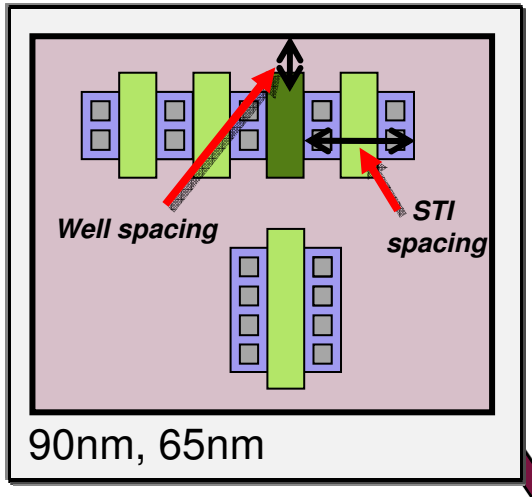
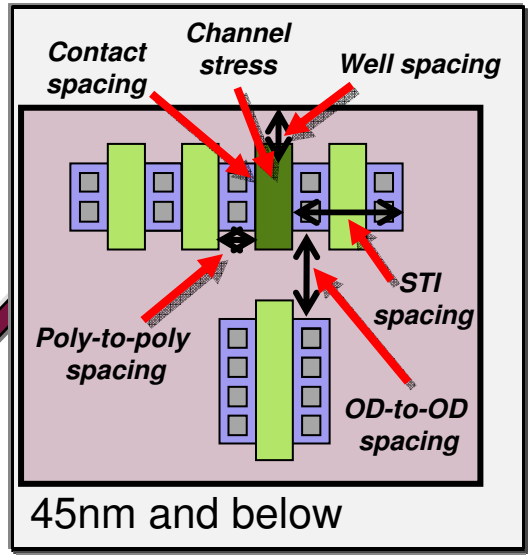
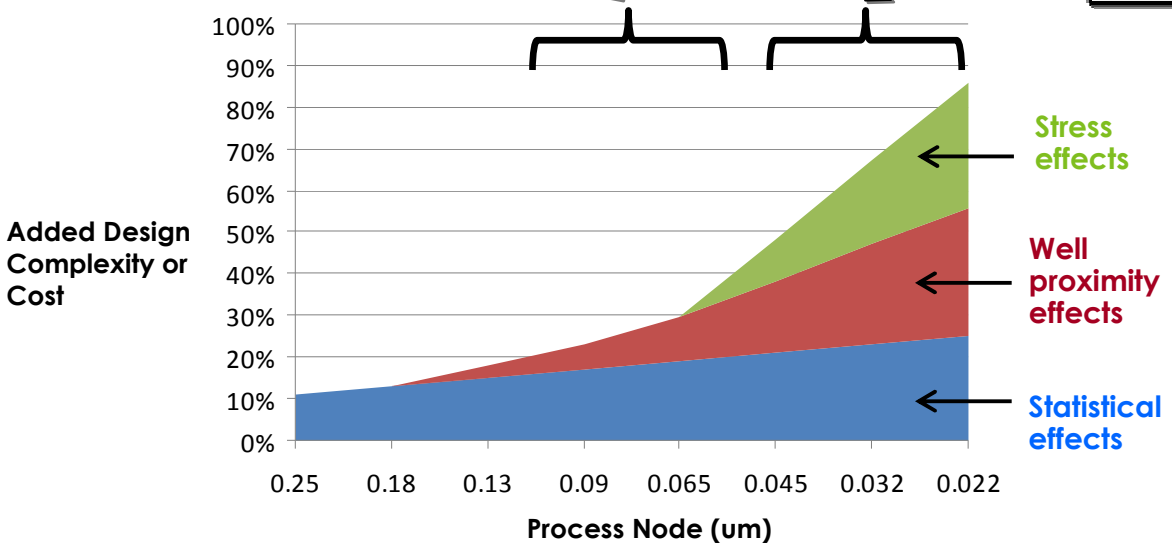
Proximity Effect Problem







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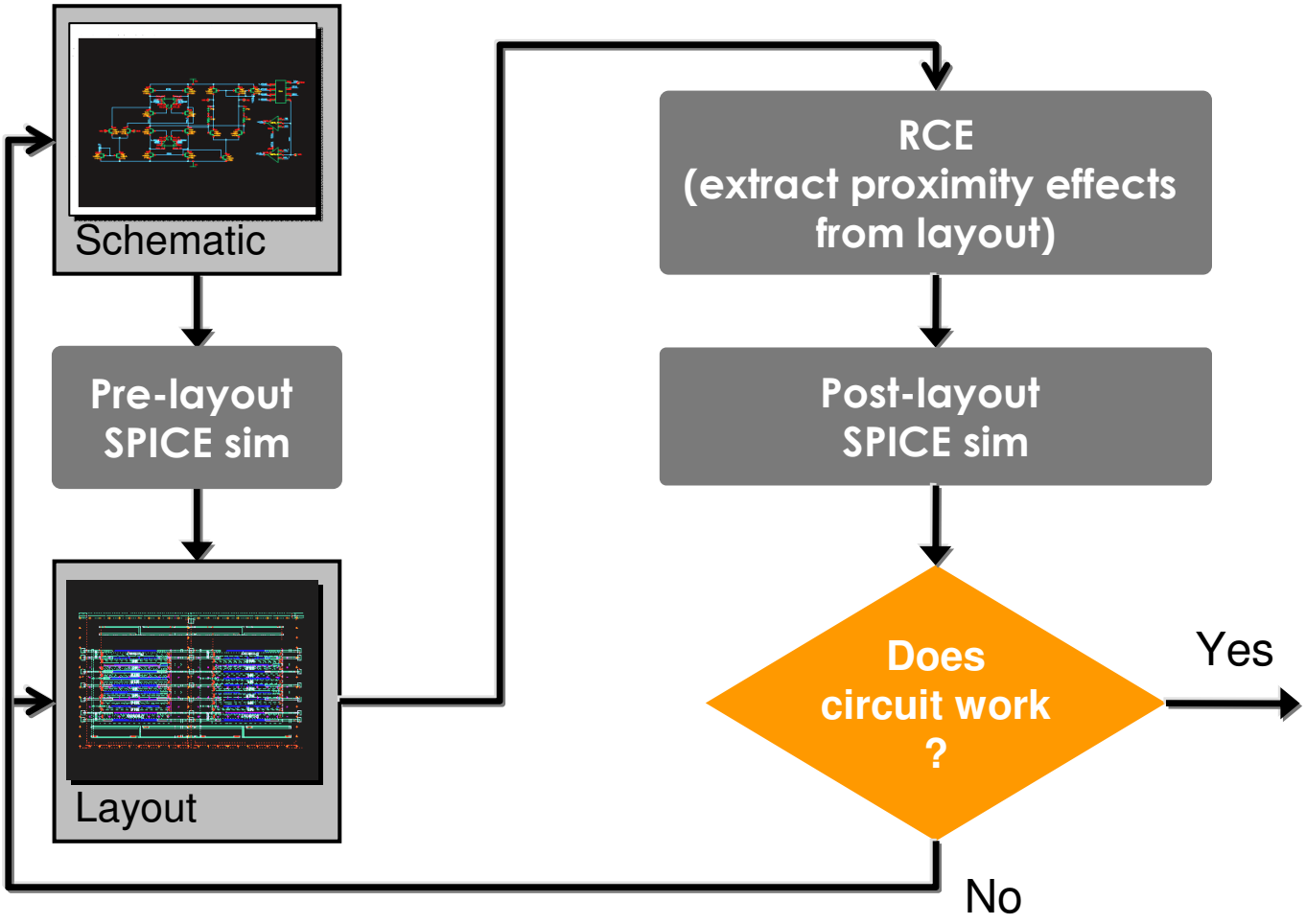
The Current Solution: Expensive Loop



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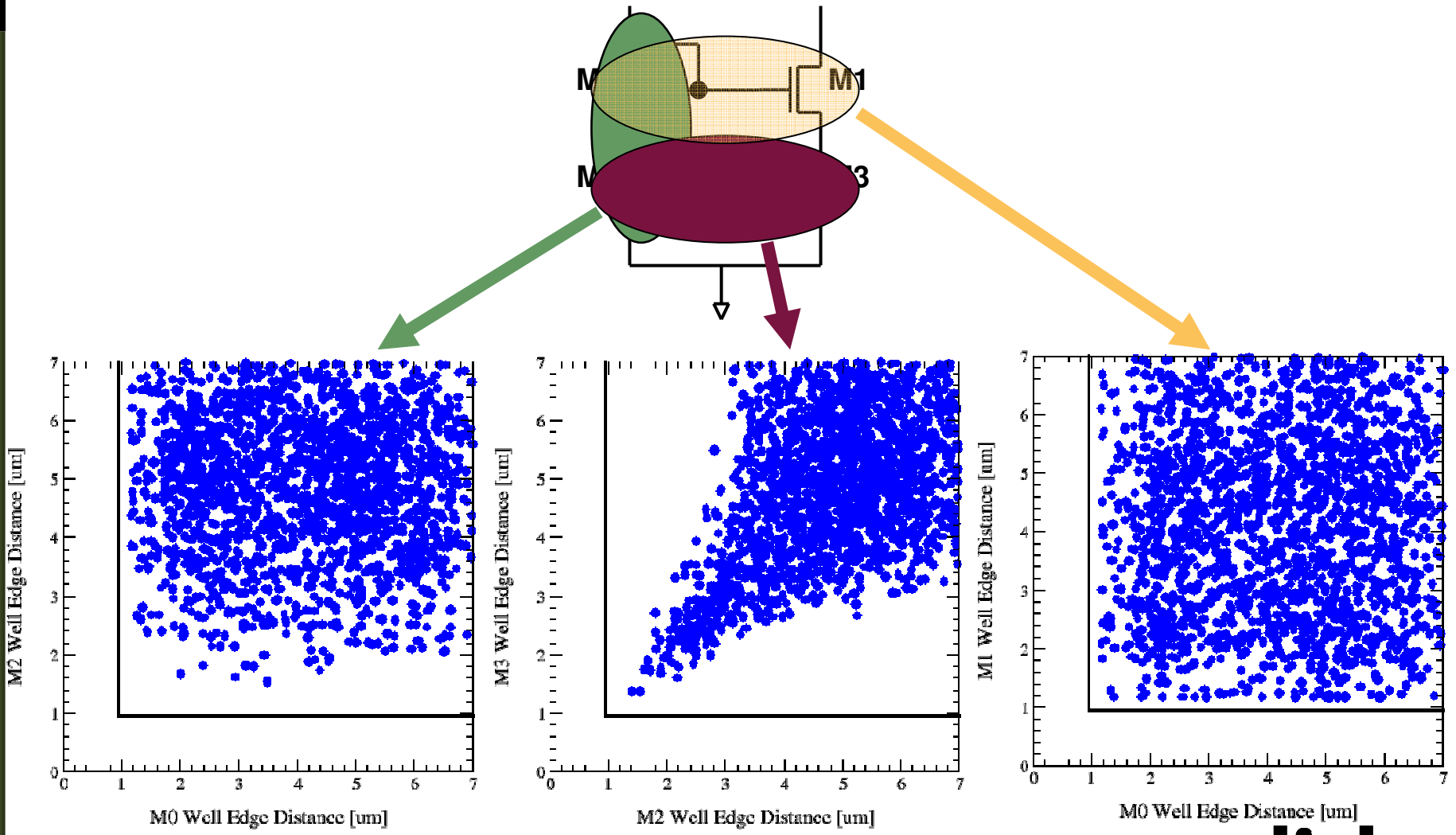
Feasibility for a Cascode Current Mirror



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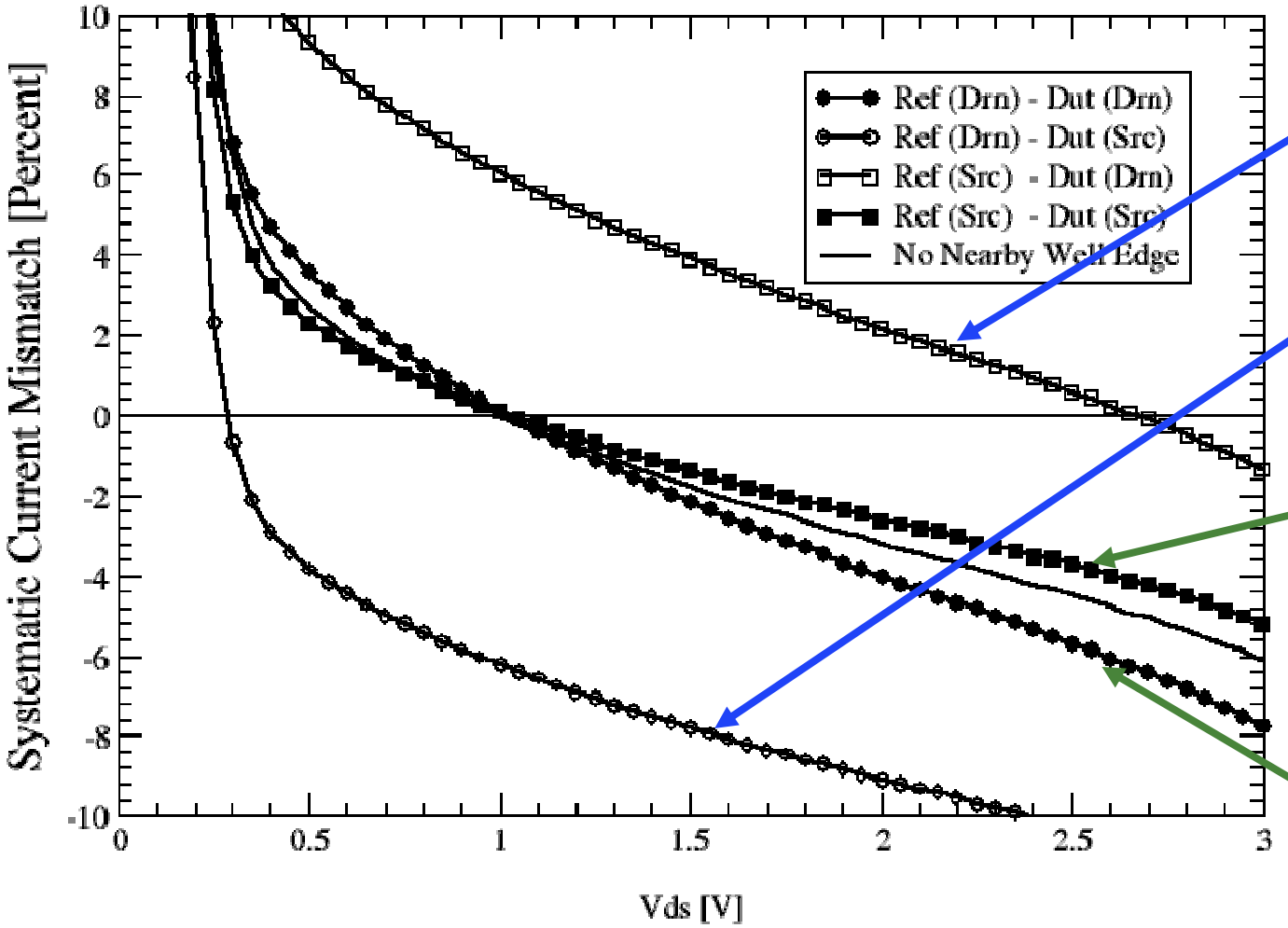
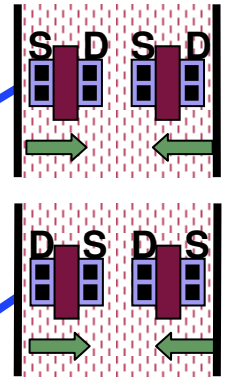
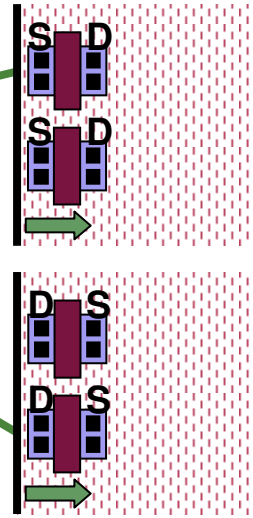
Current Mirror Outcomes Based on Layout



Example #2



Example #3



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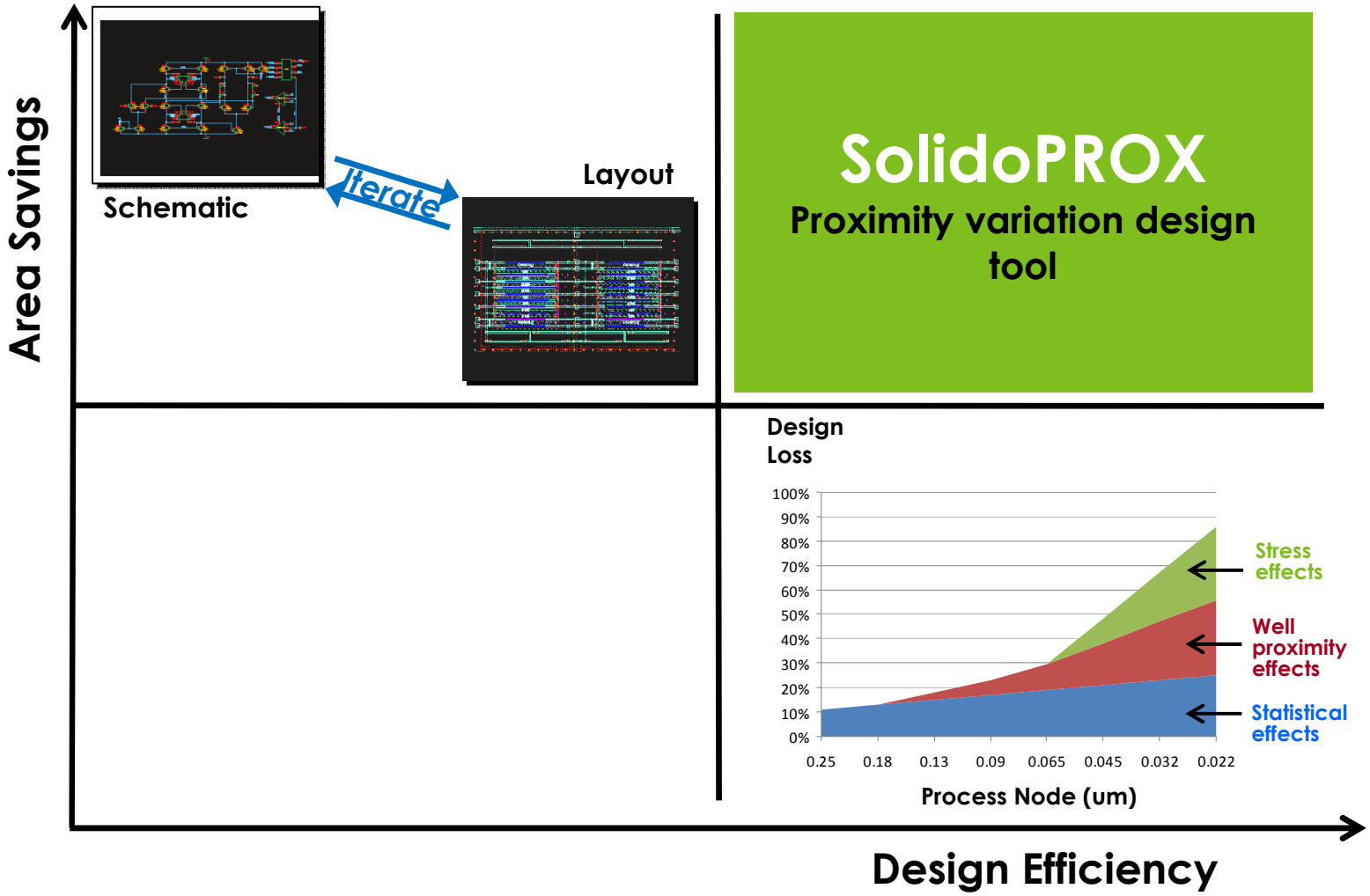
Save Design Time While Saving Area 90nm and Smaller



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Conclusions

- True Corners give a better representation of distribution
  - Local variation
  - Global variation
  - Environmental conditions
- True Corner design preserves the familiar corner driven flow
- Epistemic uncertainty allows you to design around undetermined problems
- One can design for proximity effects *before* layout