Presentation Title: The Challenge of "Realizing a 45nm System on Chip for Digital TV in the Age of Variability”

Andy Appleby NXP

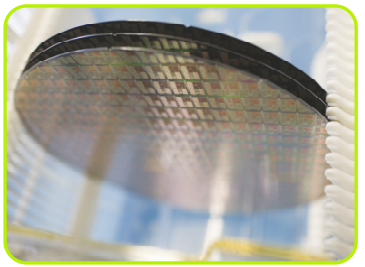
Introduction – The Challenge of "Realizing a 45nm System on Chip for Digital TV in the Age of Variability"

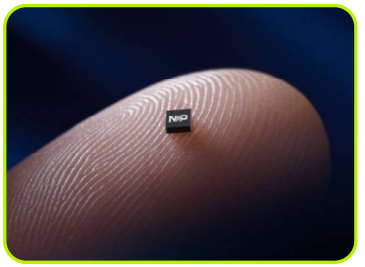
1. Background: NXP/PNX85500	(Who are we? what do we do? What is PNX85500?)
2. The Complexity Challenge	…of realising a very complex Consumer SoC ASIC for DTV)
3. The Impact of Variability	… managing the shrinking Design space
4. Physical Design Closure-Timing	Modes, Corners and Margins
5. Physical Design Closure-DFX	Design for "Excellence"
6. Summary and What Next	Working smarter and harder!

1. Background: Vibrant Media…

An R&D powerhouse

- NXP employs around 6,000 engineers to ensure optimal product creation
- Investment of about $1.2 billion in R&D in 2008 *)
- 5,700+ patent families
- 20 R&D centers located in 14 countries





NXP is the Leader in Vibrant Media Technologies

- NXP Semiconductors is the leader in vibrant media technologies that help engineers and designers develop products that deliver better sensory experiences. We invest to extend our Philips heritage as innovators in semiconductor solutions, from systems on a chip to single-function ICs and software
- Our vibrant media technologies make it easy to bring your product ideas to life. Creating better sensory experiences for consumers: brilliant images, crisp clear sound, and easy sharing of information in homes, cars, and mobile devices. All with exceptional effectiveness and efficiency. With NXP, you gain a competitive advantage that can be seen, heard, and felt
- With NXP as a partner, you can be more successful by bringing products to life that deliver better sensory experiences

ess which was largely part of the ST-NXP Wireless JV in 2008

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1. Background: Digital TV

Home

Lead in focus areas

- Leading in picture quality developments for TV, Set-Top Box (STB) and PC TV, with:
  - Motion Accurate Picture Processing: first to remove all artifacts from HDTV motion pictures
  - Best digital natural motion
  - Integrate MPEG4 decoding in TV IC
- Introduced the industry's first digital TV processor manufactured in 45nm technology
- Top 3 player in digital video systems (incl. DTV and STB) with the scale to establish a strong leadership position
- 1 out of 2 TVs worldwide contains NXP chip
- #1 in Silicon tuners
- #1 in PC TV, with 1 in 2 PC TVs using our SOC, tuner can, and silicon tuner chipsets

1. Background: PNX85500

Global single-chip HD LCD TV platform

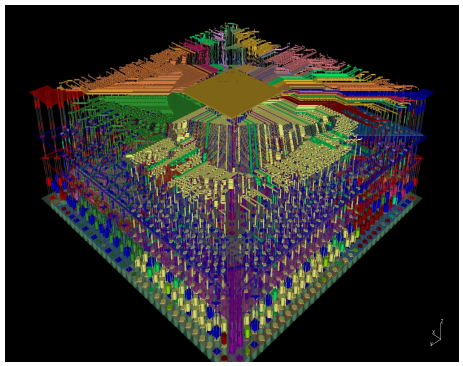
Unparalleled picture quality on mid-range TVs due to NXPs Motion Accurate Picture Processing (MAPP2) technology

MAPP2 dramatically removes the visible halo effect in motion pictures for a picture perfect image with technologies such as frame rate conversion, movie judder cancellation, motion sharpness and vivid color management.

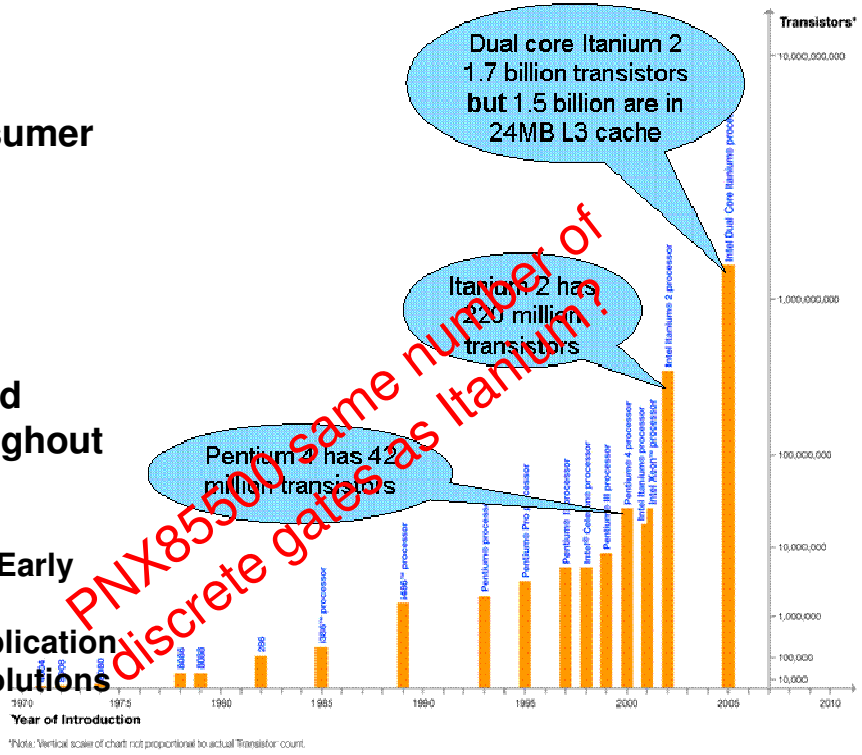
- **Combines industry-leading digital TV processing and picture quality technology into one fully integrated single-chip**
- **TV550 features DVB-T, MPEG4/H.264 decode, HDMI reception and decoding of digital SD and HD content. Supporting global digital TV switchovers.**
- **Ethernet and CI+ security features to for IP TV content, including emerging on-demand TV services,from service providers straight to the TV set.**
- **Provides high-end features including LED (2D) sectional backlight dimming, for optimum contrast with 50% lower power.**

2. The Complexity Challenge

PNX85500 Technology & Complexity



- **Most complex physical design challenge in NXP history**
  - biggest SoC, most IPs and fastest speed.
  - first 45nm – new variability effects
  - Low levels of replication
  - first SoC in flipchip
- **Most aggressive ASIC schedule in NXP history**
  - IP and SOC challenges handled concurrently
  - Predictable design closure
  - Right First Time…aggressive Time to Market
- **Strong cost focus in incredibly competitive consumer semi-conductor market**
  - Aggressive cost pressures...
  - "Plain vanilla" 45nm technology platform in TSMC
- **Success through "Global Partnership" – EDA and manufacturing partners and expert groups throughout NXP**
  - Developed new flows and new ways of working
  - Addressing Potential Issues before they occurred Early Analysis
  - Achieving Predictable Design Closure through application of technology driven but Pragmatic engineering solutions to variability issues.



2. The Complexity Challenge

PNX85500 Overview:

PNX85500 First Time Right

Functional 45nm CMOS Silicon

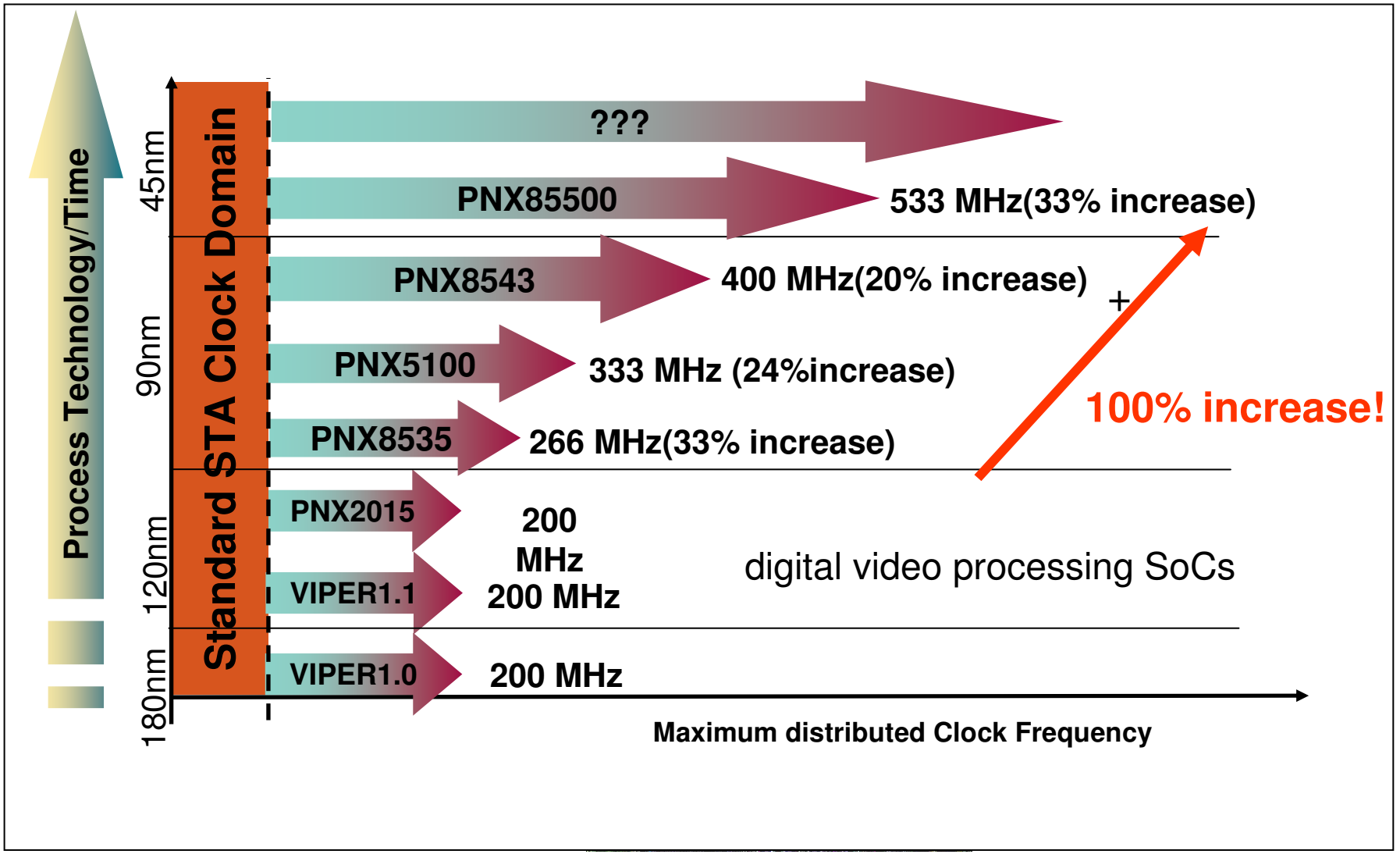
- PNX85500 the industry's first digital TV processor in 45nm CMOS
- NXP's first product in 45 nm CMOS
  - complex mixed signal SoC introduced in a new node from scratch to first gds product tape-out in 18 months

First Video Ouput from PNX85500

- The first flip chip packaged samples arrived after 8 wks of total throughput time in Southampton and are functional
- Congratulations to all teams with this achievement, realized through concurrent engineering of BU Home DTV, Operations Backend Innovation, Corporate I&T and TSMC

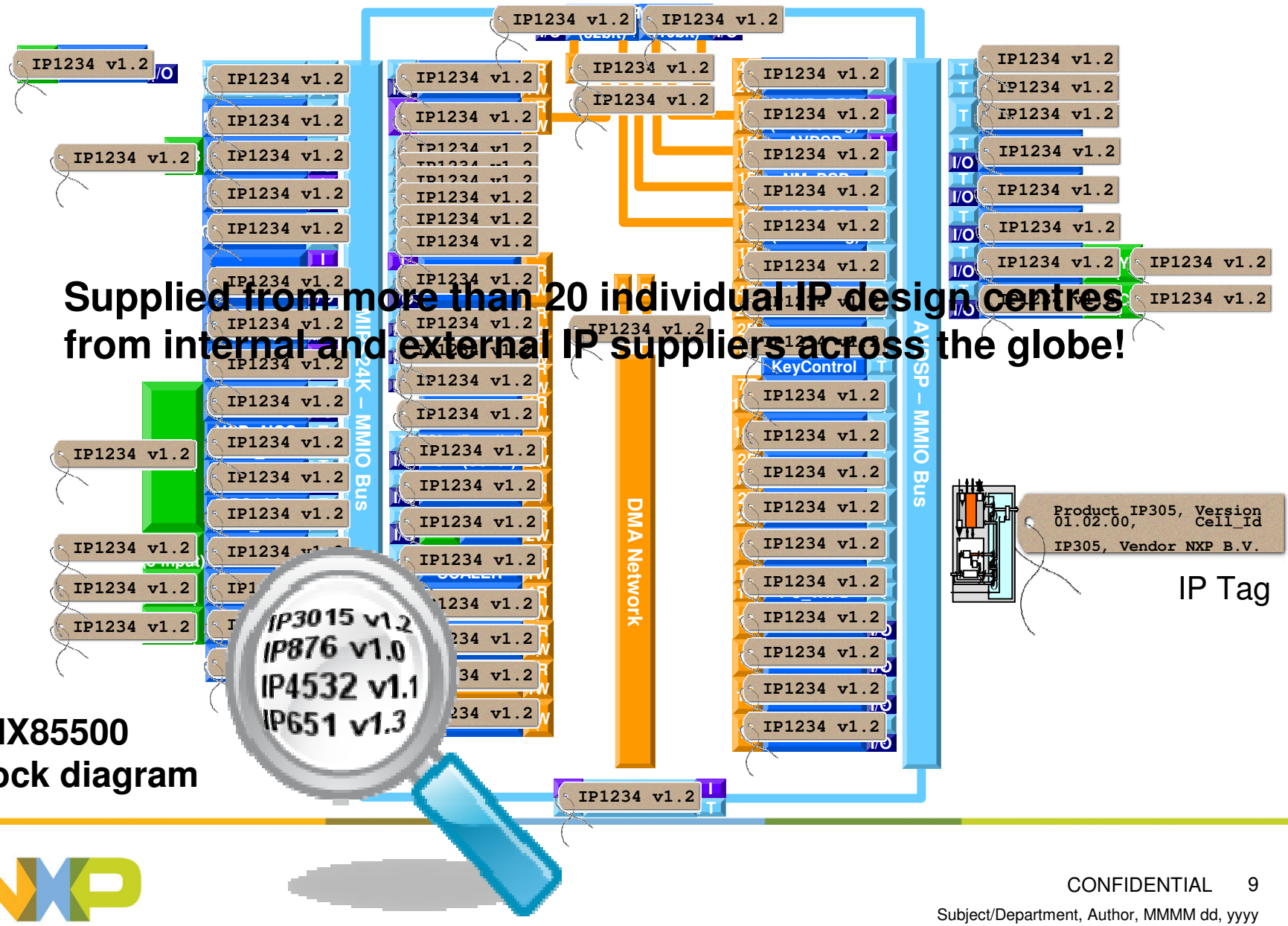
2. The Complexity Challenge

Moore's law at work:



2. The Complexity Challenge

PNX85500 – lots of IP content:

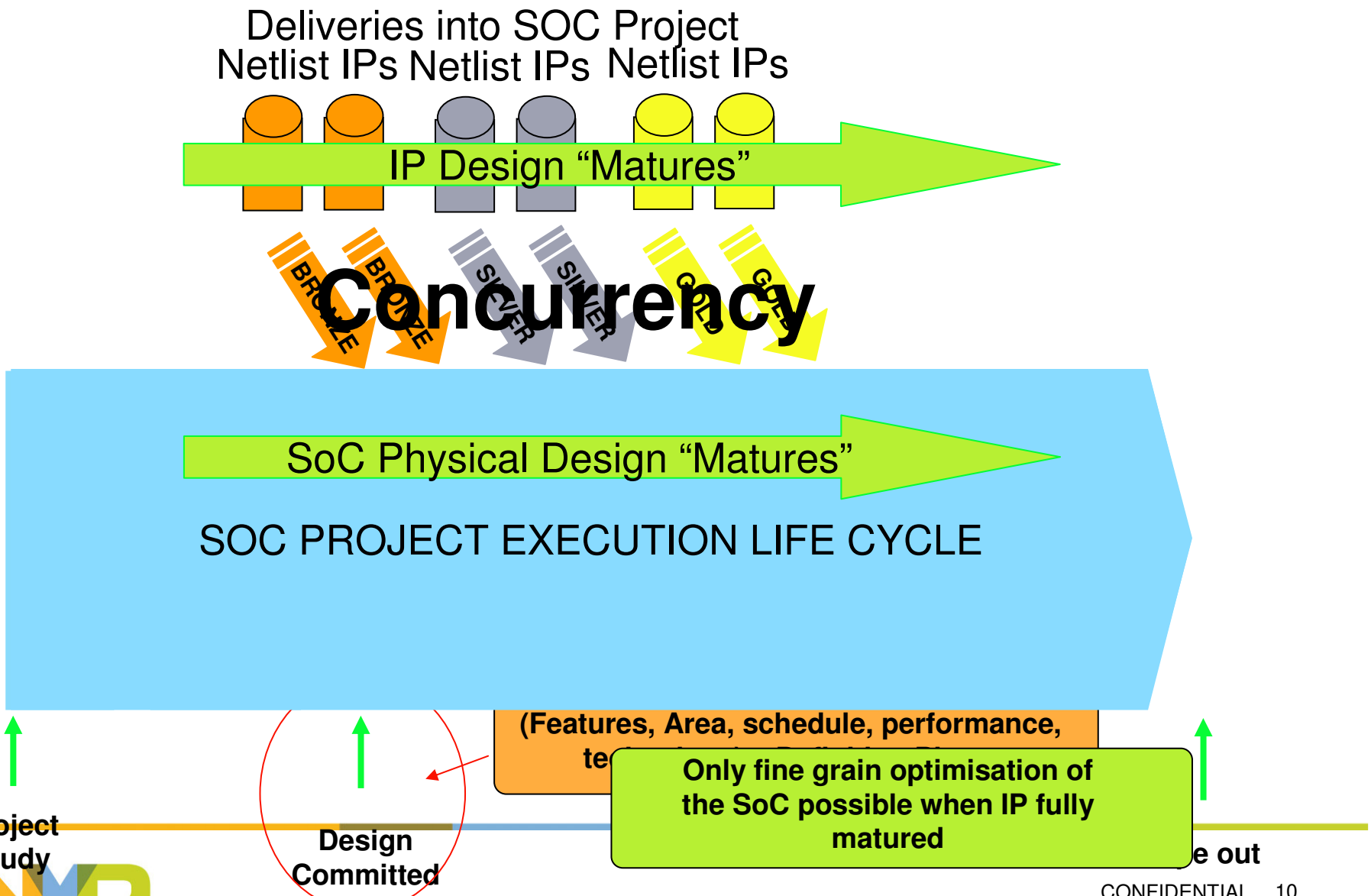


Supplied from more than 20 individual IP design centres from internal and external IP suppliers across the globe!

PNX85500 block diagram

2. The Complexity Challenge

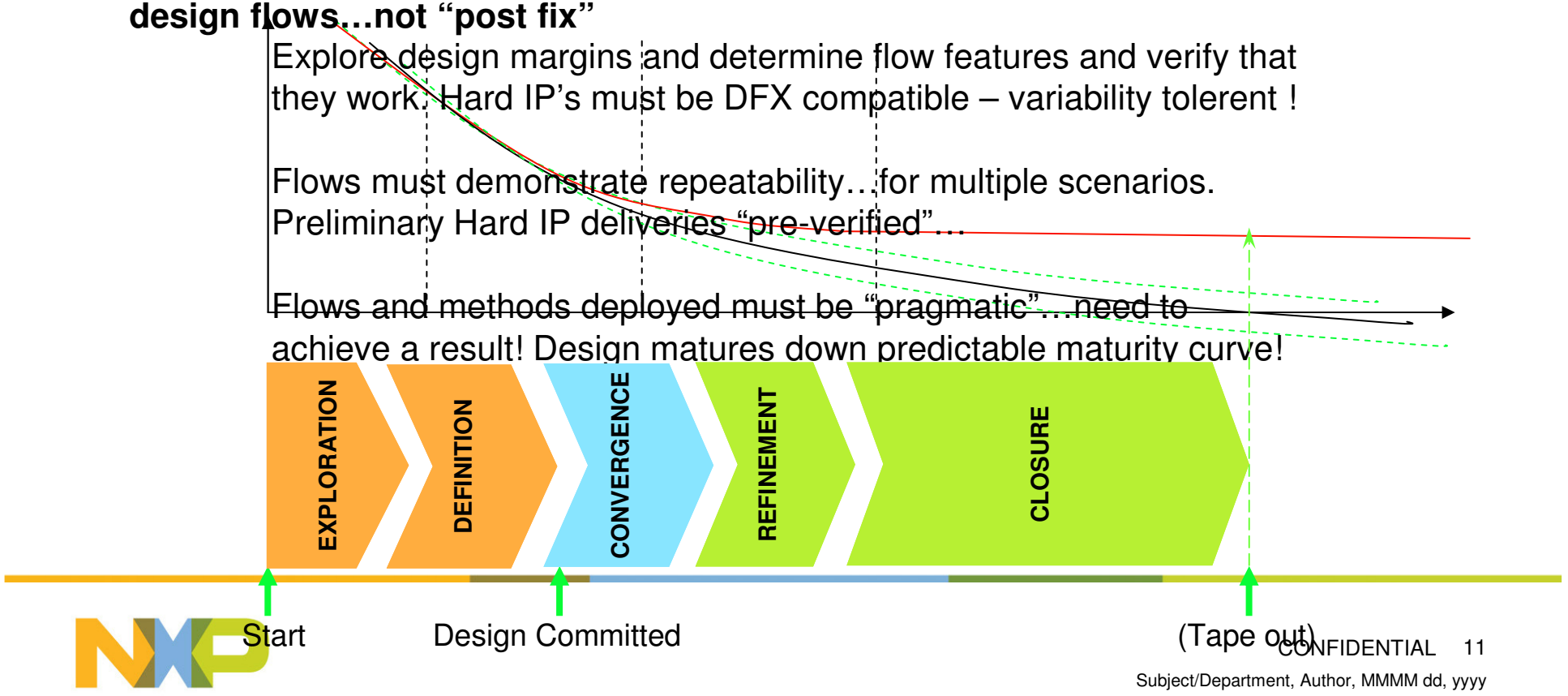
Concurrent Design



2. The Complexity Challenge

Predictable Convergence:

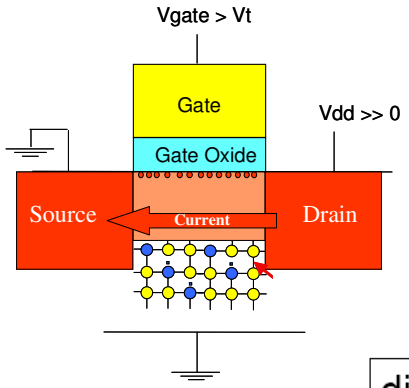
- **Must be able to predict that the design will converge within the committed design limits (timing, DFX, IR etc)…**
- **Cannot afford any big surprises during Closure Phase!**
- **Early Analysis through prototyping all aspects of the design identifies what action to take to determine convergence!**
- **Strategy for "managing variability must be built in to the IP delivery model and SoC design flows…not "post fix"**



3. The Impact of Variability

On timing

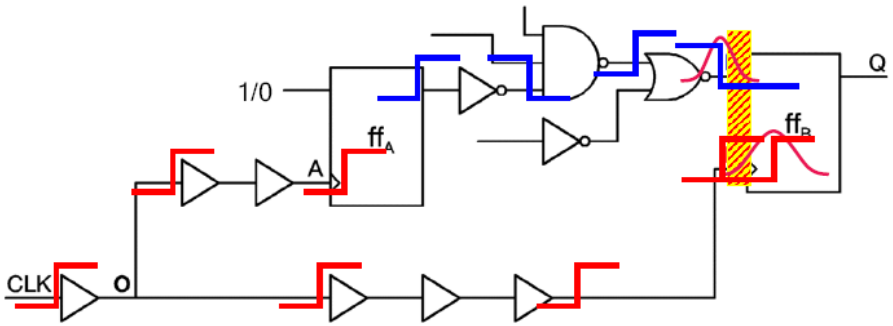
- In C045 the amount of drive current for two identically drawn minimum dimensioned transistors can be significantly different…resulting in different delays.
- Some of the variation can be due to systematic effects. The variation can occur lot to lot, wafer to wafer, die to die or gate to gate!
- Some of the variation can be totally random due to dopant fluctuations, line roughness, or interface state issues in the channel…due to very small dimensions of the transistor gate at 45nm and below...
- Local (gate to gate) variations (random and systematic) need to be treated carefully since they can result in timing failures



→1 doping atom for 10^4 atom of silicon/ cm3

→ ~ 180 doping atoms for 10 millions Silicon atoms

digital design + variability ⇨ timing uncertainty

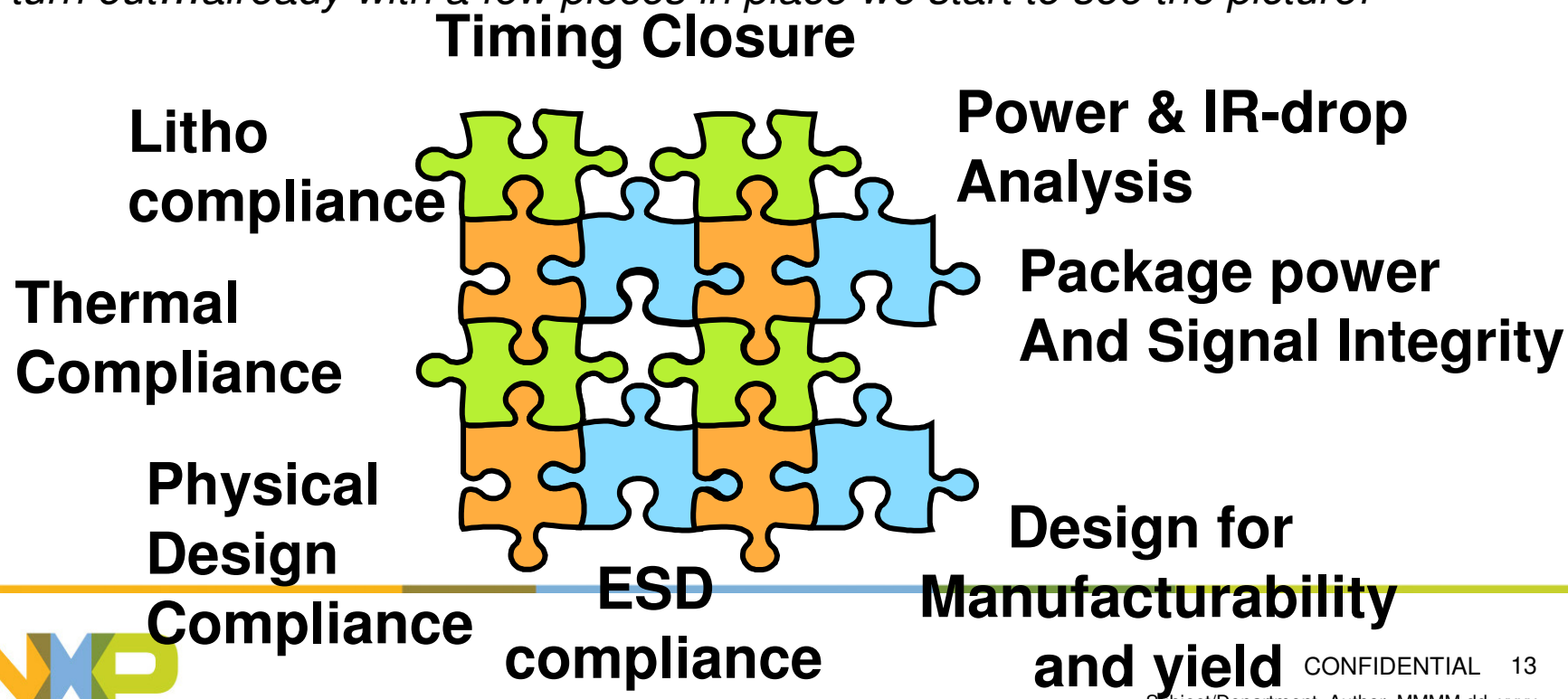


3. The Impact of Variability

Ideally: Create a local and global conditions, so that every transistor sits in a homogeneous environment and functions correctly within the characterised performance range?

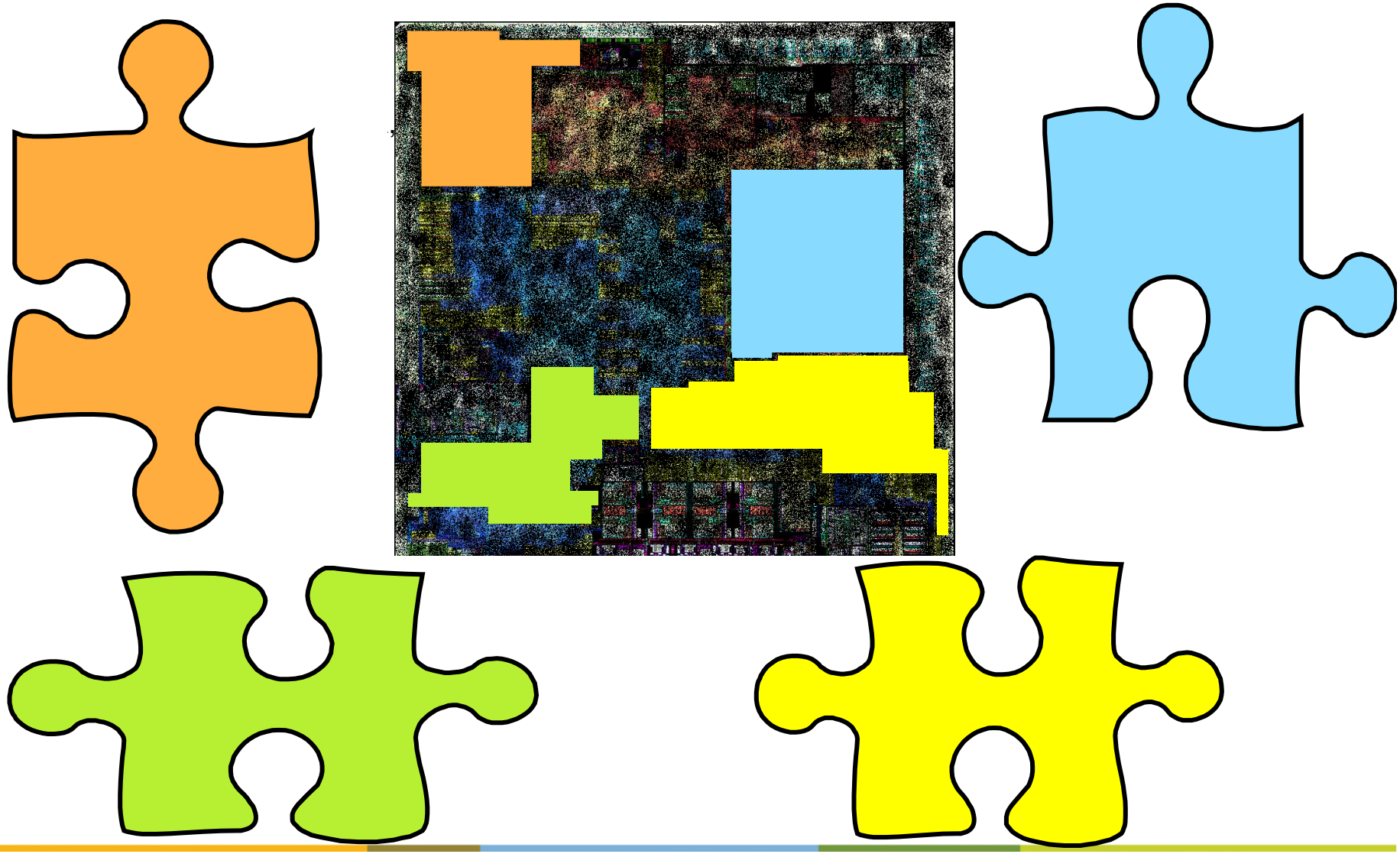
Practically: Minimise systematic variation as much as possible and margin design (include random effects)

Physical Design Closure is like building a complex jigsaw puzzle with pieces missing…! We need to start assembling the picture to see how it's going to turn out…already with a few pieces in place we start to see the picture!



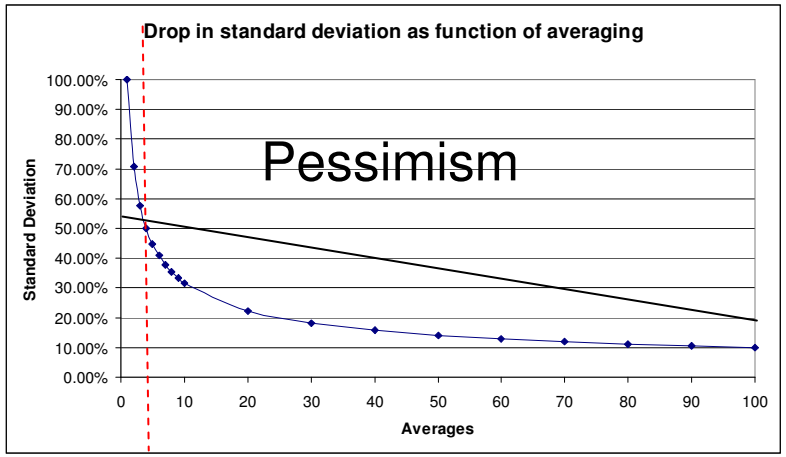
3. The Impact of Variability

Where Variability fits



3. The Impact of Variability

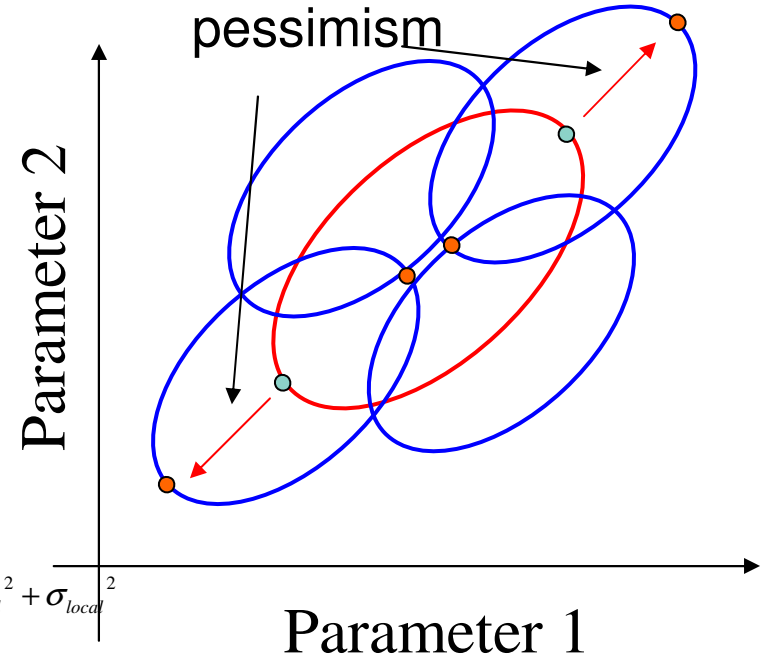
- Variability is essentially managed in 2 ways:
- 1. Minimise systematic effects by homogenising local environment that transistor/gate sits in. Trying very hard to make every transistor sit in an equivalent environment…
- 2. Margin for random effects and residual systematic effects after (1).



$$\sigma_{total} = \sqrt{N \cdot \sigma_{stage}^{\ 2}} \text{ (where N is the number of stages)}$$

- Margin comes in the form of characterisation limits, clock uncertainties (setup and Hold) and OCV.
- Margining the design has tendency for pessimim...

Strategy for Managing Variability



$$\sigma_{total}^{\ 2} = \sigma_{global}^{\ 2} + \sigma_{local}^{\ 2}$$

Global :

A die can be anywhere in global region (Die-to-die, wafer-to-wafer, lot-to-lot and mask-to-mask)

Spectre: “process”: “process” variation is the same for all instances in a simulation

Local (Intra die):

Individual transistors then vary in their corresponding local area

Within die variation obtained from mismatch data.

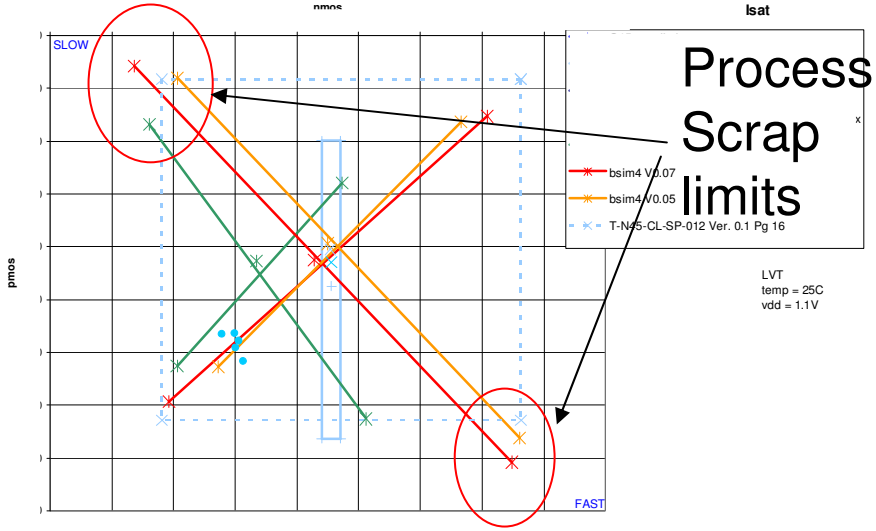
Spectre: “mismatch”: Mismatch variation is different for each instance in a simulation

4. Physical Design Closure-Timing

Timing Sign-off PVT:

- One of the greatest challenges of SoC Design is Timing Closure.
- Protecting the specification means identifying modes and corners for optimisation and sign-off
- The library characterisation corners protect the scrap limits of the process -typical performance parameter for speed is IDsat. Interconnect parameters for wire RC delays increasingly improtant
- Multiple Modes and Corners identified to protect the application “design space”…voltage, temperature and frequency

	WCCOM		NCCOM	LTCOM		WCCOML		OCV
	cworst	cbest	typical	cworst	cbest	cworst	cbest	
Application Mode (setup/hold)	✓		✓		✓	✓		
Scan Shift (setup/hold)	✓		✓		✓	✓		
Scan Capture (setup/hold)	✓		✓		✓	✓		
BIST (setup/hold)	✓		✓		✓	✓		
IO Timing	✓				✓	✓		
Max Transitions Timing (clock)	✓		✓		✓	✓		
Crosstalk (application mode)	✓	✓	✓	✓	✓	✓	✓	
Critical IO Timing	✓		✓		✓	✓		
Critical Clock Paths (what-if analysis; MSR analysis)	✓		✓		✓	✓		

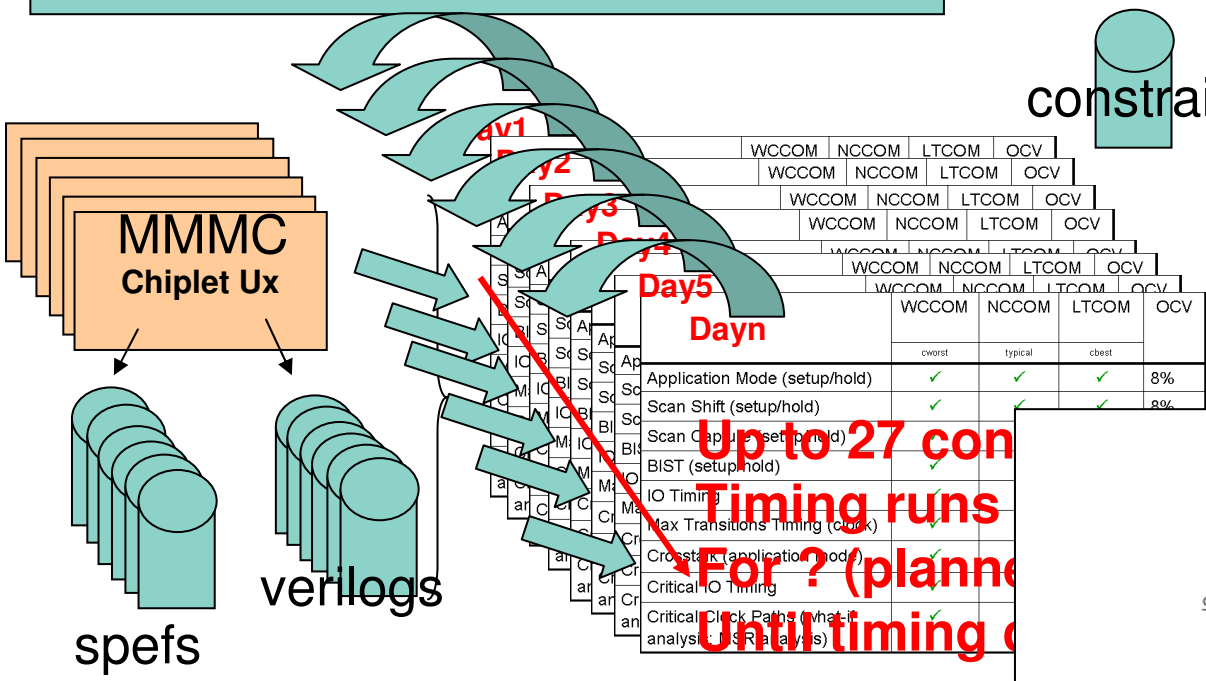


STA Corner	Voltage (V)	Temperature (C)	Process	Extraction
LTCOM	1.21	-40	FF	Cbest
NCCOM	1.1	25	TT	Typical
WCCOM	0.99	125	SS	Cworst25
WCCOML	0.89	-40	SS	Cworstm40

Corner	Voltage (V)	Temperature (C)	Process	Extraction
LTCOM*	1.21	-40	FF	Cbest
LTCOM	1.21	-40	FF	Cworstm40
NCCOM*	1.1	25	TT	Typical
WCCOM	0.99	125	SS	Cbest
WCCOM*	0.99	125	SS	Cworst25
WCCOML	0.99	-40	SS	Cbest
WCCOML*	0.99	-40	SS	Cworstm40

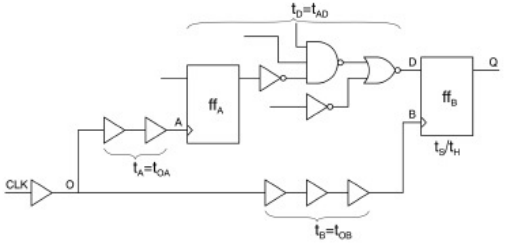
4. Physical Design Closure-Timing

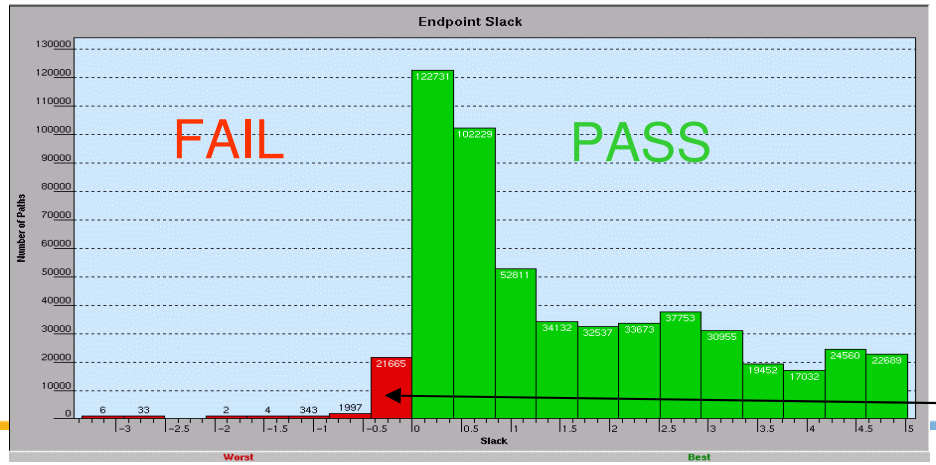
Static Timing Analysis



Timing "closed" when all timing paths for all modes and corners meet specified Performance Requirement!

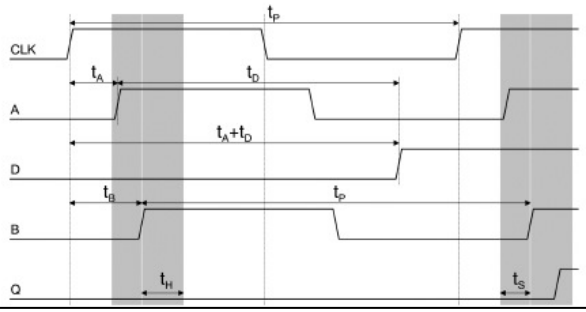
Up to 27 con
Timing runs
For ? (planne
Until timing c





Hold constraint can be expressed as follows: $t_A + t_D \geq t_B + t_H$

Setup constraint can be expresses as follows: $t_A + t_D \leq t_B + t_P - t_S$



Apply timing ECOs to correct violations

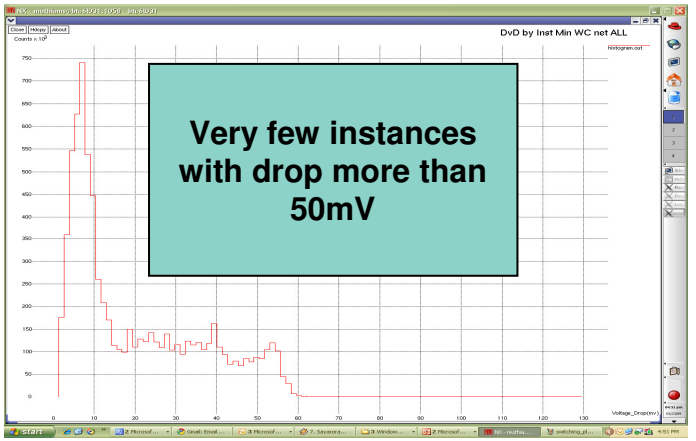
Consequences of Margining

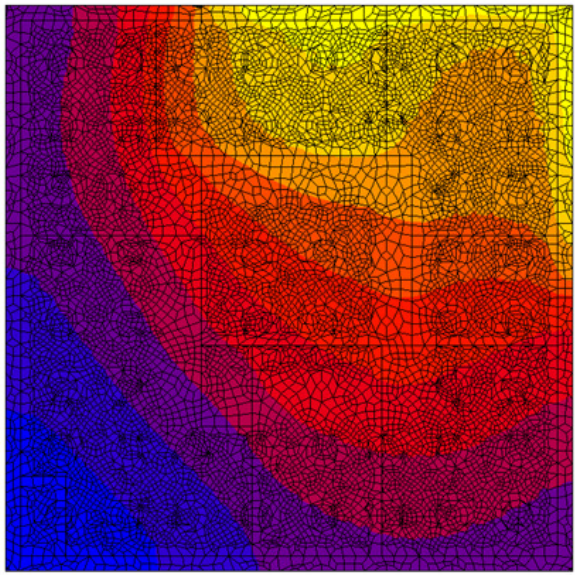
- Achieving Timing Closure is increasingly difficult at 45nm and beyond…!
- The range of possible path delays (fastest to slowest) for All corners is much greater than previous process generations…due to systematic and random delay variation factors…
- If we apply conservative margins…as for earlier technologies, designs become "unclosable"…we must take specific action to reduce the spread…
- Management of systematic variability effects allow some margin reduction…performance spread is still large though - design window is reduced!
- MMMC optimisation techniques can cope better with performance spread – automatically working within the design window. Expect longer run times.
- Result: <2% increase in post route optimisation utilisation – acceptable.
- Conclusion: Overal timing closure task is significantly more difficult than it was for early process generations, but tools – if used correctly – offer significant mitigation.

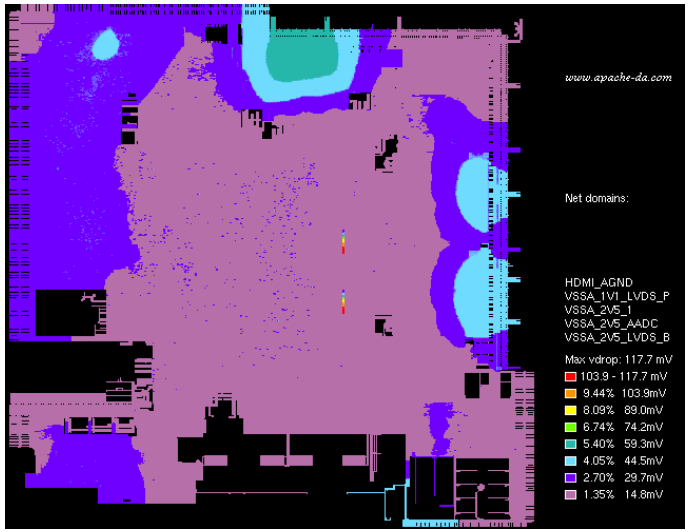
4. Physical Design Closure - DFX

Power/static/dynamic IR-drop/thermal

- Target IR
  - 55mV total static IR-drop
  - 100-150mA max bump current
- Achieved IR
  - 46mV total static IR-drop
  - Most of chip <10mV drop
  - Dynamic - most of chip < 50mV
- Thermal Gradient <10degC

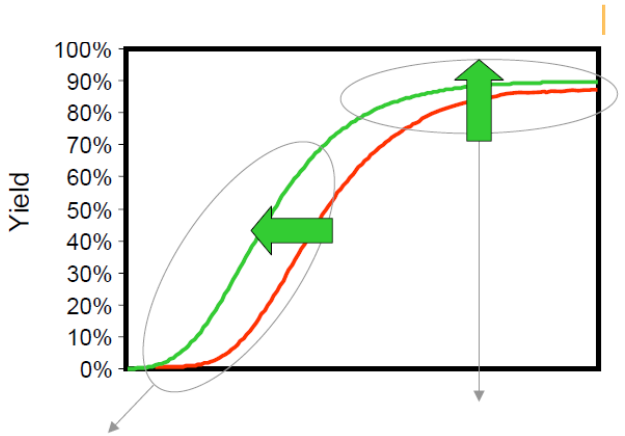






4. Physical Design Closure - DFX

Apply DFX strategy



DfM in Phase1:
Desensitize to systematic yield loss
→ **Time-to-Market**

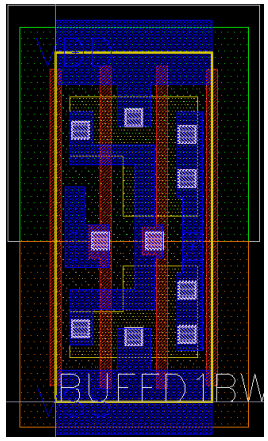
DfM in Phase2:
Desensitize to random defects
→ **Die price**

Yield Loss Contributors

- Yield = Yrandom * Ysystematic * Yparametric * Ytest
- **Critical Area Analysis (CAA)**
  - DfM reduces the critical area by wire widening, wire spreading, via doubling and therefore the sensitivity for random defectivity. Based on defect models validated by fab with process monitors.
    Represents Yrandom
- **Lithography Analysis (Litho)**
  - Litho requirements are part of DRM. Level-1 Litho hotspots are yieldkillers.
    Part of Ysystematic
  - The electrical effect of litho CD variations can be extracted for gates and interconnect.
    Part of Yparametric
- **Chemical Mechanical Polishing Analysis (CMP)**
  - Density and density gradient requirements are part of DRM. CMP adds a model-based simulation to detect yieldkillers hotspots.
    Part of Ysystematic
  - Extraction of thickness variations can highlight parametric effects due to CMP.
    Part of Yparametric

4. Physical Design Closure - DFX

- “Standard” IP delivered variability aware by foundary:

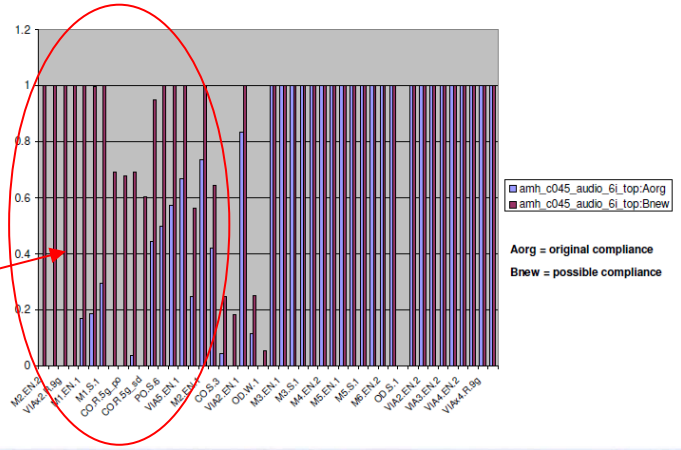


Recommended rules
Could be applied at no
Area penalty

- Custom IP goes through rigorous IP “screening” process…checked “Early” – pre-completion and again for IP sign-off.
- DFX checks include Litho, CAA, CFA, CMP (small components create array)
- For CAA Look for outliers…

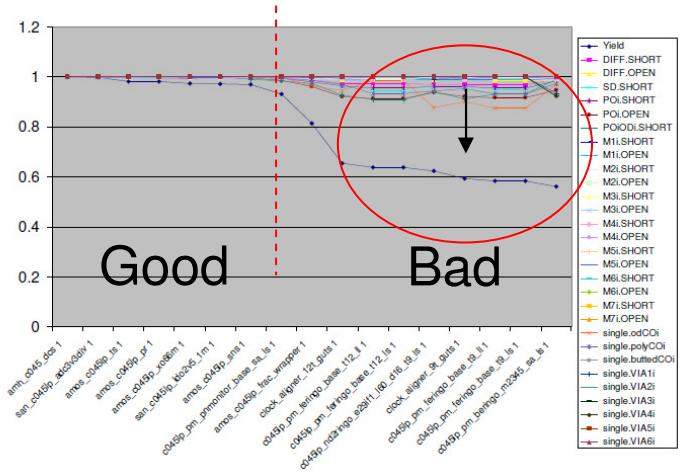
IP DFX screening:

Results – CFA, 1 cell sample



Mentor Graphics IP Analysis, NXP Ian Smith Mentor Confidential 11

Results - CAA



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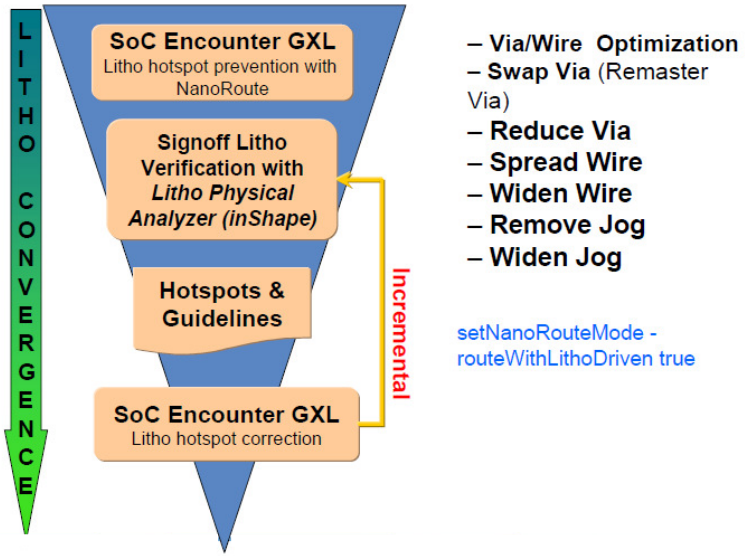
5. Physical Design Closure-DFX

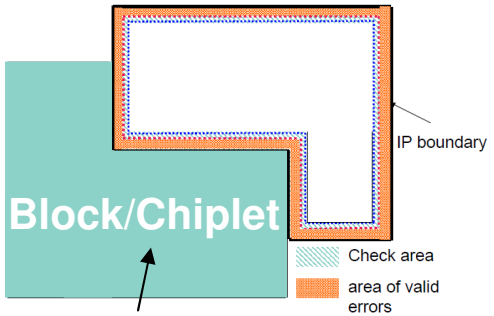
DFM Aware Place and Route and sign-off

- Litho issue avoidance during routing prevents 80% of the potential errors
- Hierarchical sign-off Litho analysis is a must due to huge demands on memory and cpu time
- Blocks/chiplets are checked post-route – 10 hours 24cpu
- Litho issues very short range effect <1um
- Only Block/chiplet boundaries are checked at top level…very fast – 2hours
- Final “Full Flat” check carried out only as sanity check – initiated at TO – 5days 32cpu concurrent with mask-making.

Litho Prevention with NanoRoute

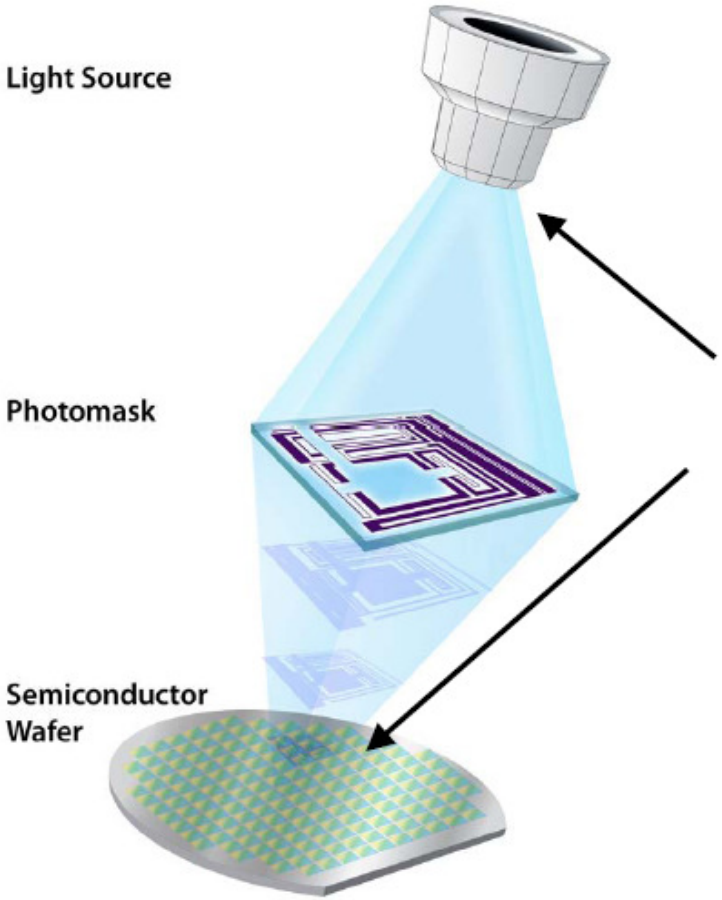


Hierarachy Lithography Checks



Litho Error Classification:

Sources of Lithographic Variability



Two main sources of lithographic variability

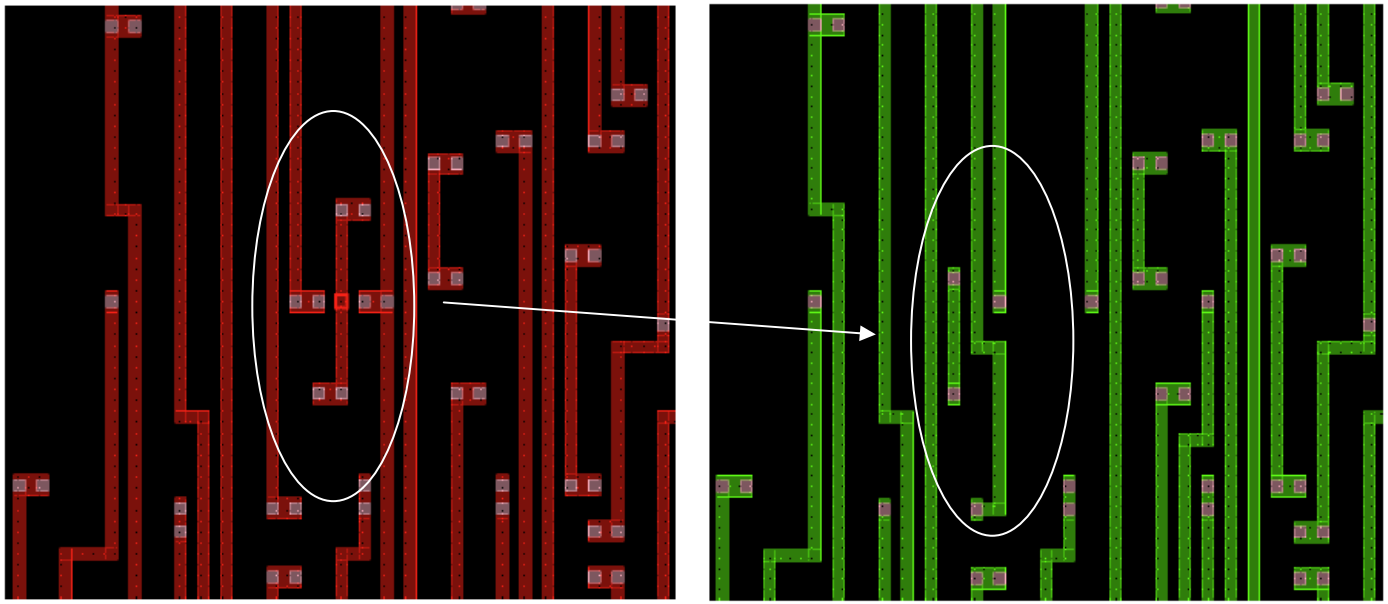
- **Exposure dose**: variation in intensity
- **Focus: variation** of wafer in **z** axis
- Both define the **"process window"**: How far can you get from nominal processing, and still meet tolerances

Litho Analysis and fixing

M5 Level-1 repair

Pre-repair

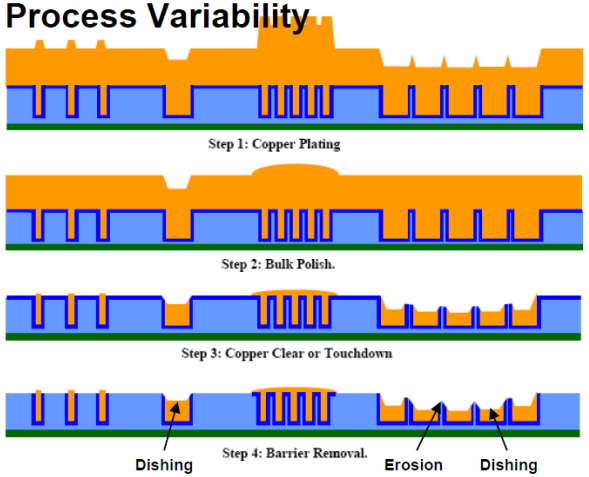
Post-repair



5. Physical Design Closure-DFX

CMP – Density/Gradient Analysis:

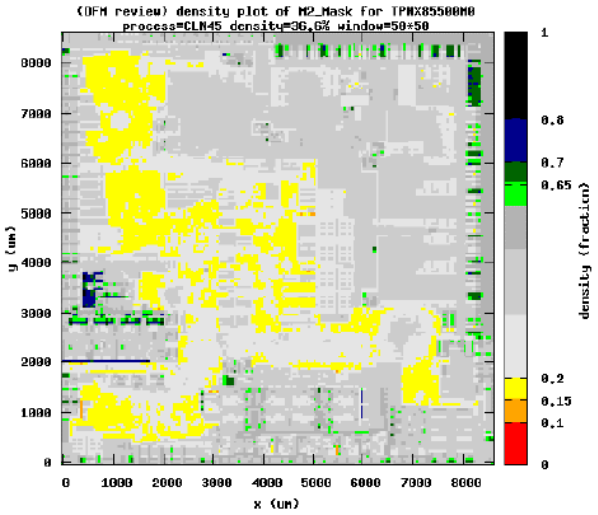
CMP Process Variability



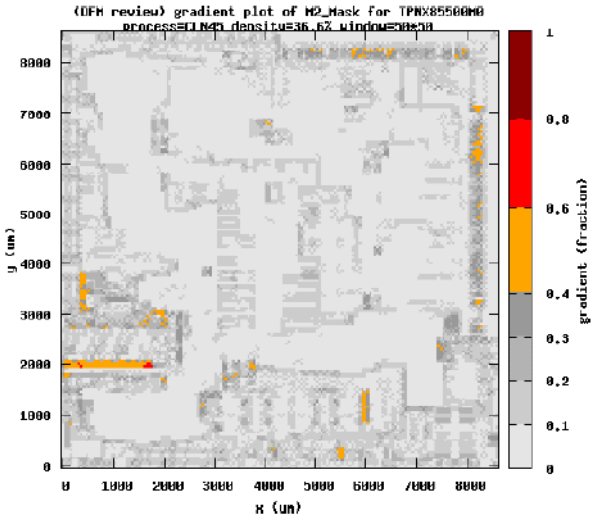
- Dishing & Erosion add up from layer to layer => transfer to layers above

- Rule based “Density Fill”
- Rule based Density and density gradient analysis (DRC) is augmented by Model Based sign-off CMP Analysis in pre-TO check.
- Fill patterns adjusted with different tile geometries

Metal 2 (Density)



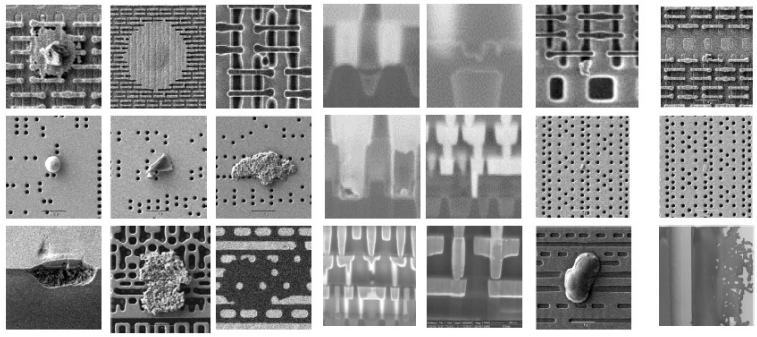
Metal 2 (Gradient)



5. Physical Design Closure-DFX

Critical Area/Feature Analysis:

CAA : examples of 'random' defects



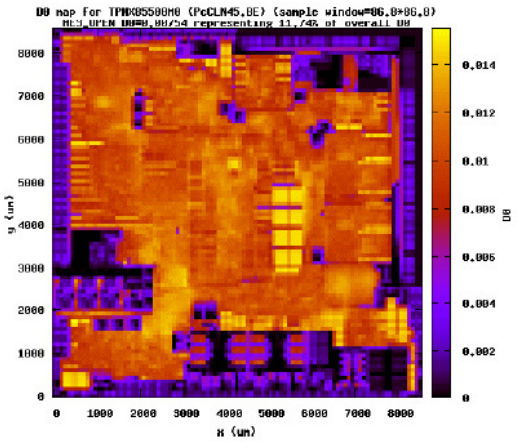
– Often randomly distributed across wafers

– Easy to characterize and model

– **Yield loss is "design dependent"** : Some designs are more sensitive then others

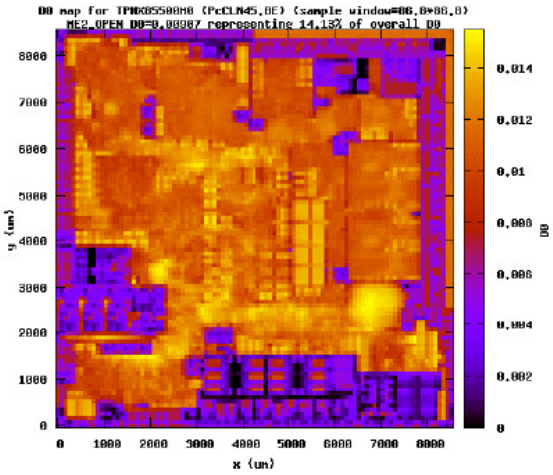
- Random routing defects addressed by DFM aware routing: via doubling medium effort, wire spreading.
- Augmented by CAA "sanity checks" at pre-TO check. Little scope to make significant changes…

M3 Open



Observation: Sensitivity to ME3 opens and shorts => nothing really special (Homogeneous density everywhere on the routing)
Recommendation: NA

M2 Open



Observation: Sensitivity to ME2 opens and shorts => nothing really density everywhere on the routing)Recommendation: NA

5. Physical Design Closure-DFX

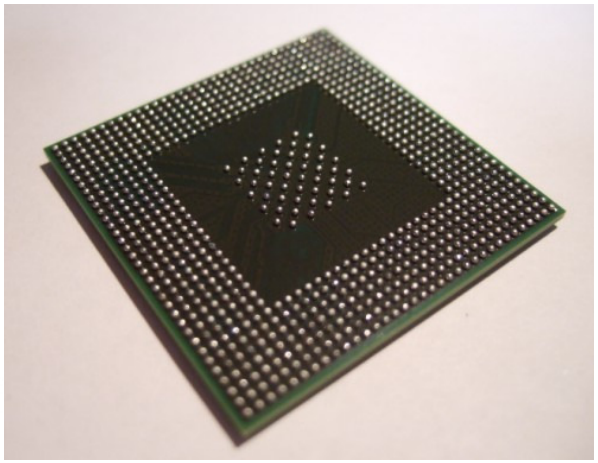
Summary:

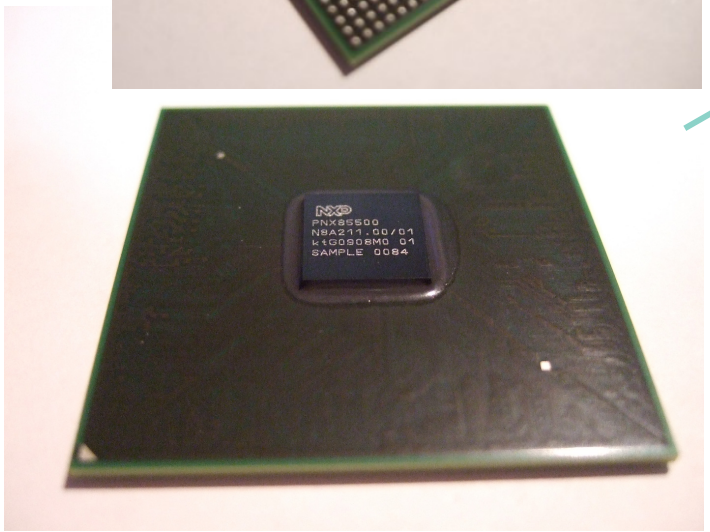
- In advanced process nodes like 45nm susceptability to systematic and random process variation is minimised by use of advanced DFM techniques.
- Strategies must be deployed early…in IP creation and before and during place and route phase.
- Timing is then margined to “achievable limits”…
- Fixing issues outside P&R is avoided due to impact on timing closure and cycle time.
- Sign-off is accelerated by using concurrent hierarchical approach.
- A holistic DFX approach is deployed using Litho prevention and fixing, via doubling, wire spreading density fill and local fine tuning of density/density-gradient.

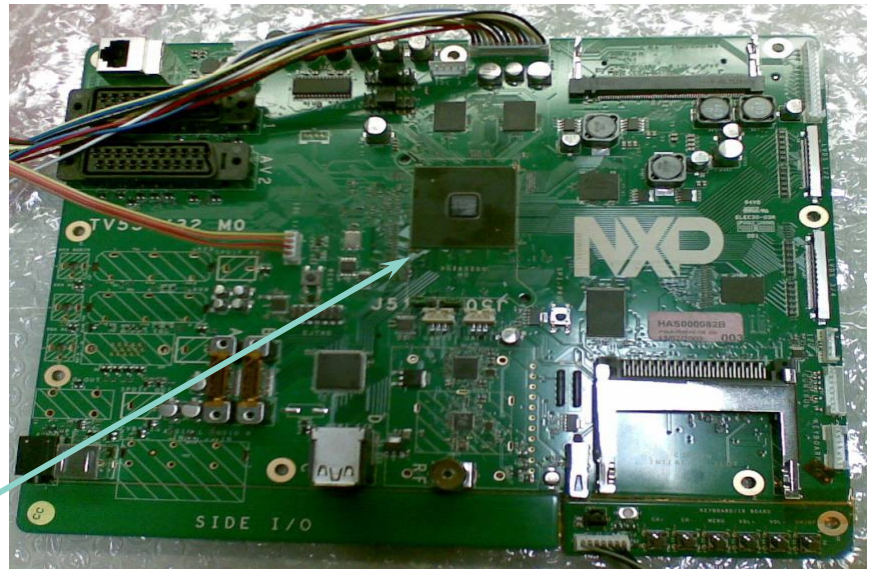
6. Summary and What Next

The Result – The Product!

- The TV550 System Board with the Worlds first fully integrated one chip Digital TV Processor with Full Picture Enhancement - MAPP







Success! From packaged parts received to System bring up in less than 10days…very High level of functionality and performance… Unprecedented for this complexity point!

6. Summary and What Next

Summary

- Variability is now a key factor in SoC Realisation.
- Strategies must take a holistic view of managing the issues…must be embedded transparently into flows and deployed “Early” in IP creation, Place and Route, and Timing Optimisation Cycle…
- Don’t start thinking about variability and how to manage it in Design Closure Phase! Cannot afford any surprises that late… iterating the design could lose a market window!
- Tools work well, but are now quite complex…essential to work closely with EDA partners to get the best from them!
- Be pragmatic…you don’t have to use every feature…it’s about getting the job done.
- Be prepared to work even harder than you already are…!

6. Summary and What Next

What would I like to see next?

- Statistical Timing Sign-off…gain confidence in capability to support sign-off! What about IP statistical timing models?
- Initially would expect to be used to manage sign-off risk of “stubborn violators”…later full sign-off! (maybe derivative designs?)…more robust sign-off!
- Statistical Multi mode Multi corner (V,T) optimisation…”harvest silicon”

- Acknowledgements and Thanks!
- To EDA partners…Cadence, Mentor, Apache, Synopsis for excellent support…
- All colleagues in NXP for presentation material and discussions…
- PNX85500 Team…for exception al efforts in realising this chip!

Any Questions?