Verification Techniques for Advanced Mixed-Signal Design

(A 90nm Transceiver IC designed using VHDL-AMS)

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Paper Content

- Introduction
- Introduction to NFC (Near Field Communication)
- Overview of Mixed-Signal Design Methodologies
- The NFC Transceiver mixed-signal design
- Design Flow & Tools
- Results

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Introduction to NFC (Near Field Communication)

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Near Field Communication (NFC)

- Short range wireless technology allowing two devices to communicate
- Based on existing standards & technologies such as ISO/IEC 14443, 18092
- Operates within the globally available and unlicensed RF band at 13.56 MHz $[\lambda = 22\mathrm{m}]$
- Working distance: 0-10 cm
- Speed: 106 kb/s, 212 kb/s or 424 kb/s

Near Field = Purely magnetic field around conductor loop – less than $\lambda/2\pi$ from loop [antenna]

Two communication modes:

Active: devices have own power supply and communicate by transmitting

Passive: The Initiator device provides a carrier field and the target device answers by modulating existing field. Target device may draw its operating power from the Initiator-provided electromagnetic field.

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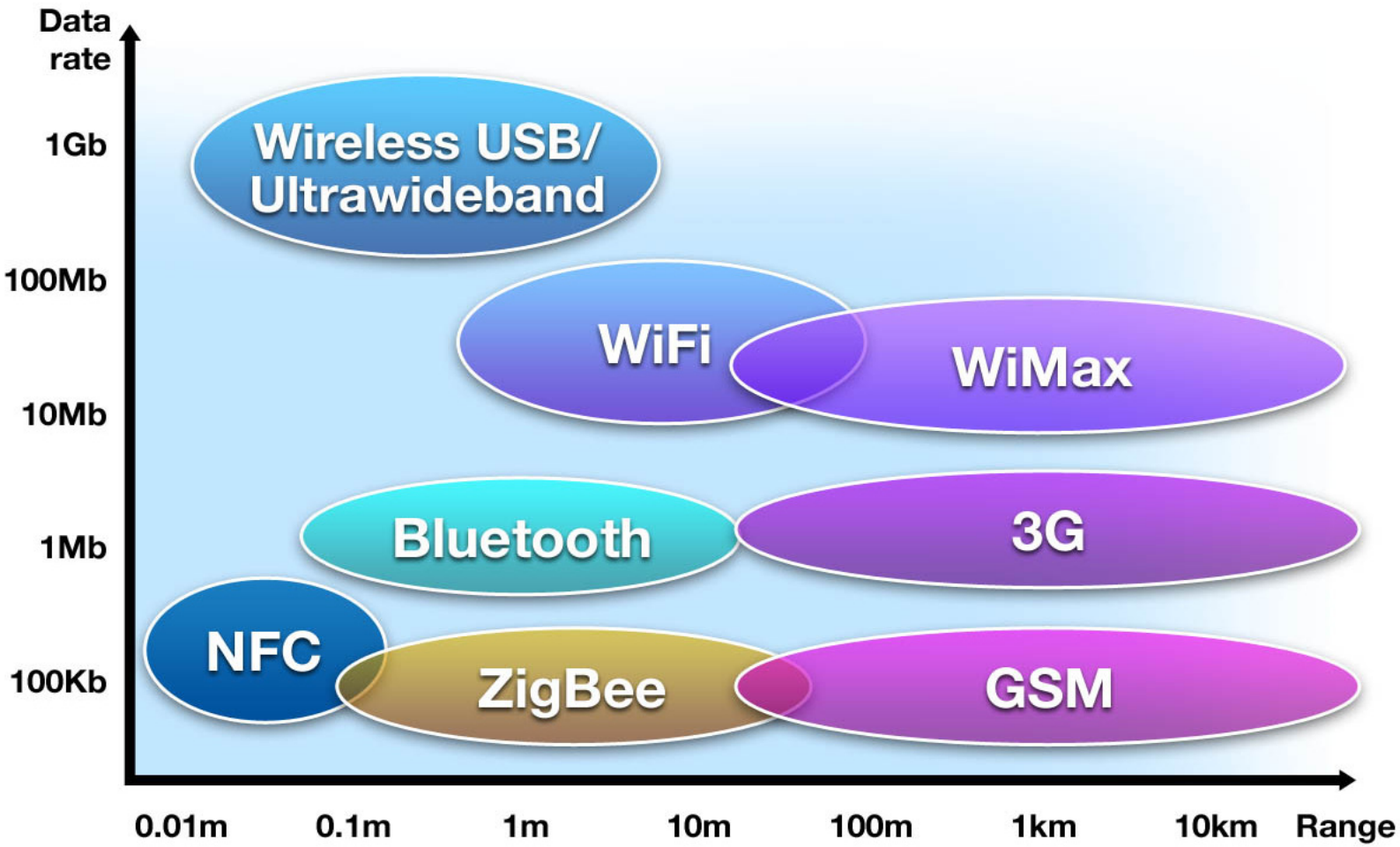
Wireless Market Space



(Source: NFC Forum)

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NFC Has Multiple Uses

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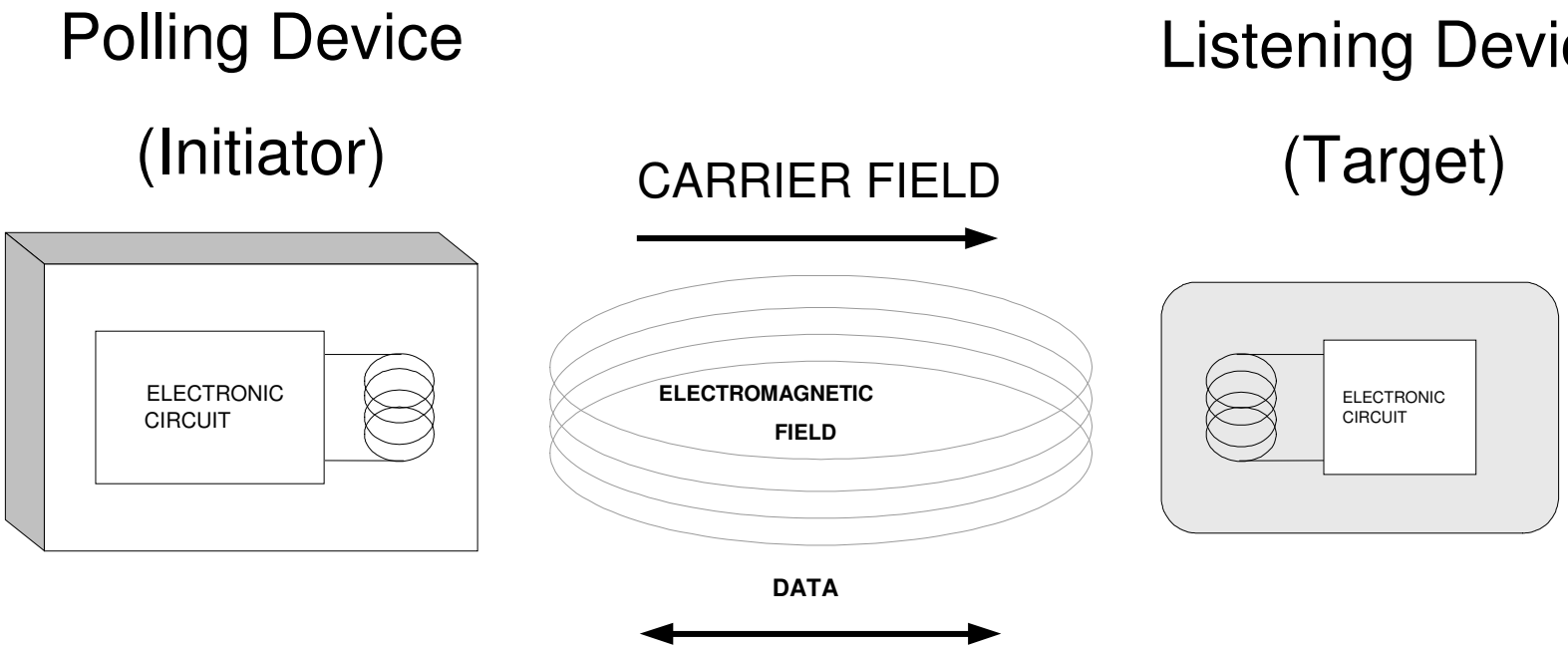
NFC – Magnetic Coupling



NOTE: Short range (up to a few cms) = security

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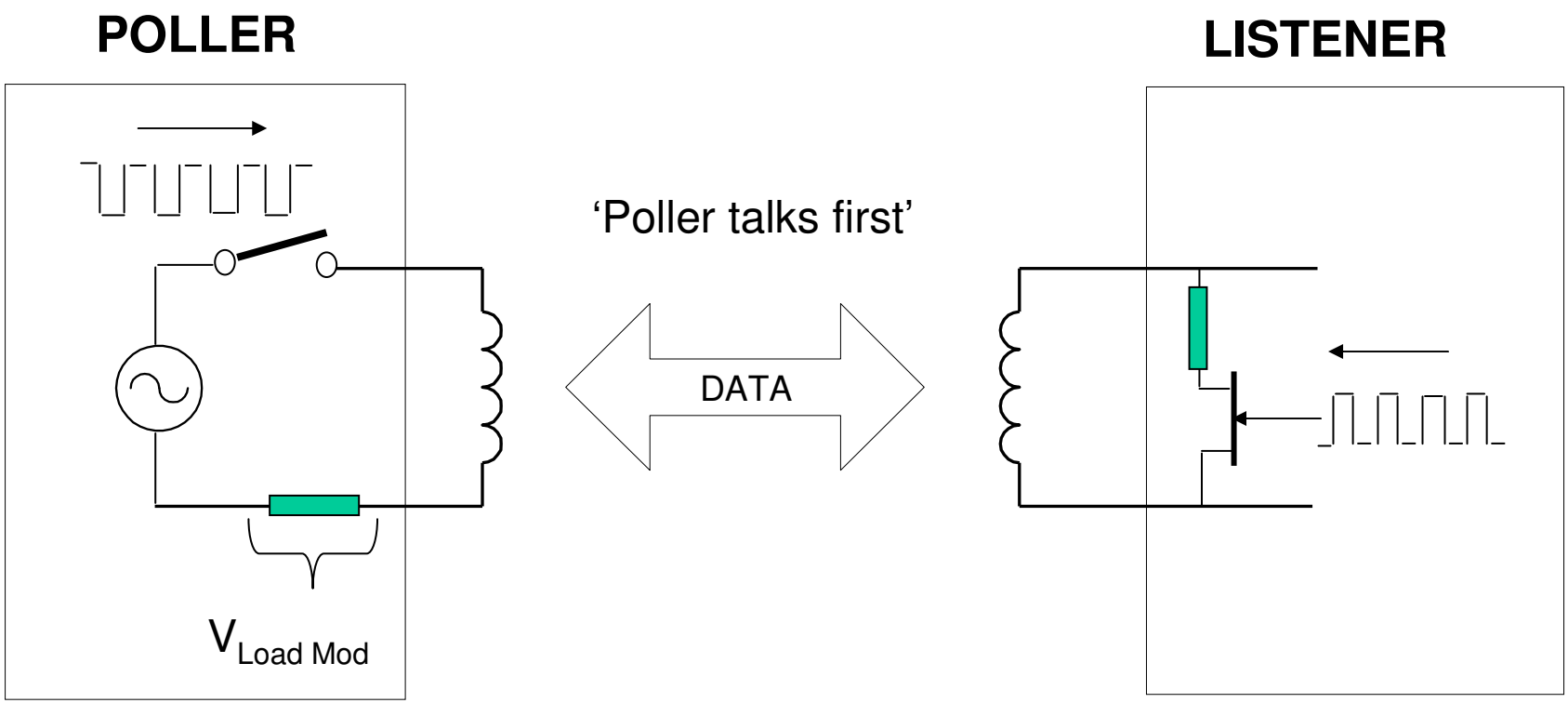
NFC Passive at 13.56 MHz



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NFC device market is building...

Nokia
6131 NFC
2007

Nokia
6212 Classic
2008

Nokia
6216 Classic
2009/10

Samsung
S5230N - NFC
2010

Nokia NFC
Bluetooth
Headsets

Parrot NFC
Bluetooth Speakers
2008

Parrot NFC
Bluetooth Photoframe
2008

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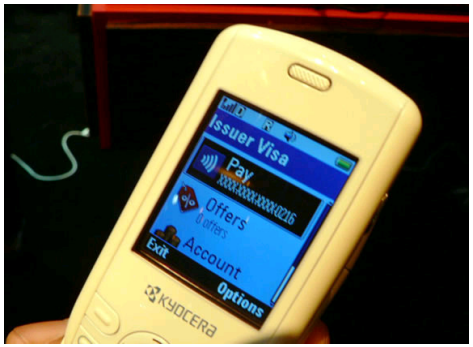
Trial NFC devices…

Sagem
my700X
2006

Samsung
SGH-X700
2006



Kyocera

2007

BenQ
T80
2008

Samsung
D500E
2006/7

Motorola
L7 (SLVR)
2008

LG
KU380 NFC
2009

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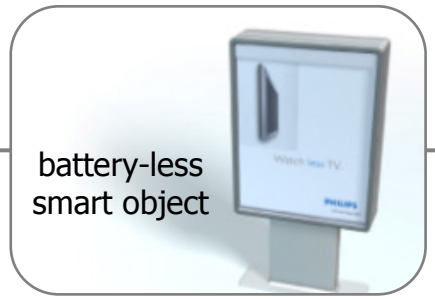
There are 3 Fundamental Operating Modes for NFC

Mode 1
Peer to Peer



Mode 2
Reader Writer

SECURE

Mode 3
Card Emulation

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Mode 1 - Peer to Peer

Two NFC use cases exist

1. **Data transfer between NFC enabled devices using NFC air interface**

2. **Data transfer between NFC enabled devices using another air interface e.g. WUSB. I.e. an NFC thin pipe touch, triggering a WUSB fat pipe (i.e. enabling connectivity)**

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Mode 2 – Reader Writer

Reading NFC Smart Posters

Touch the logo, get the info

Writing to NFC Smart Posters

Touch the logo, leave your info

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Mode 3 - Card Emulation - Ticketing

NFC becomes your travel ticket

No more "Wallet full of cards"

No more "travelling just to top up"

NFC becomes your entry ticket

No more "will it arrive in the post"

No more "will there be any tickets left"

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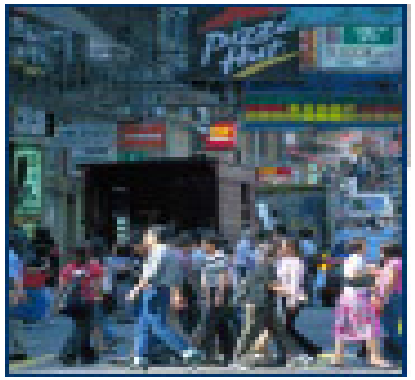
Mode 3 - Card Emulation – Mobile Payment

Smart shopping



NFC becomes your credit card

No more "wallet full of cards"

No more "will it eat my card"

Smart vending

NFC becomes your cash

No more "can you change this fiver"

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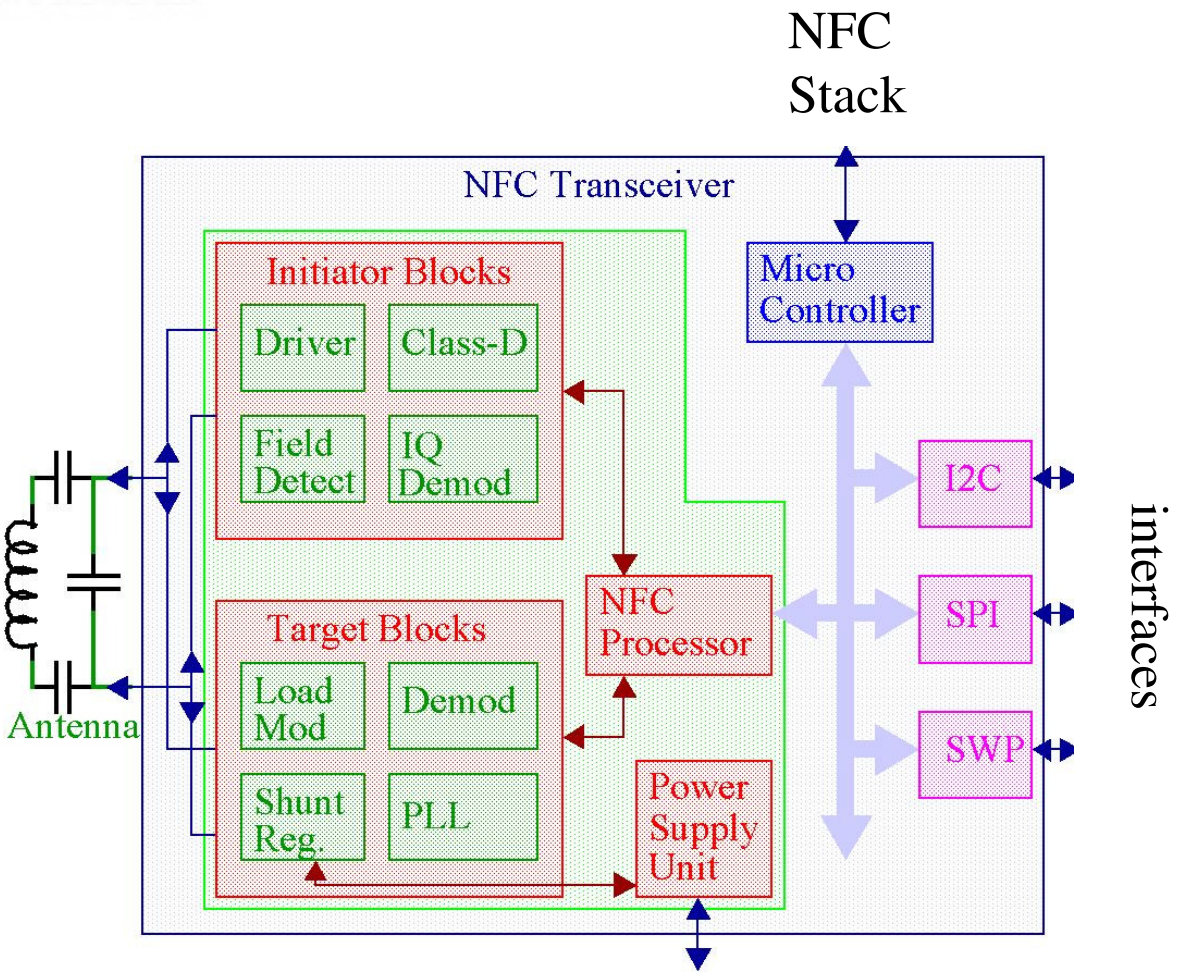
Block Diagram of NFC Transceiver



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Analog/Mixed-signal Design Methodologies

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Bottom-Up Mixed-Signal Design

The traditional approach to design is referred to as bottom-up design.

In it, the design process starts with the design of the individual blocks, which are then combined to form the system.

The design of the blocks starts with a set of specifications and ends with a transistor level implementation. Each block is verified as a stand-alone unit against specifications and not in the context of the overall system. Once verified individually, the blocks are then combined and verified together, but at this point the entire system is represented at the transistor level.

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PROBLEMS with Bottom-Up Mixed-Signal Design

Effective for small designs, BUT for large designs ….. problems:-

- For complex designs, the greatest impact on the performance, cost and functionality is typically found at the architectural level. With a bottom-up design style, little if any architectural exploration is performed and so these types of improvements are often missed.
- Once the blocks are combined, simulation takes a long time and verification becomes difficult and perhaps impossible.
- Any errors or problems found when assembling the system are expensive to fix because they involve redesign of the blocks.
- Communication between designers is critical, yet an informal and error prone approach to communication is employed. With the limited ability to verify the system, any failure in communication likely results in the need of a silicon re-spin.
- Several important and expensive steps in the bottom-up design process must be performed serially, which stretches the time required to complete the design.

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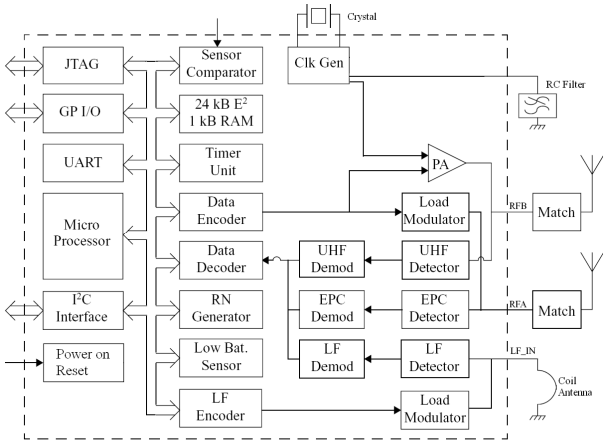
Top-Down Mixed-Signal Design

In a top-down approach, the architecture of the chip is defined as a block diagram and simulated and optimized using a system simulator such as Matlab or Simulink.

From the high-level simulation the performance requirements for the individual circuit blocks are derived. Circuits are then designed individually to meet these specifications.

Finally, the entire chip is laid out and verified against the original requirements.



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Purely Top-Down?

Top-down design only addresses one of the problems we identified earlier with bottom-up design –

that of the first point: "for complex designs, the greatest impact on the performance, cost and functionality is typically found at the architectural level. With a bottom-up design style, little if any architectural exploration is performed and so these types of improvements are often missed".

-> the focus of top-down design is performance and the issue of verification is **not** addressed.

In addition, a traditional top-down design style adds a discontinuity in the design flow that results because the representation used during the architectural exploration phase is incompatible with the representation used during implementation. This discontinuity leaves the block designers without an efficient way of assuring that the blocks all work together as expected.

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solution …..

We need to add functional verification.

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Top-down design & verification

• A top-down design and verification process layers a formal modeling and verification methodology onto a top-down design process.

• A top-down design and verification methodology systematically proceeds from architecture- to transistor-level design. Each level is fully verified before proceeding to the next and each level is leveraged in verification of the next.

• A top-down verification process also formalizes and improves communications between designers. This reduces the number of flaws that creep into a design because of miscommunication.

• The formal nature of the communication also allows designers to be located at different sites and still be effective.

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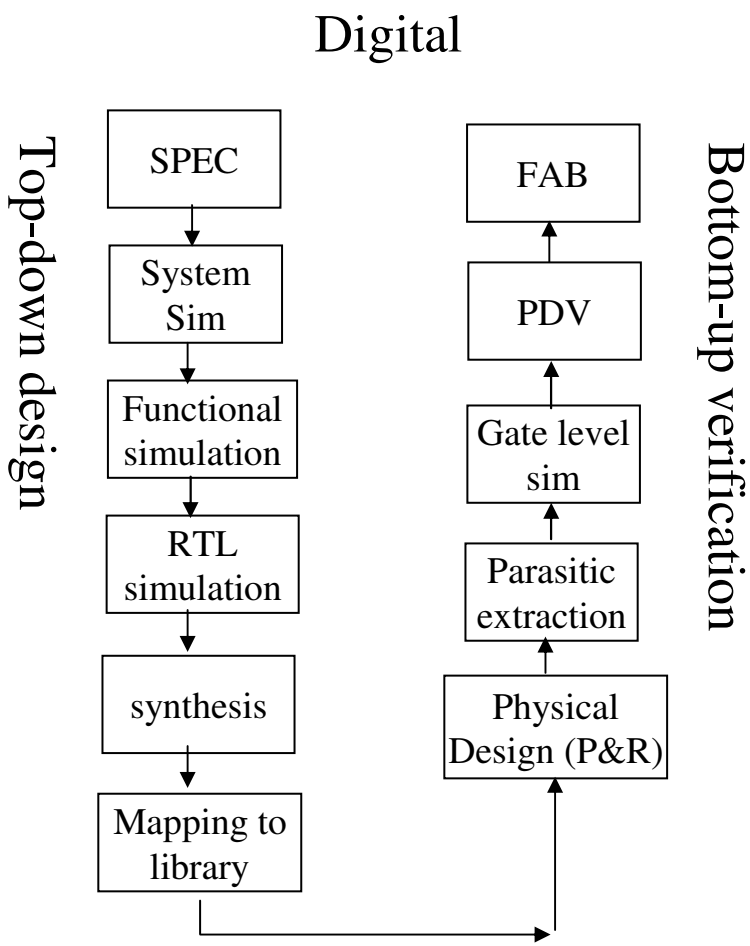
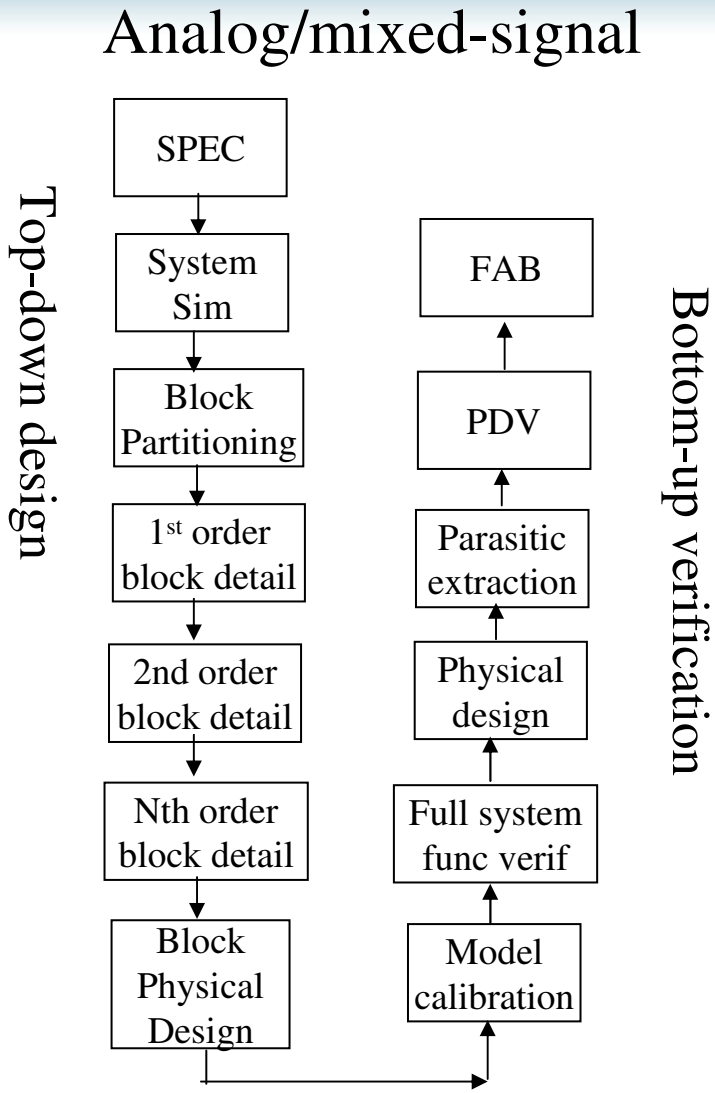
Top-down Design for Digital vs Mixed-Signal





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Languages for mixed-signal design & verification

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VHDL

- traditionally used for digital design and synthesis
- discrete time
- event driven

but

- extensions allow it to be used for analog functions

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VHDL in mixed-signal design & verification

VHDL

- fast simulator (event-driven)
- link with project database (VHDL tool box)
- standard language (IEEE 1076)
- available tool (part of most CAD suites)

Kirchoff "ANAPACK" package [**]

- define type analog, (type RF, etc)
- implements Kirchoff laws using a resolution function

** *NOTE: Anapack is produced and owned by Xemics*

- **Fast (>1ms/min)**
- **Implementation of Kirchoff to handle interactions between blocks**
- **link with schematic database without modifying schematics**
- **minimum overhead (reuse, standard)**
- **widely available tool (=cheap!)**

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VHDL-AMS

- addition of mixed-signal capabilities to VHDL (1999, IEEE Standard 1076.1)
- continuous time signals can be used
- analog quantities – electrical, magnetic, mechanical, etc
- can include other modelling paradigms (e.g. SPICE)
- now supported by most EDA vendor tool-sets

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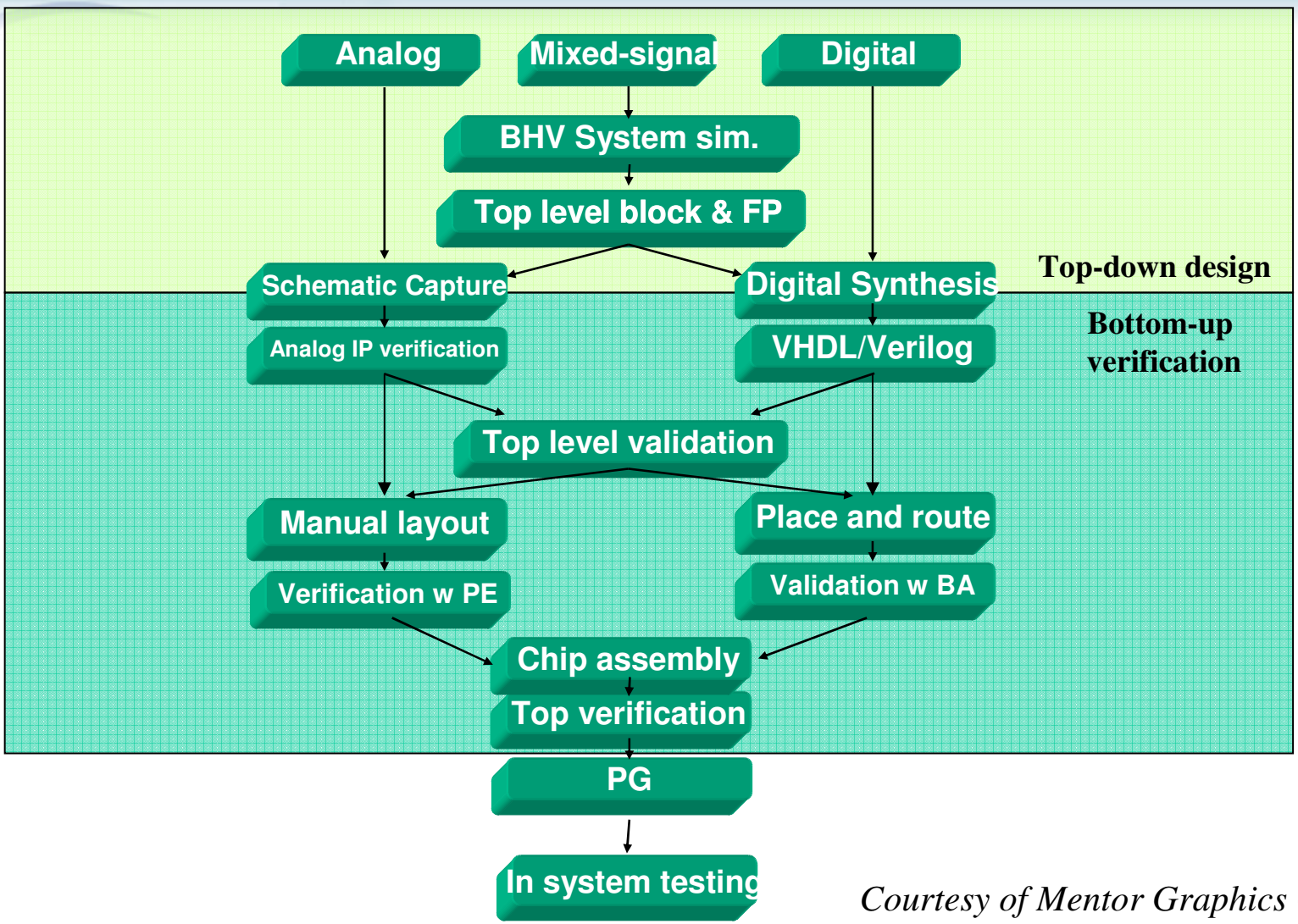
Enabling AMS SoC Design



Courtesy of Mentor Graphics Corp

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Example of NFC SoC Design using VHDL-AMS

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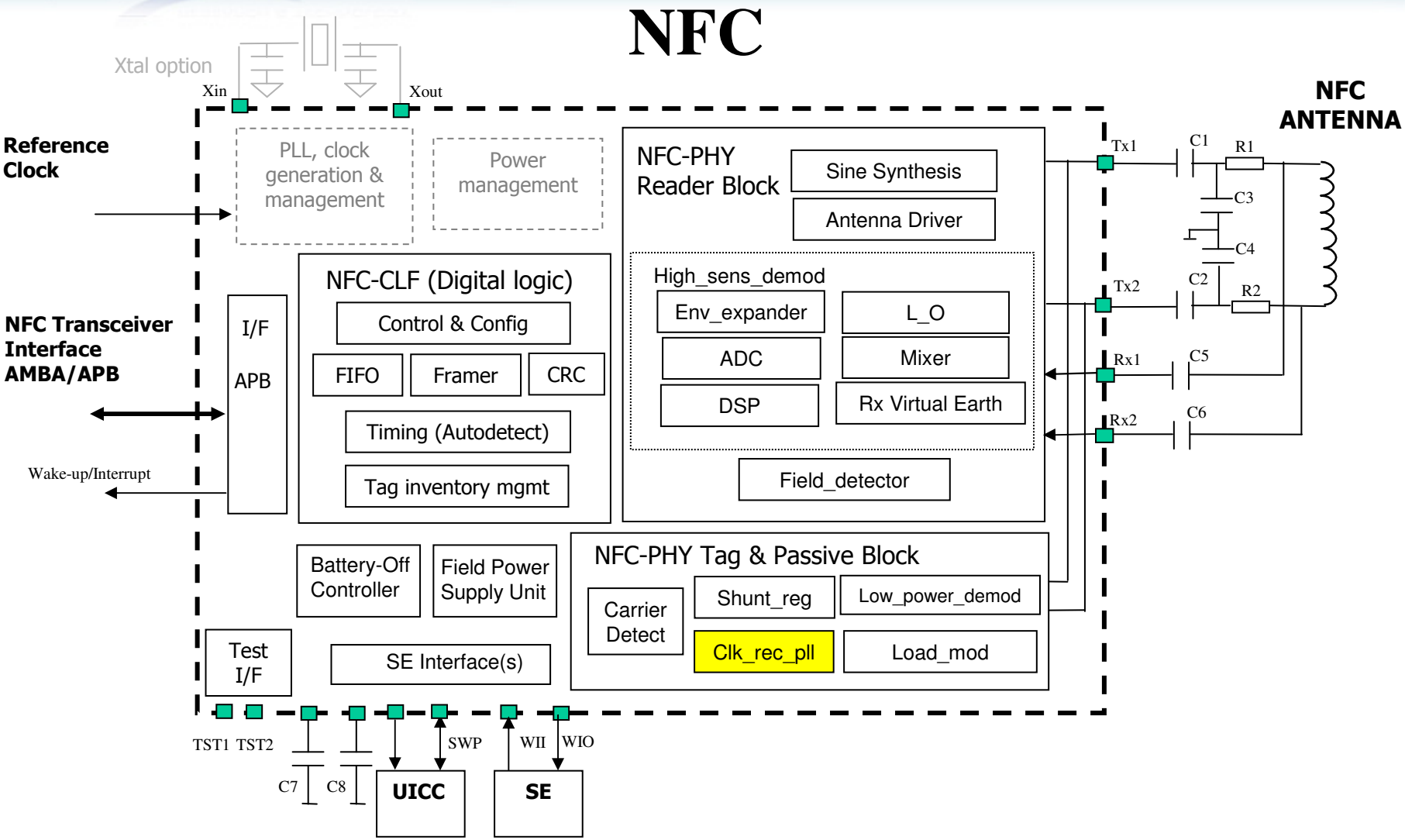
NFC IC



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Design flow used

- Design flow makes use of a VHDL-AMS simulator throughout
  - from early system partitioning stage right through to final design verification stages
- configuration chosen for which view is to be netlisted for the desired simulation
  - e.g. VHDL-AMS models for system partitioning; transistor level Spice views during verification
- Design initially partitioned into digital RTL VHDL and analog VHDL-AMS
  - simulated at this stage using VHDL-AMS simulator
  - uses testbenches written in VHDL and VHDL-AMS
- Same VHDL-AMS simulation and environment may be used through design flow
  - from design/system partitioning to final chip verification
- the design flow using VHDL-AMS complements existing design flows already in place for digital and MS design

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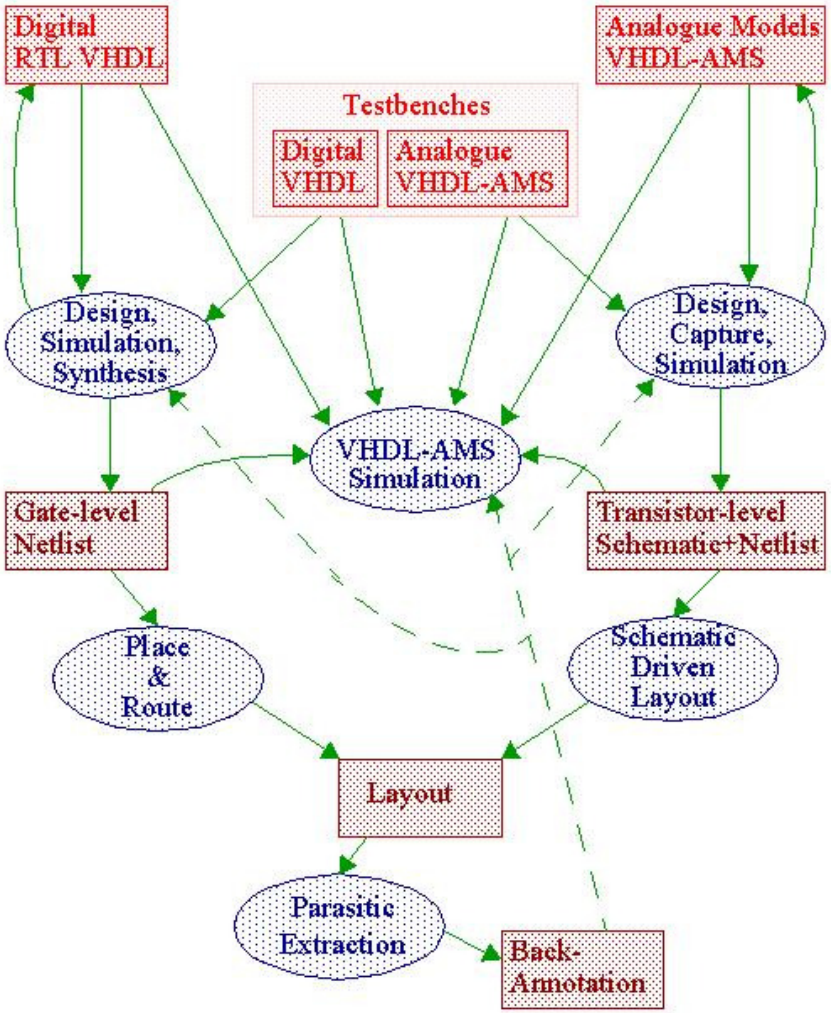
VHDL-AMS Design Flow



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Design tools used

- Industry standard tools
  - **simulation** using Mentor tools
    - ModelSim – digital simulation (or QUESTA/ModelSim)
    - Eldo and ADiT – analog simulation
    - ADVanceMS – combined VHDL-AMS, VHDL and Spice simulations
  - schematic capture and layout using Cadence tools
    - Cadence Composer – schematic capture
    - Virtuoso XL – layout
    - Cadence Hierarchy Editor – netlisting for simulation
  - extraction and physical design verification using Mentor's Calibre

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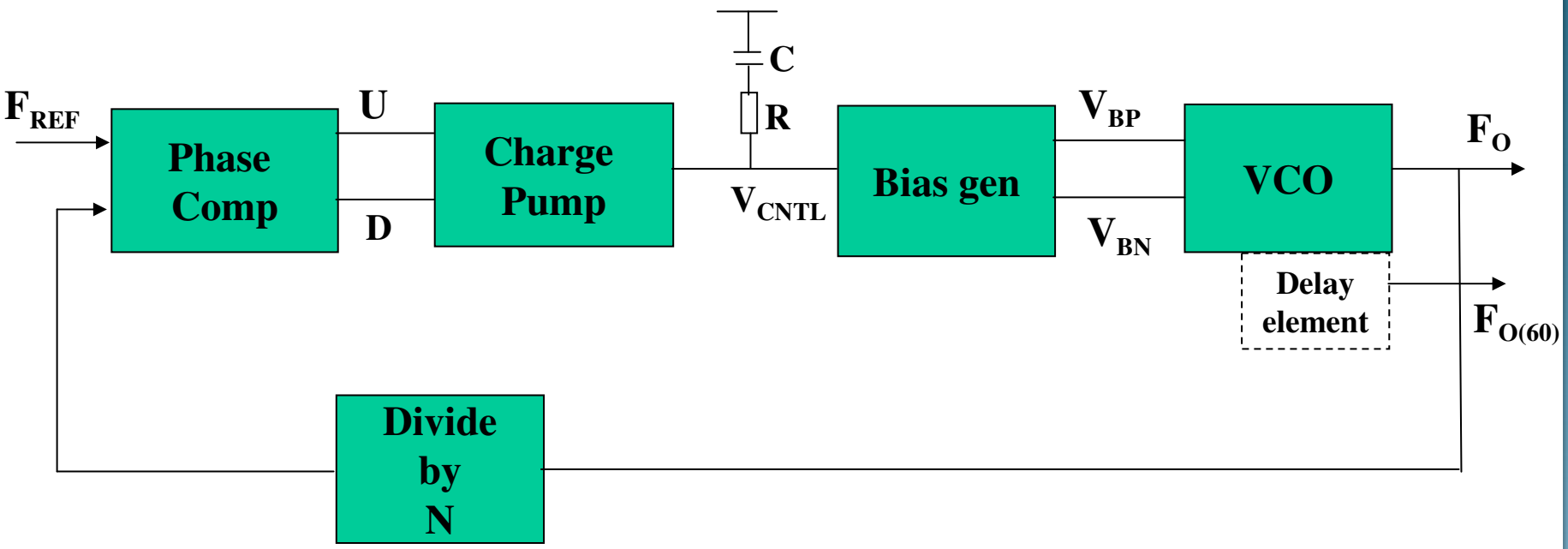
Block Diagram of PLL [1]



[1. from J.Maneatis, 1996]

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VHDL-AMS Model of VCO

```
library IEEE;
   use IEEE.std_logic_1164.all;
   use IEEE.electrical_systems.all;
   use IEEE.math_real.all;
entity vco is
   port (
      signal     initp        : IN  std_logic;
      signal     initn        : IN  std_logic;
      signal     enp          : IN  std_logic;
      signal     enn          : IN  std_logic;
      signal     ck54m24        : OUT std_logic;
      signal     ck54m24_early : OUT std_logic;
      terminal   VP           : ELECTRICAL;
      terminal   VN           : ELECTRICAL;
      terminal   VBP          : ELECTRICAL
   );
end vco;
architecture adms_vhdlams of vco is
quantity  freq      : real      := 270.0e6;
quantity  phase     : real      :=  0.0;
quantity  phase60   : real      :=  MATH_2_PI / 6.0;
quantity  vout      : real      :=  0.0;
quantity  vout60    : real      :=  0.0;
quantity  vpow across ipow_static,
                ipow_dynamic through VP to VN;
quantity  vin  across iin          through VP to VBP;
signal      static_current     : real      :=  0.0;
begin
   static_current  <=  0.2e-3 when enp = '1'else 0.0;
   ipow_static     ==  static_current'ramp(10.0e-9);
ipow_dynamic == 5.0e-12 * freq; -- 5uA/MHz
   iin             ==  0.0;
   if vin'above(0.66)
use freq == (vin - 0.66) * 100.0e6; -- 100MHz/V
      else freq    ==  0.0;
   end use;
   if domain = quiescent_domain
      use  phase       ==  0.0;
         phase60     ==  MATH_2_PI / 6.0;
      else phase'dot   ==  MATH_2_PI * freq;
         phase60'dot ==  MATH_2_PI * freq;
   end use;
   vout    == sin(phase);
   vout60  == sin(phase60);
conv2dig : process (enp, initp, vout'above(0.0),
vout60'above(0.0))
      begin
         if enp = '1' and initp = '1'
            then if vout'above(0.0)
                  then ck54m24_early   <=  '1';
                  else ck54m24_early   <=  '0';
               end if;
               if vout60'above(0.0)
                  then ck54m24         <=  '1';
                  else ck54m24         <=  '0';
               end if;
            end if;
      end process conv2dig;
end adms_vhdlams;
```

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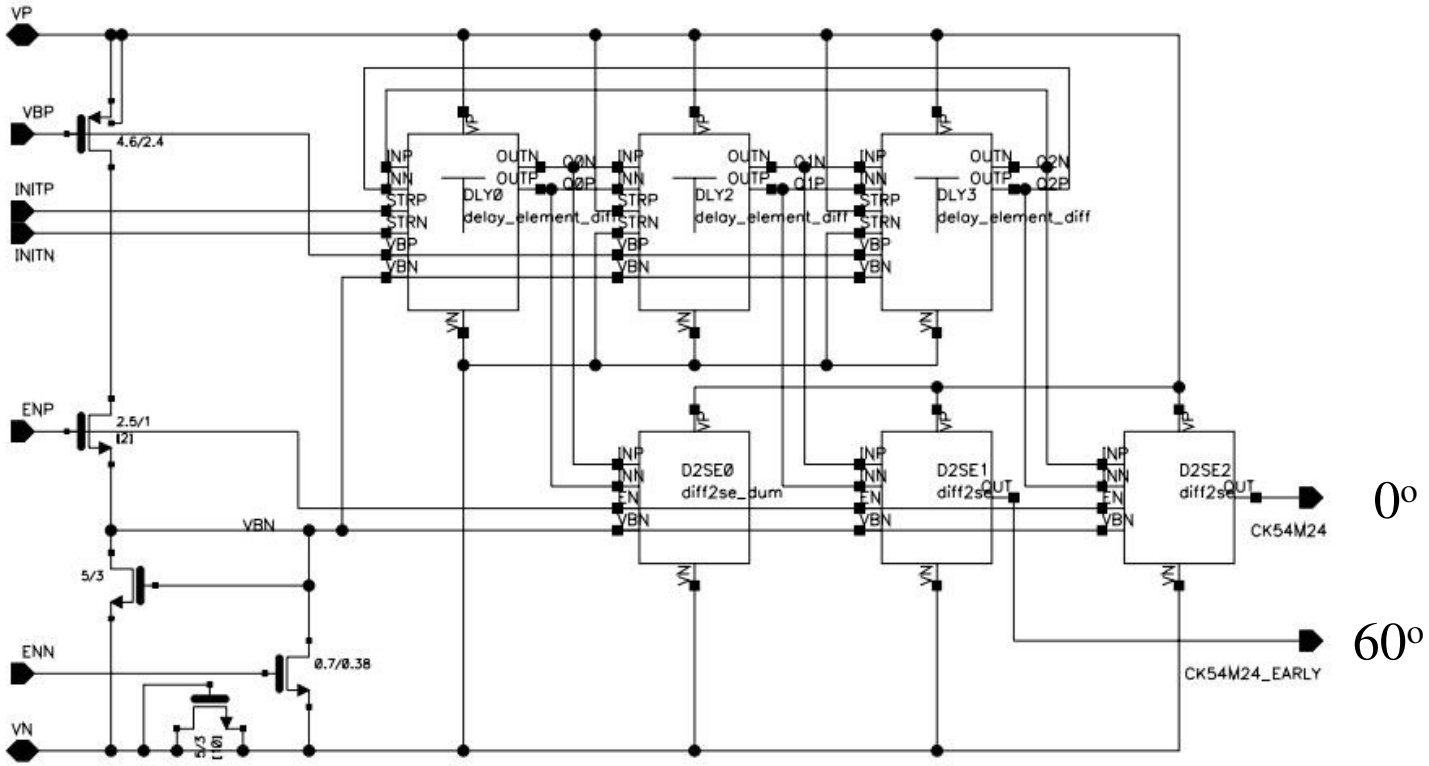
Transistor level model of VCO



Schematic of VCO

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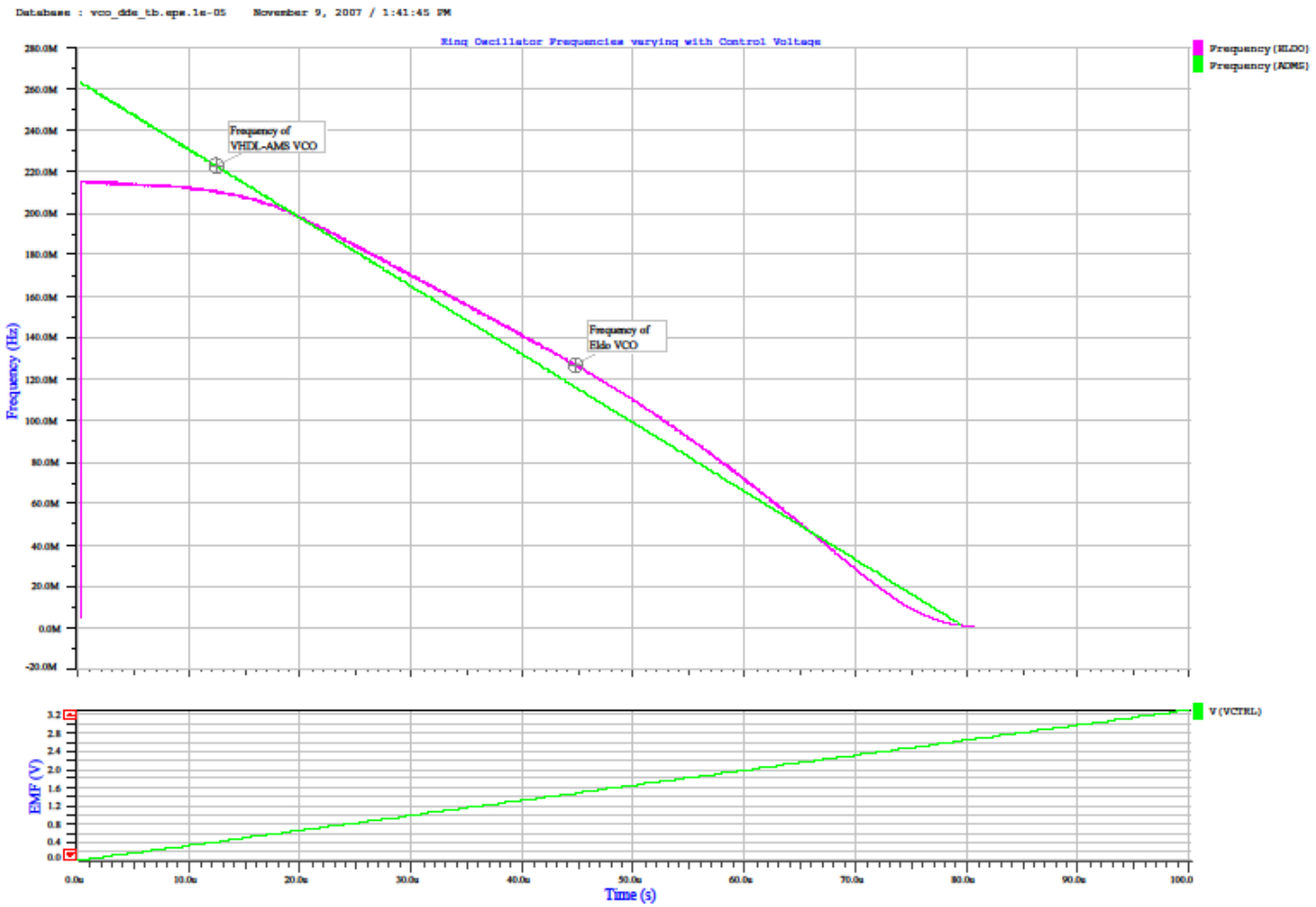
Simulation of VCO Frequencies (VHDL-AMS vs ELDO)



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VCO simulation times

Comparing simulation times is never simple as both spice-like simulators and MS simulators have numerous control options.

Need to include accuracy settings:-

Global Accuracy, EPS	CPU simulation times (min, sec)	
	ELDO	VHDL-AMS
1.00E-05	39m 14s	20s
1.00E-04	36m 29s	20s
1.00E-03	29m 7s	20s
1.00E-02	27m 45s	20s

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VHDL-AMS Model of Charge Pump

```
LIBRARY IEEE;
   USE ieee.std_logic_1164.ALL;
   USE IEEE.ELECTRICAL_SYSTEMS.ALL;

entity pll_chpump is
   port (
      signal     dnp       : in  std_logic;
      signal     dnn       : in  std_logic;
      signal     upp       : in  std_logic;
      signal     upn       : in  std_logic;
      terminal   VP        : ELECTRICAL;
      terminal   VN        : ELECTRICAL;
      terminal   OUT_CAP   : ELECTRICAL;
      terminal   VBN       : ELECTRICAL
   );
end pll_chpump;

architecture adms_vhdlams of pll_chpump is

quantity vout_up across iout_up through OUT_CAP to VN;
quantity vout_dn across iout_dn through VP to OUT_CAP;
quantity vref    across iref    through VBN to VN;

constant    res1    : real   := 80.0e3;

begin

   iref    ==  0.0;

   IF upp /= `1'
      USE  iout_up == 0.0;
   ELSIF vout_up'ABOVE(0.5)
      USE  iout_up == 1.0          * vref / res1;
      ELSE iout_up == 2.0 * vout_up * vref / res1;
   END USE;

   IF dnp /= `1'
      USE  iout_dn == 0.0;
   ELSIF vout_dn'ABOVE(0.5)
      USE  iout_dn == 1.0          * vref / res1;
      ELSE iout_dn == 2.0 * vout_dn * vref / res1;
   END USE;

end adms_vhdlams;
```

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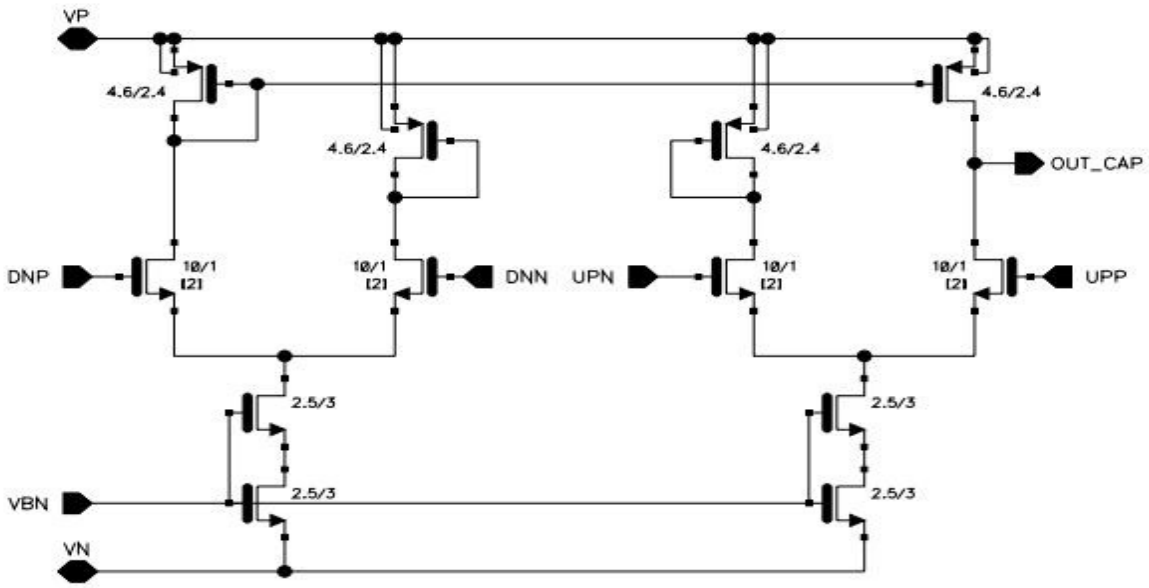
Schematic of Charge Pump



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Results

Digital VHDL RTL was verified by simulation

- the synthesised placed/routed netlist was verified

1. **by formal equivalence with the VHDL RTL**
2. **simulation using extracted SDF timings**

Mixed-signal was verified

1. **At block level using ELDO**

   - verify desired functionality

   - verify validity of VHDL-AMS models ("calibration")

2. **At Transceiver design level**

   - firstly using VHDL-AMS behavioural models of all MS blocks

   - selected blocks resimulated using ELDO views

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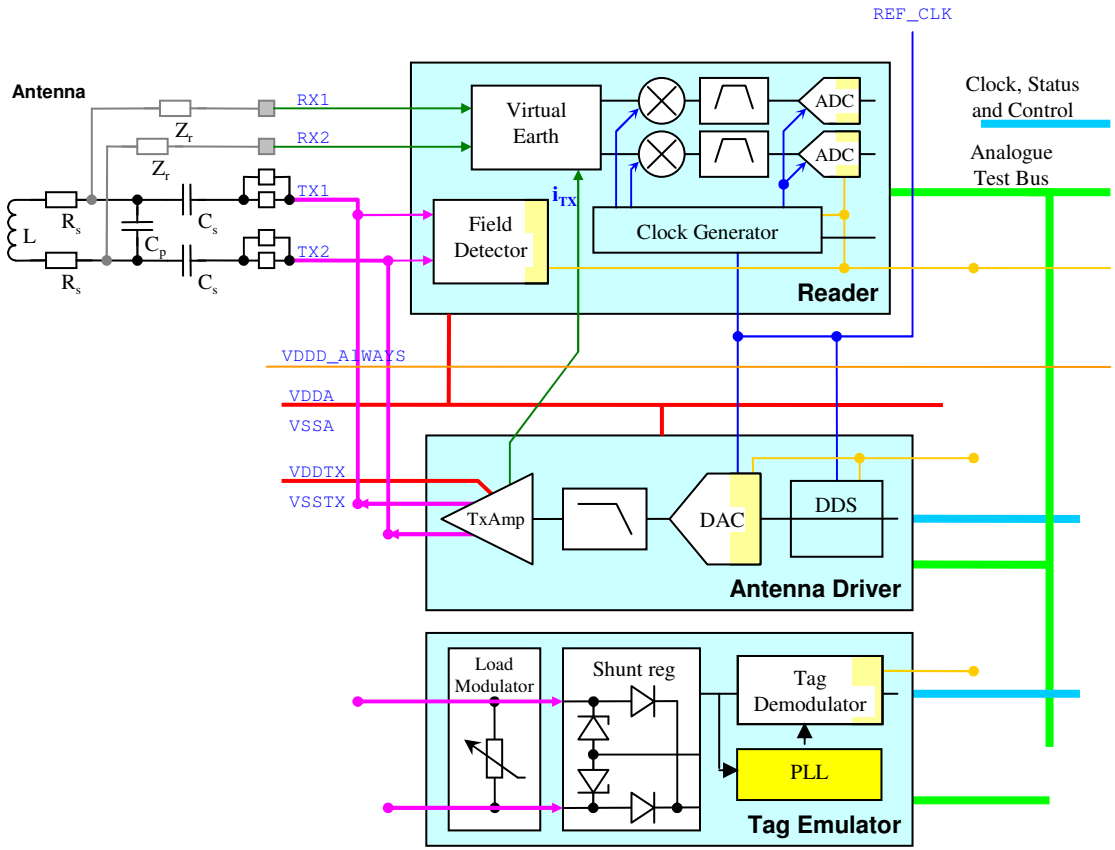
Simplified block diagram of transceiver



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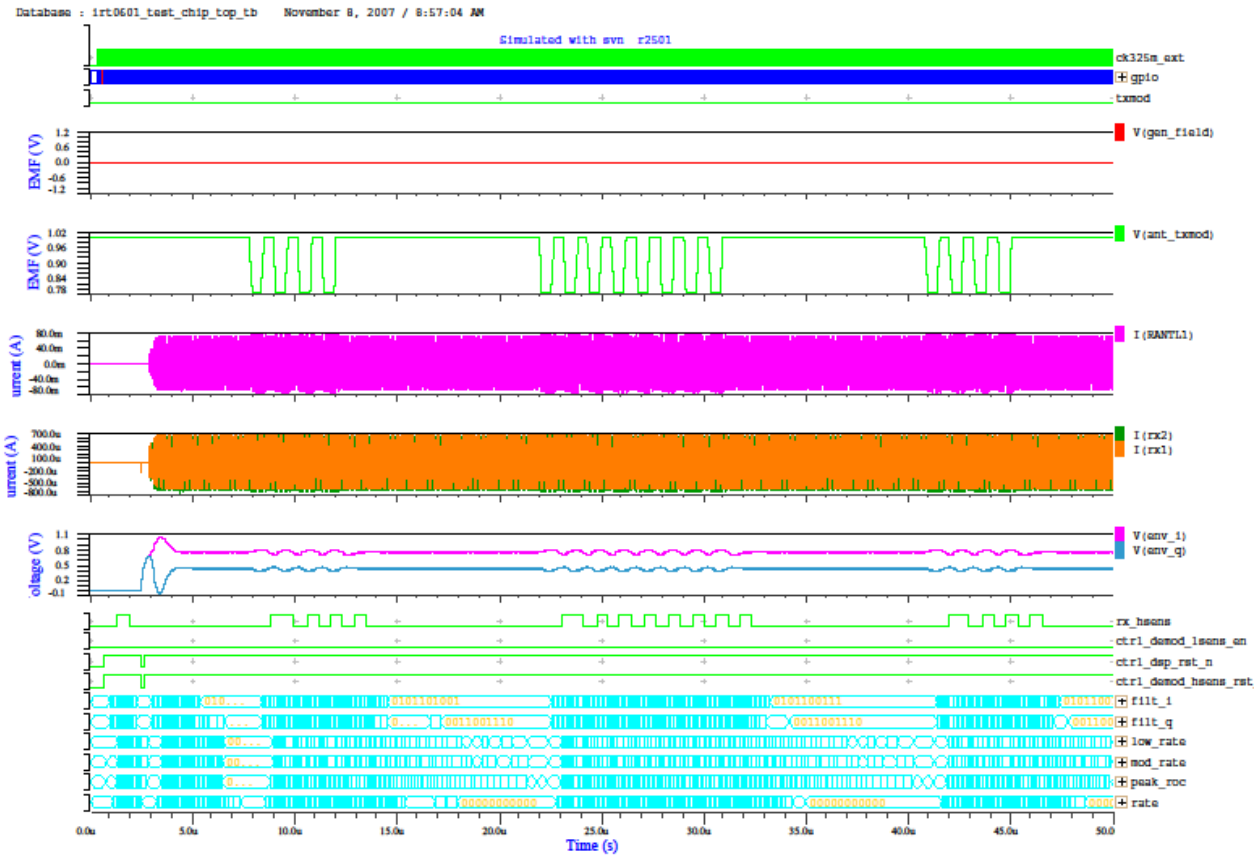
VHDL-AMS Simulation of NFC Transceiver

with all mixed-signal blocks simulated in VHDL-AMS mode:-



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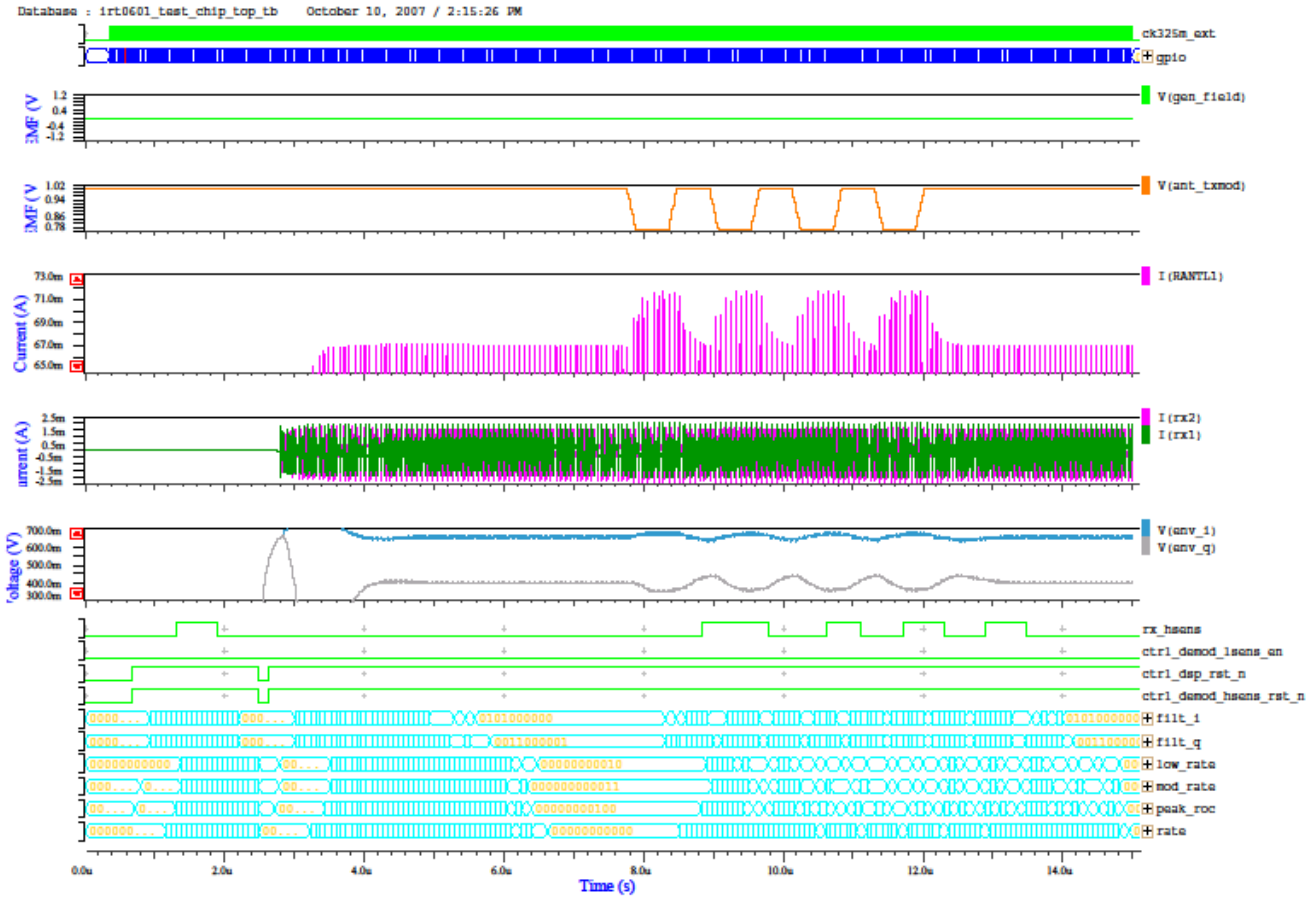
Combined ELDO and VHDL-AMS Simulation of NFC Transceiver

with antenna driver, shunt reg, power supply unit, field detect and IQ demod running in ELDO and all other blocks in VHDL-AMS mode:-



Factor of x4000 speed improvement compared with ELDO simulation!

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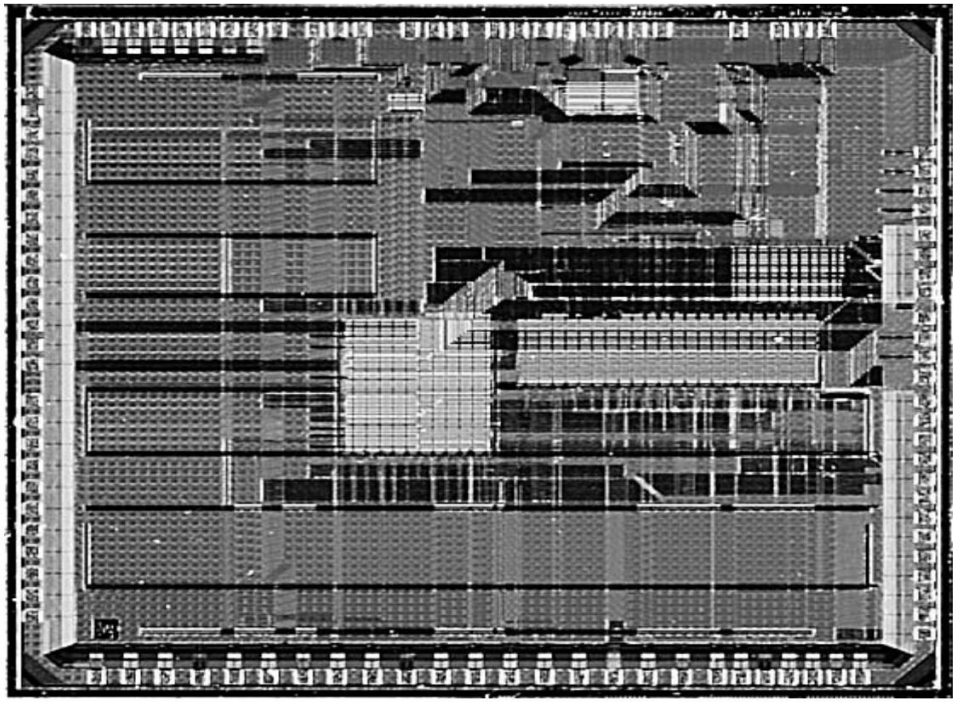
The NFC Chip

The NFC chip realised in 90nm CMOS process:-



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