Digital Control of High Efficiency Analog Switch-Mode Power Supplies

Simon Effler

Circuits and Systems Research Centre
University of Limerick
Limerick
Ireland
simon.effler@ul.ie

NMI/MIDAS, "Digitally Assisted Analogue", 22.10.2009

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Outline

1. Circuits and Systems Research Centre
2. Control of SMPS - Short History
3. Oversampled Control
   - Problem
   - System Overview
   - Bumpless Compensator Architecture
   - Verification
   - Conclusions

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Outline

1. Circuits and Systems Research Centre
2. Control of SMPS - Short History
3. Oversampled Control
   - Problem
   - System Overview
   - Bumpless Compensator Architecture
   - Verification
   - Conclusions

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Circuits and Systems Research Centre

- University of Limerick
- 2 Research areas
- 7 Research/academic staff
- 5 Ph.D. students
- Commercialisation Activities
  - Powervation
  - Chipsensors
- `www.csrc.ie`

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Mixed Signal IC Group (MSIC)

Members

- Dr. Ciaran MacNamee
- Dr. Tony Scanlan
- Brendan Mullane
- Vincent O'Brien

New Projects

- A Scalable Efficient Digital to Analog Converter Architecture, SEDACA (Brendan Mullane)
- High Efficiency Embedded A/D Converter in Scaling Nanometer Technologies, Hi-Cosant (Tony Scanlan)

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Intelligent Power Management and Advanced Control

Members

- Dr. Mark Halton
- James Mooney
- Martin Scharrer
- Simon Effler

Projects

- Digital Controller for High-efficiency DC-DC Conversion, HieCon (Mark Halton)
- Digital Power Incorporating Time/Event Driven Control, EdCon (Mark Halton)

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Outline

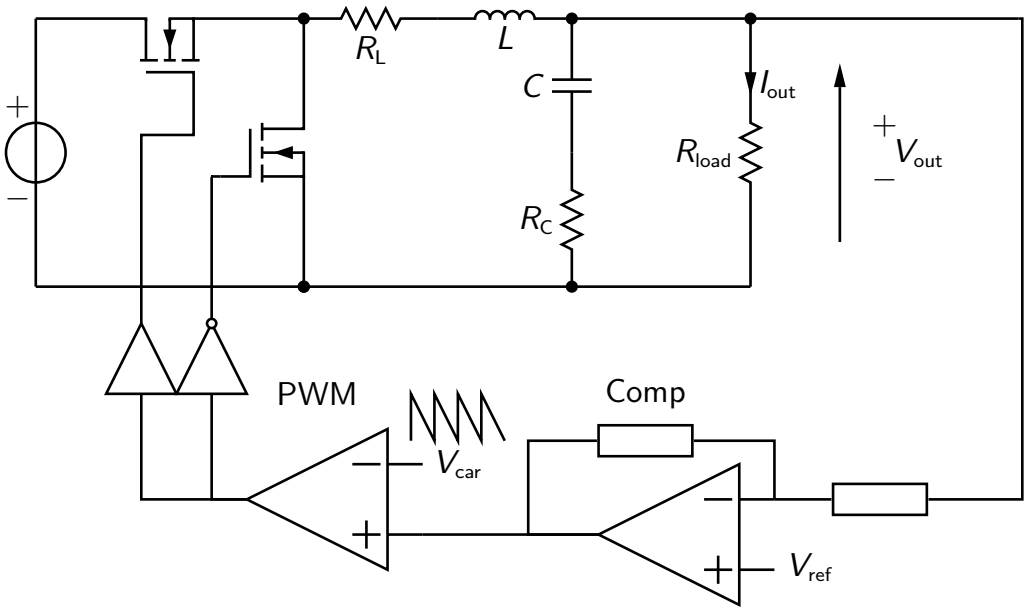
1. Circuits and Systems Research Centre
2. Control of SMPS - Short History
3. Oversampled Control
   - Problem
   - System Overview
   - Bumpless Compensator Architecture
   - Verification
   - Conclusions

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

Analogue Control of SMPS

- Analogue control loop
- + Inexpensive process
- + Relatively simple control
- − Large PCB footprint
- − No system integration

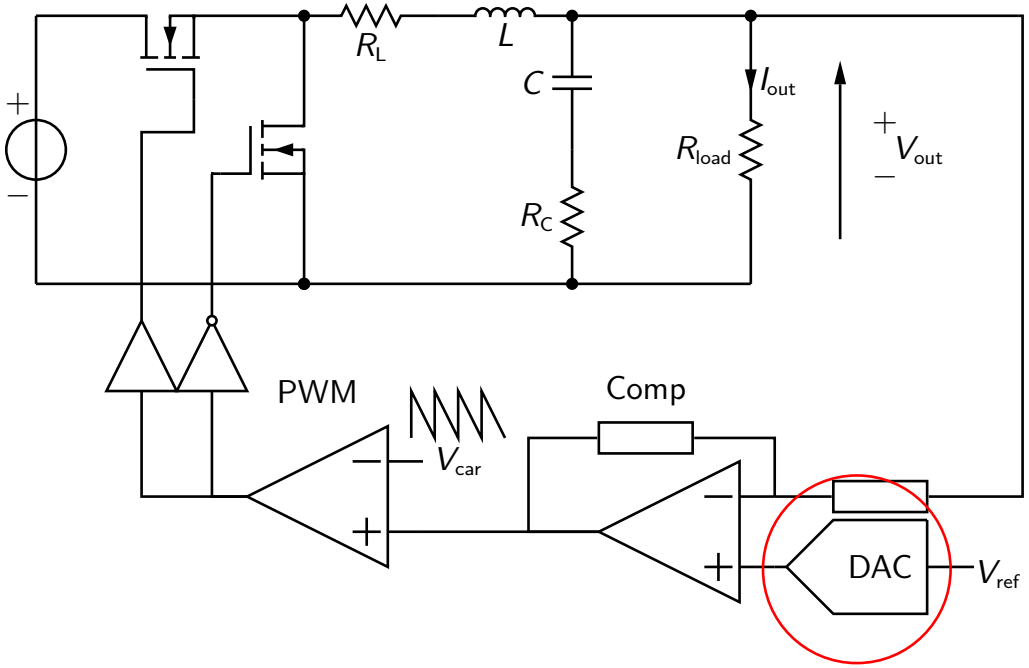


"Digital Wrappers"

- Analogue control loop combined with a digital interface

+ Fast, well-understood control loop
+ System integration via digital communication
  - Monitoring
  - Limited configuration

− Demands on analogue components
− Limited process scalability

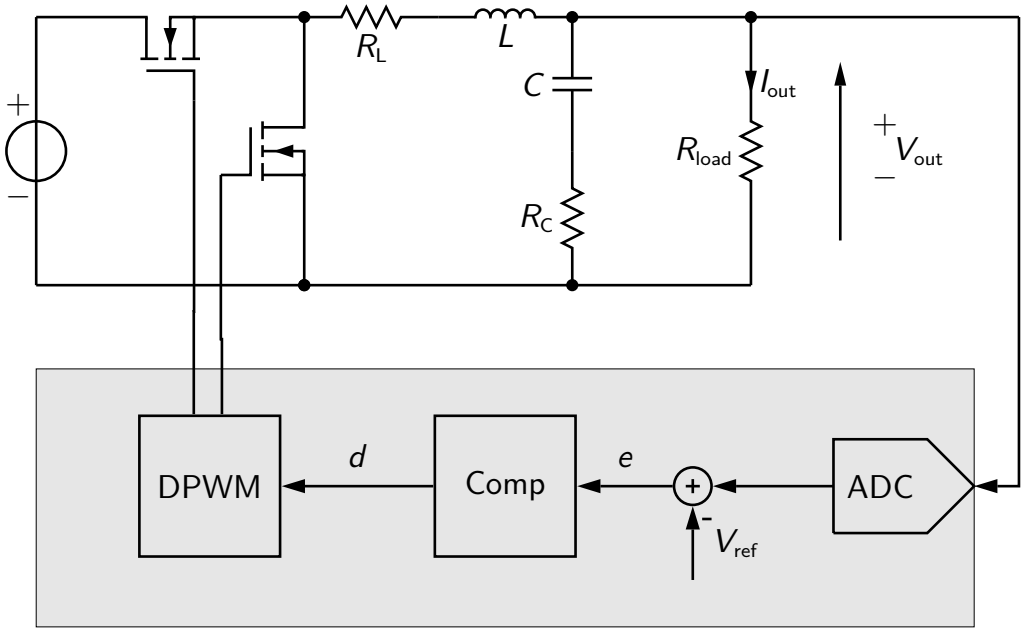


OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc circuits and systems research centre

Digital – Mixed Signal SOC

- Digital control loop
- Analogue: ADCs, (DPWMs)
- \+ System level integration
  - Configuration
  - Monitoring
- \+ Small PCB footprint
- \+ Scalable with process
- – Power demand with higher switching frequencies



Simon Effler, Zdravko Lukic, and Aleksandar Prodic. "Oversampled Digital Power Controller with Bumpless Transition Between Sampling Frequencies". In: *Proceedings of IEEE Energy Conversion Congress and Exposition 2009*, 2009

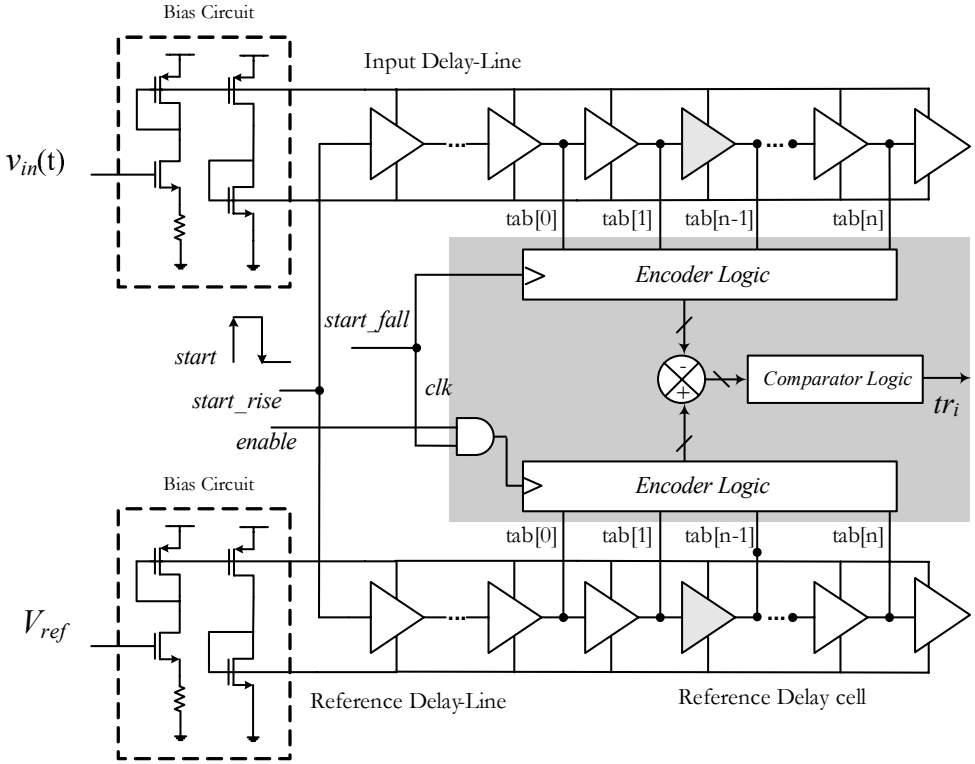
OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc circuits and systems research centre

Digital – ”Fully Digital System“

- Digital control loop
- "Unconventional, digital ADCs"

+ Low-power
+ Scalable process
+ Load integration



A. Parayandeh, A. Stupar, and A. Prodic. “Programmable Digital Controller for Multi-Output DC-DC Converters with a Time-Shared Inductor”. In: *Proc. 37th IEEE Power Electronics Specialists Conference PESC ’06*. 2006, pp. 1–6.

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc circuits and systems research centre

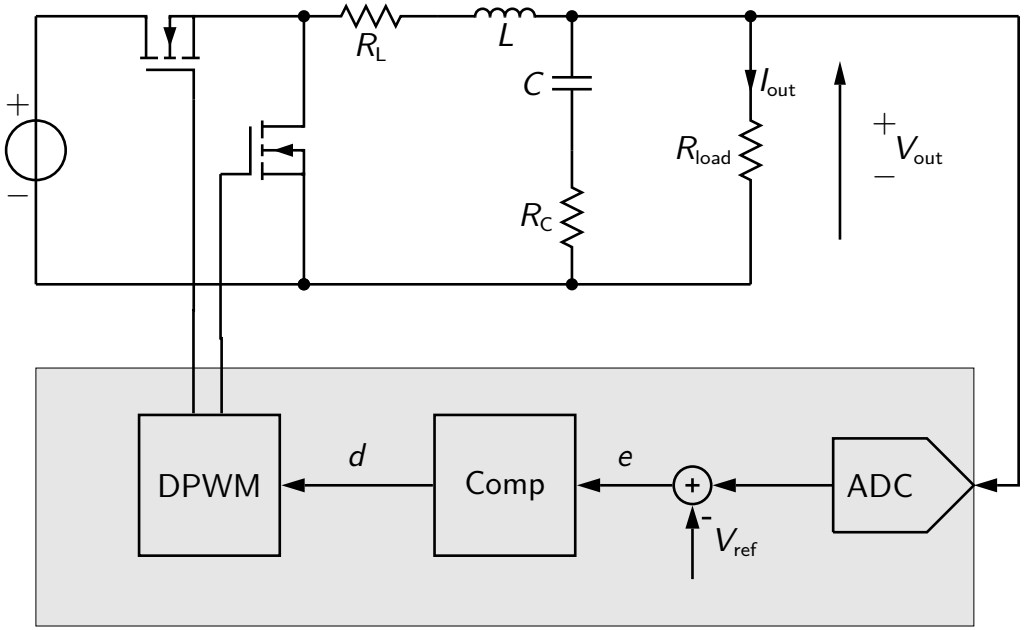
Outline

1. Circuits and Systems Research Centre
2. Control of SMPS - Short History
3. Oversampled Control
   - Problem
   - System Overview
   - Bumpless Compensator Architecture
   - Verification
   - Conclusions

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

System Block Diagram



Oversampling

Sampling with a multiple of the switching frequency

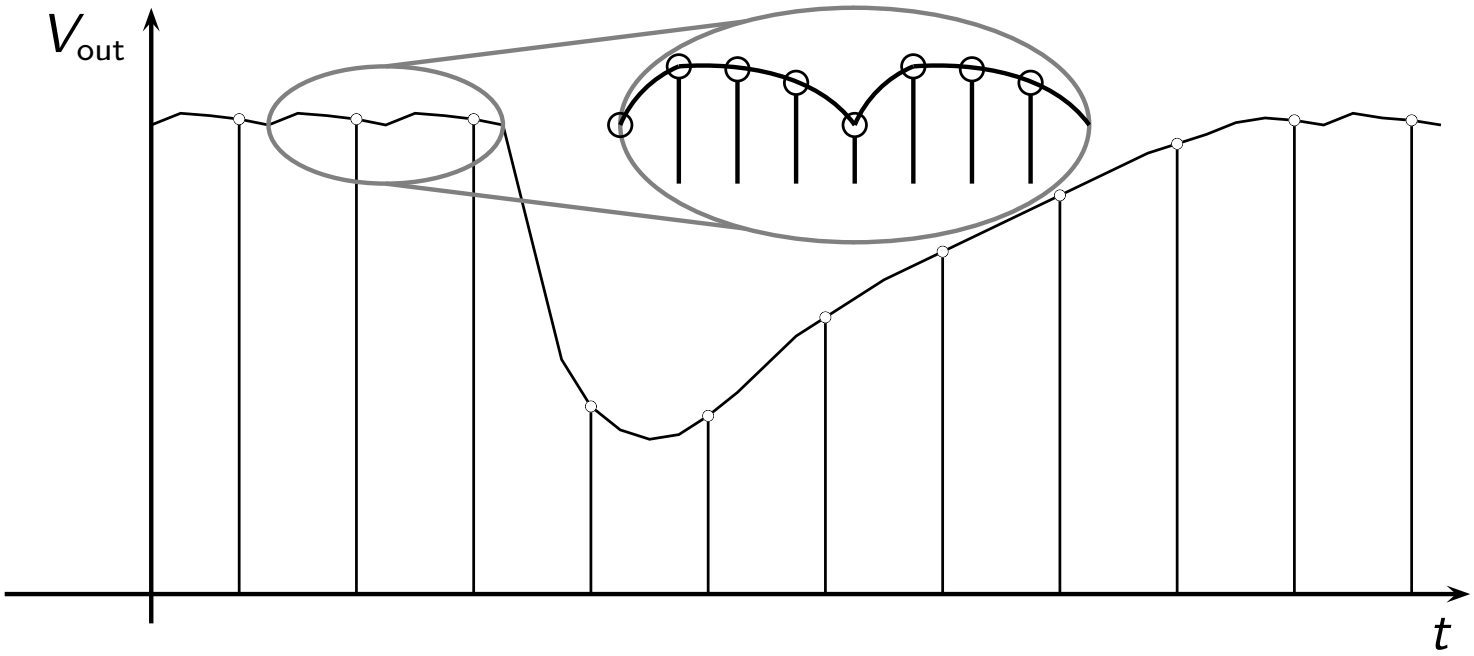
Advantages

- "Faster" compensators possible
- Better utilization of ADCs

Challenges

- Noise propagation through loop
- No natural sampling noise suppression

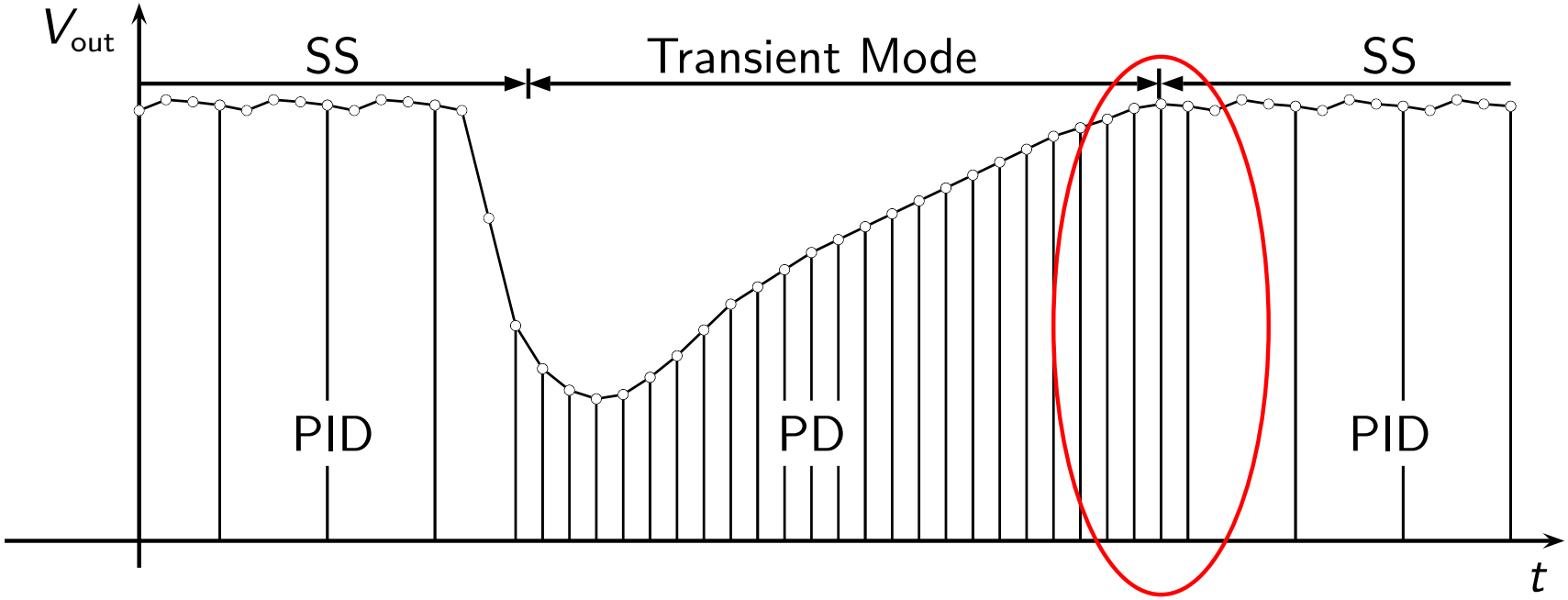
Natural Sampling Noise Suppression



System Overview

- Variable "sampling" frequency
- Steady-state: "Sampling" at switching frequency
- Transients: Oversampling
- Bumpless transition between compensators
- ⇒ No additional filters required.

Modes of Operations



⇒ Need for a bumpless transition

Bumpless transition: control theory

- Change between two compensators without causing an additional transient
- Used in PLCs
- Mainly for continuous-time compensators
- No change of sampling frequency
- Relatively straight-forward for PID compensators
- $\Rightarrow$ Keep compensator output constant during transition

Bumpless transition in detail

PD

$$d_{T,N} = d_{bias,N} + K_{P,T}\ e_N + K_{D,T}\ (e_N - e_{N\text{-}1})$$

PID

$$\begin{aligned} d_{SS,N} &= d_{i,N} + K_{P,SS}\ e_N + K_{D,SS}\ (e_N - e_{N\text{-}1}) \\ d_{i,N} &= d_{i,N\text{-}1} + K_{I,SS}\ e_N \end{aligned}$$

Transition

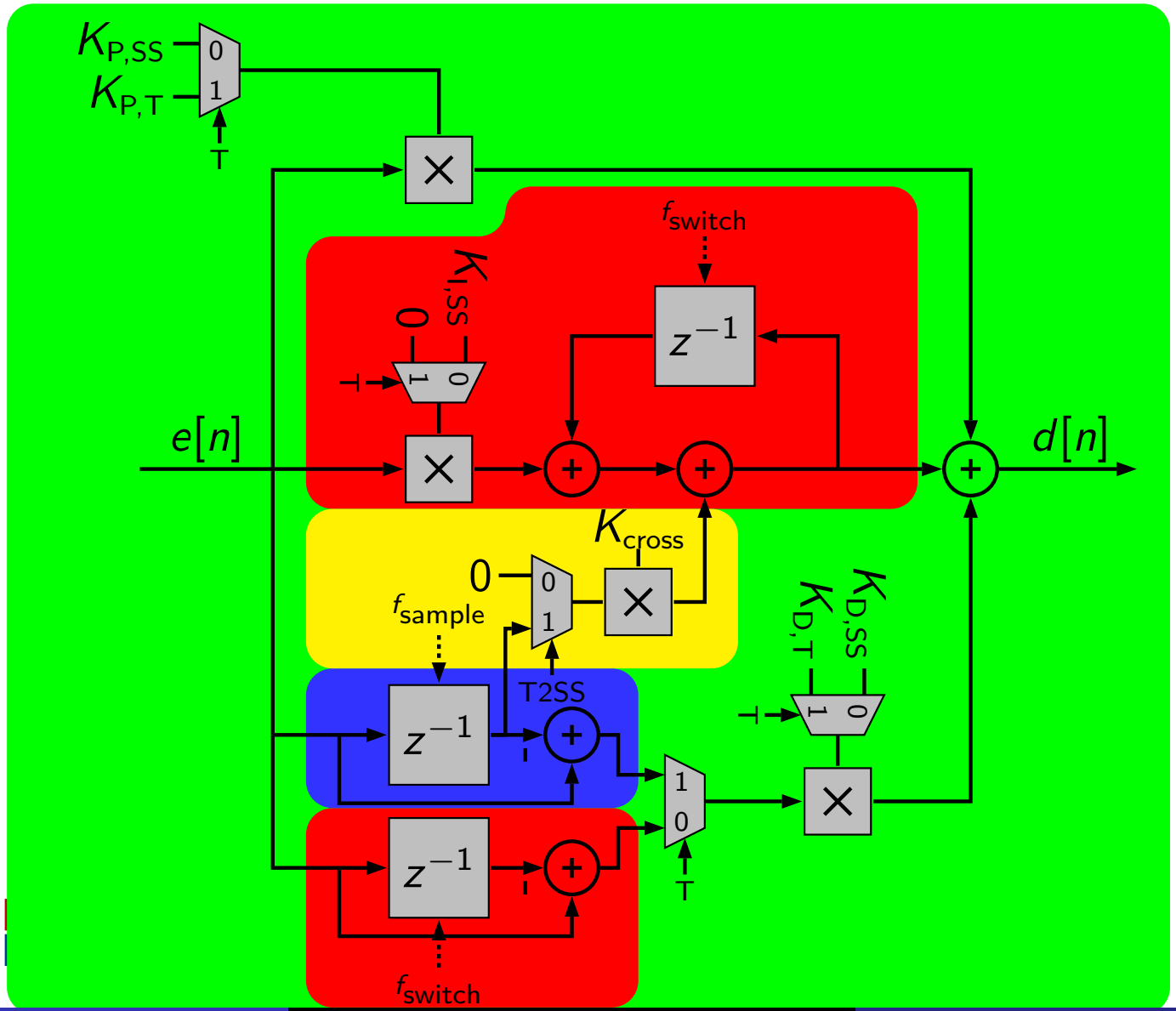
$$d^* = (K_{P,T} - K_{P,SS})\ e_{N\text{-}1}$$

- Use integral part of PID to compensate for perturbation during transition

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

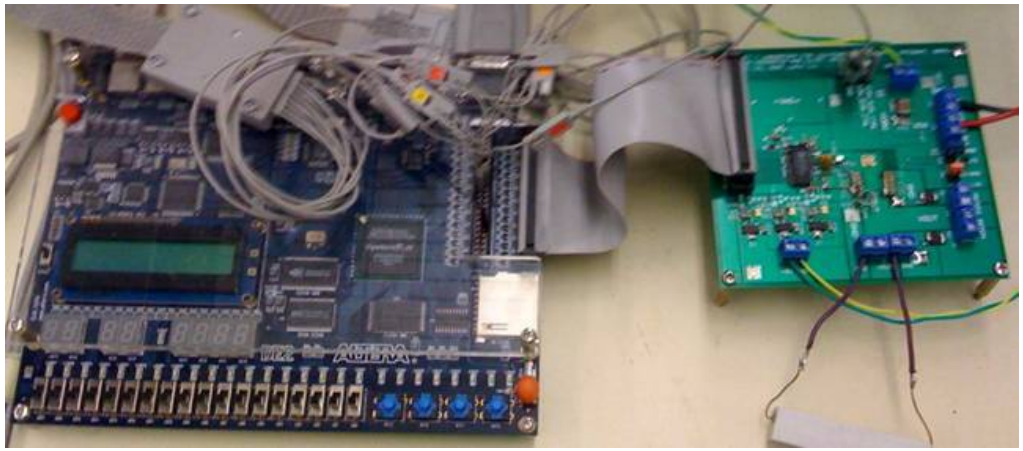
csrc circuits and systems research centre

Implementation of bumpless compensator

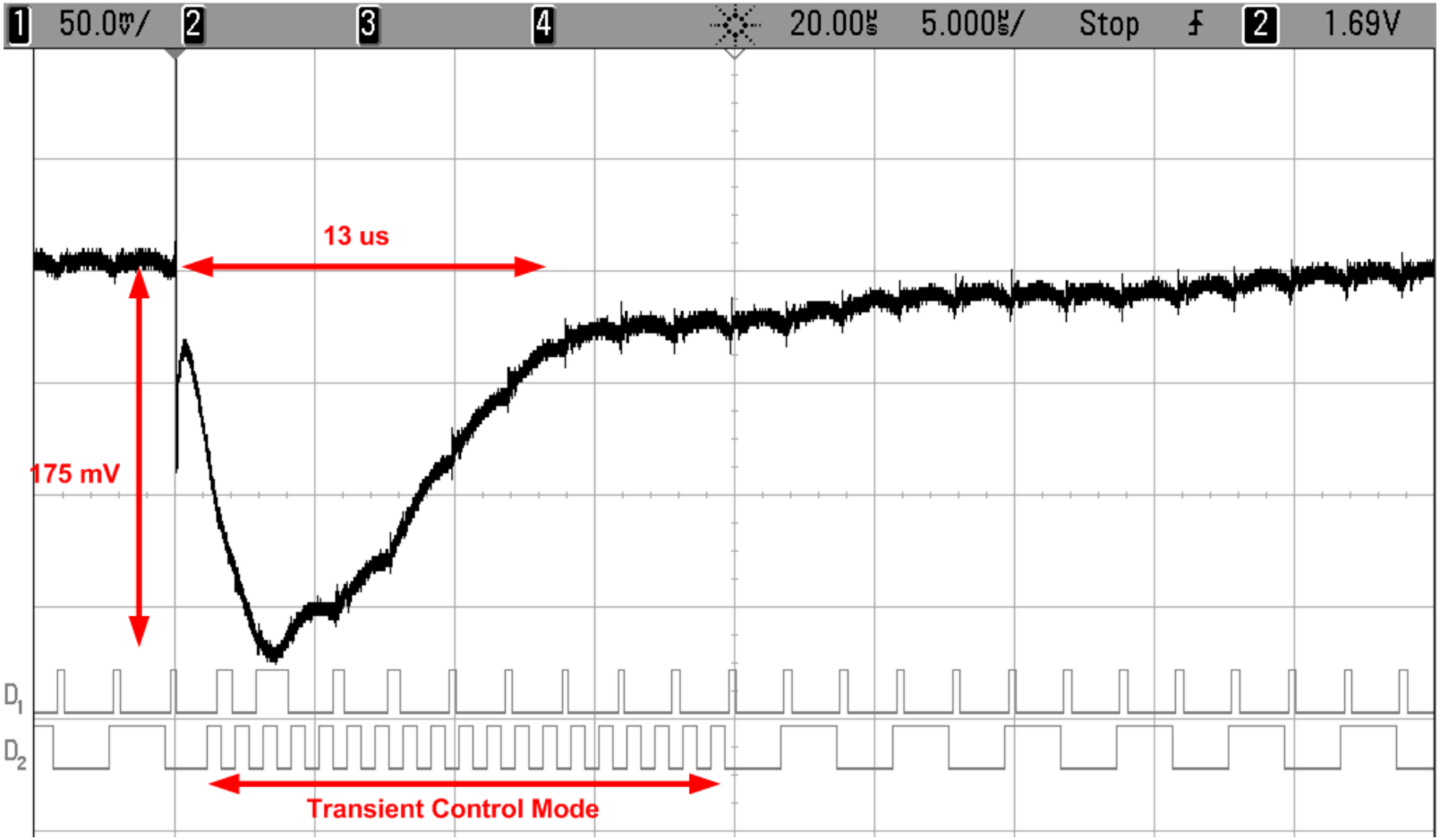


Prototype

- Buck converter
- Oversampling: 4
- FPGA prototype
- f_s=500 kHz
- V_{In}=12 V
- V_{out}=1.5 V
- L=950 nH
- C=250 µF
- 15 A load step



Experimental Results



Conclusions I

Oversampled compensator with variable sampling frequency

- Steady-state: Switching frequency
- Transients: Sampling frequency
- Bumpless transition between operation modes

Advantages - Naturally sampled compensators

- Improved transient performance
- Reduction of transient by about 50%
- Virtually for free

Conclusions II

Advantages - Oversampled compensators

- Reduction of filter requirements
- Reduction of computational requirements
- Two independent compensator designs

Future work

- Transient detection independent of ADC
- Free ADC resources for other signals
- Special ADCs with variable sampling speed

Thank You for Your Attention!

Questions?

Contact:
simon.effler@ul.ie

Detailed Information:
`www.csrc.ie`

Simon Effler, Zdravko Lukic, and Aleksandar Prodic. "Oversampled Digital Power Controller with Bumpless Transition Between Sampling Frequencies". In: *Proceedings of IEEE Energy Conversion Congress and Exposition 2009*. 2009

OLLSCOIL LUIMNIGH
UNIVERSITY OF LIMERICK

csrc
circuits and systems research centre

[1] Simon Effler, Zdravko Lukic, and Aleksandar Prodic. "Oversampled Digital Power Controller with Bumpless Transition Between Sampling Frequencies". In: *Proceedings of IEEE Energy Conversion Congress and Exposition 2009*. 2009.

[2] A. Parayandeh, A. Stupar, and A. Prodic. "Programmable Digital Controller for Multi-Output DC-DC Converters with a Time-Shared Inductor". In: *Proc. 37th IEEE Power Electronics Specialists Conference PESC '06*. 2006, pp. 1–6.

[3] `www.csrc.ie`.