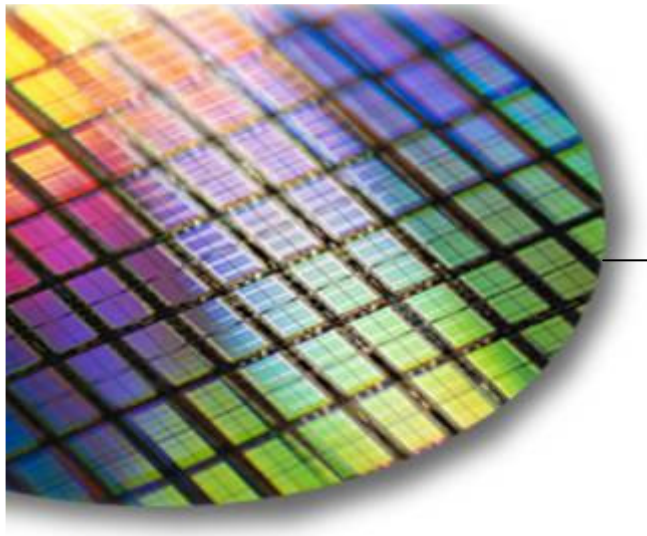

The World Leader in High Performance Signal Processing Solutions

Low Power Wireless Transceiver Architectures with Digitally Assisted RF

Philip Quinlan, Hyman Shanan
Analog Devices, Cork, Ireland

Oct 22 2009

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ANALOG DEVICES

Talk Outline

- Background
- Wireless Transceiver Technology in CMOS
- Use of Digital Calibration to improve Receiver IR Performance
- Use of Digital Pre-emphasis to extend Transmitter Bandwidth

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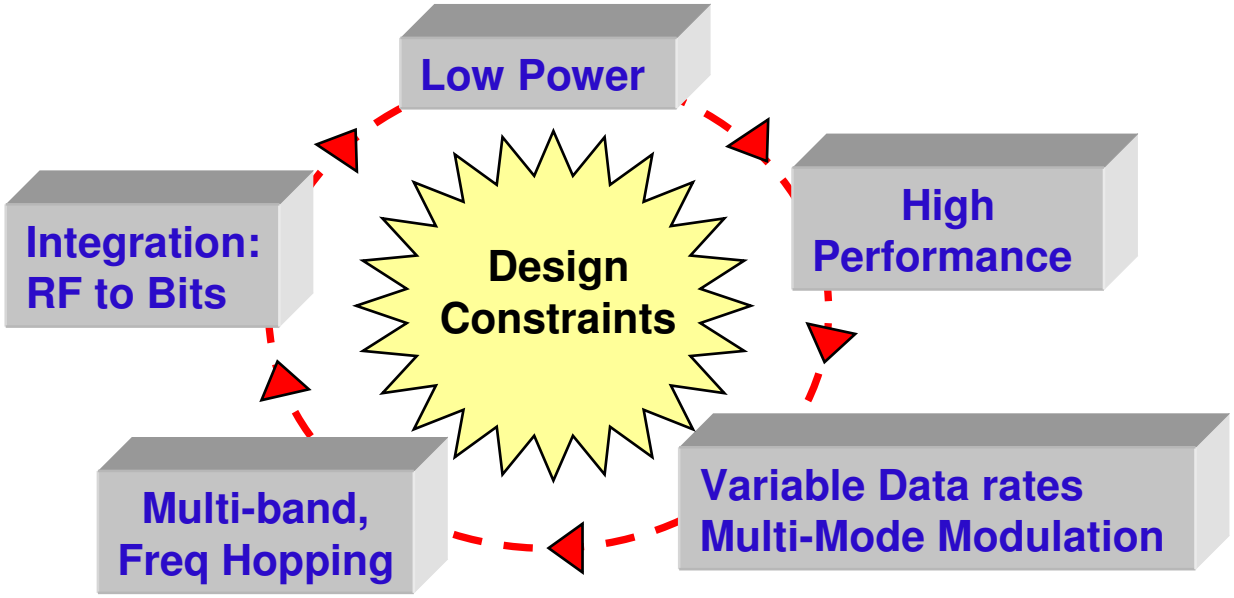
Low Power Wireless Transceiver – Design Challenges

Applications

- ❑ Building/Home Automation
- ❑ Wireless Metering (Water, Gas, power)
- ❑ Healthcare
- ❑ Industrial Process Control
- ❑ Security



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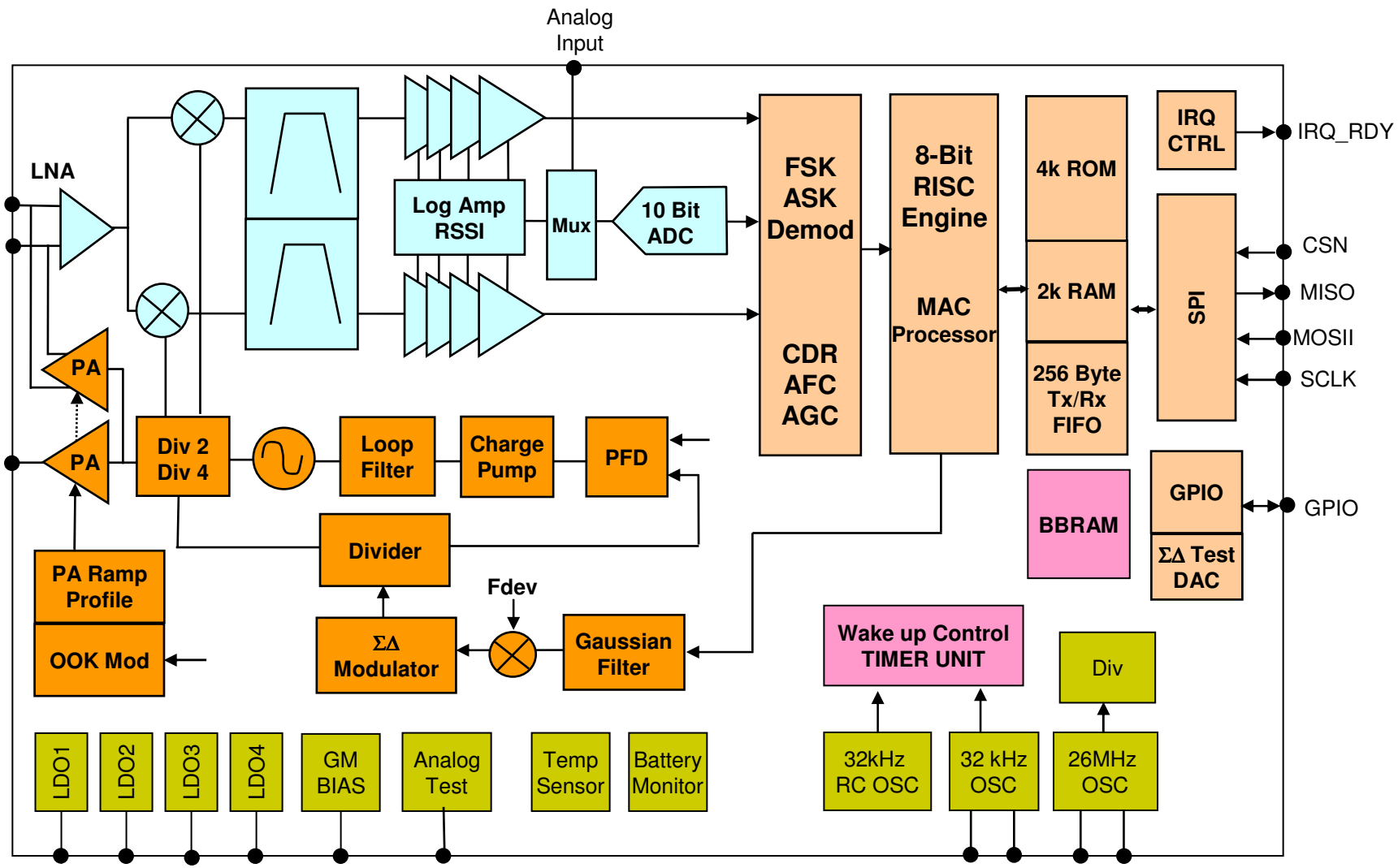
0.18um CMOS: 433/868/915 MHz Wireless Transceiver



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Product Highlights

- 0.18um CMOS Technology, 32 Pin LFCSP
- Single Chip UHF Transceiver with on-chip MAC Support
- RF Bands: 433MHz, 868MHz, 915MHz
- Modulation: FSK/GFSK/GMSK/OOK with Freq Hopping
- G/FSK Data Rates 1Kbps - 300Kbps
- Rx Idd: 13.5mA typ
- Tx Idd: 22mA @ +10dBm
- Single Ended and Differential PA
- Integrated low power RISC processor
- Enhanced Image Rejection Performance

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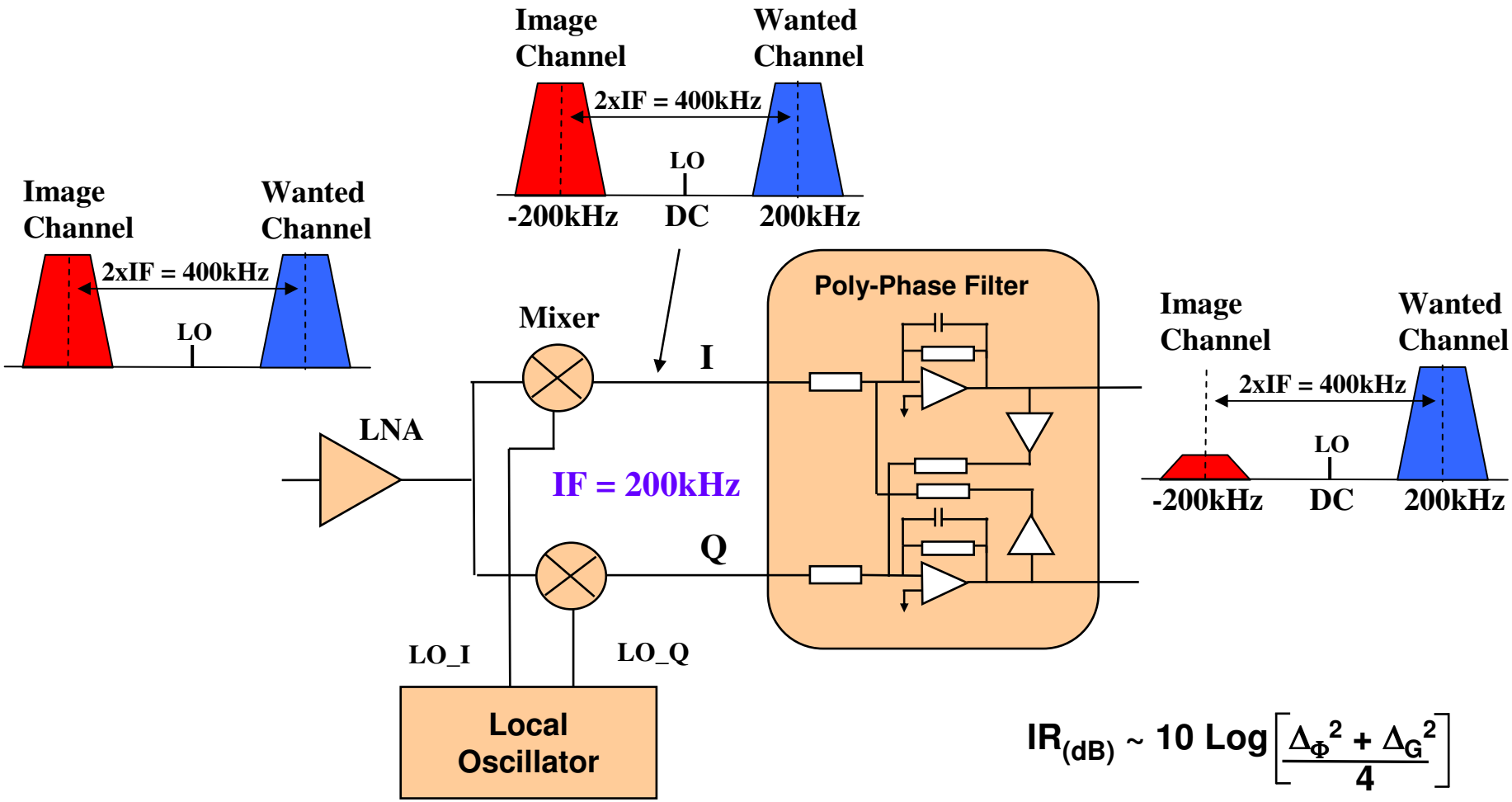
Image Rejection – The Problem in Low IF Rx



$$IR_{(dB)} \sim 10 \text{ Log}\left[\frac{\Delta_\Phi^2 + \Delta_G^2}{4}\right]$$

$$IR_{(dB)} \sim 25\text{-}30dB$$

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Important Considerations

- Use a Digital Calibration engine ?
- Fully Autonomous Calibration – no external HW support ?
- Off-line or In-line Cal ?
- How to generate the RF signal source for IR Cal ?
- Must calibrate over multiple RF bands: 433/868/915MHz
- Minimise Power, Cost, Area

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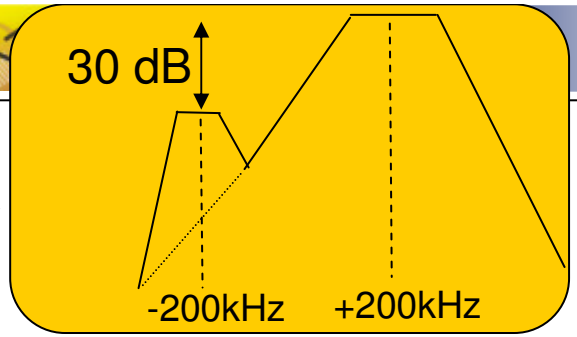
IR Calibration ....

$$IR_{(dB)} \sim 10 \text{ Log}\left[\frac{\Delta_\Phi^2 + \Delta_G^2}{4}\right]$$



LNA

Mixer

Gain/Phase Correction

5'th Poly-phase IF Filter

Power Measurement

Limiter

Log Amp RSSI

7-Bit ADC

Mux

En

905.0MHz

RF Source

Gain/Phase Adjust

RISC Processor

2-D Gain/Phase Update Algorithm

I

Q

905.2MHz

Fractional-N Synthesizer

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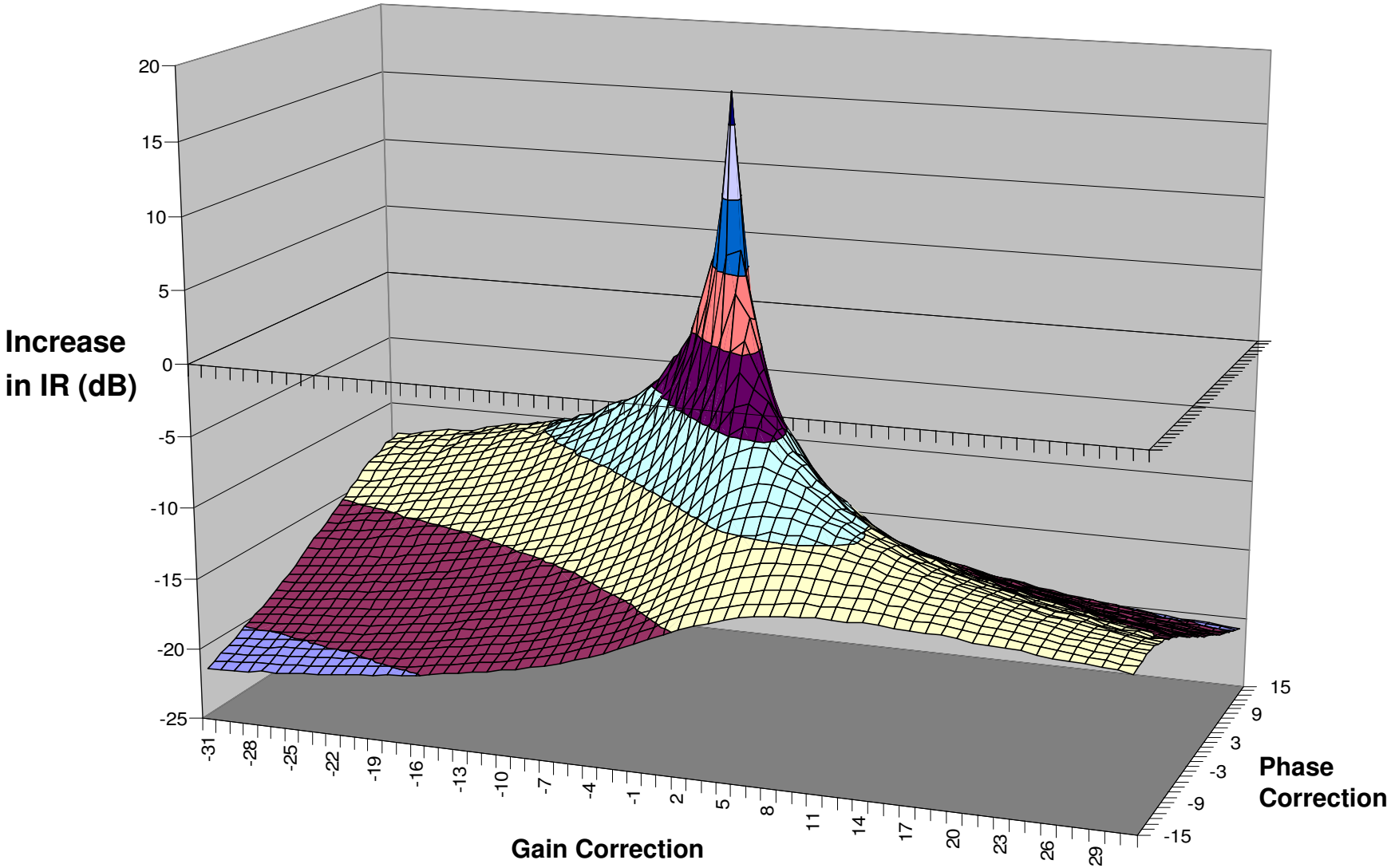
Image Rejection Vs Quadrature Gain/Phase Correction



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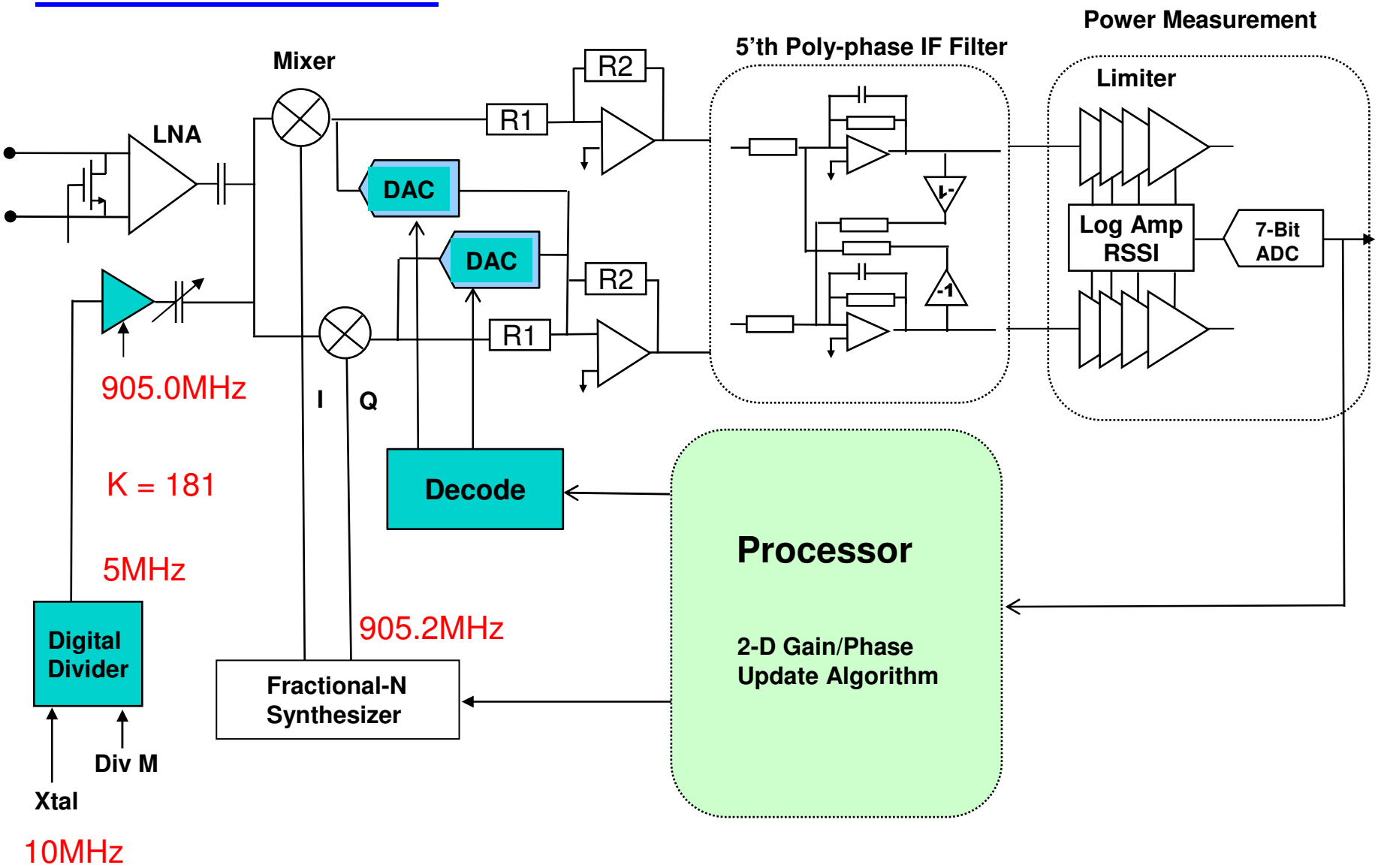
IR Calibration Details



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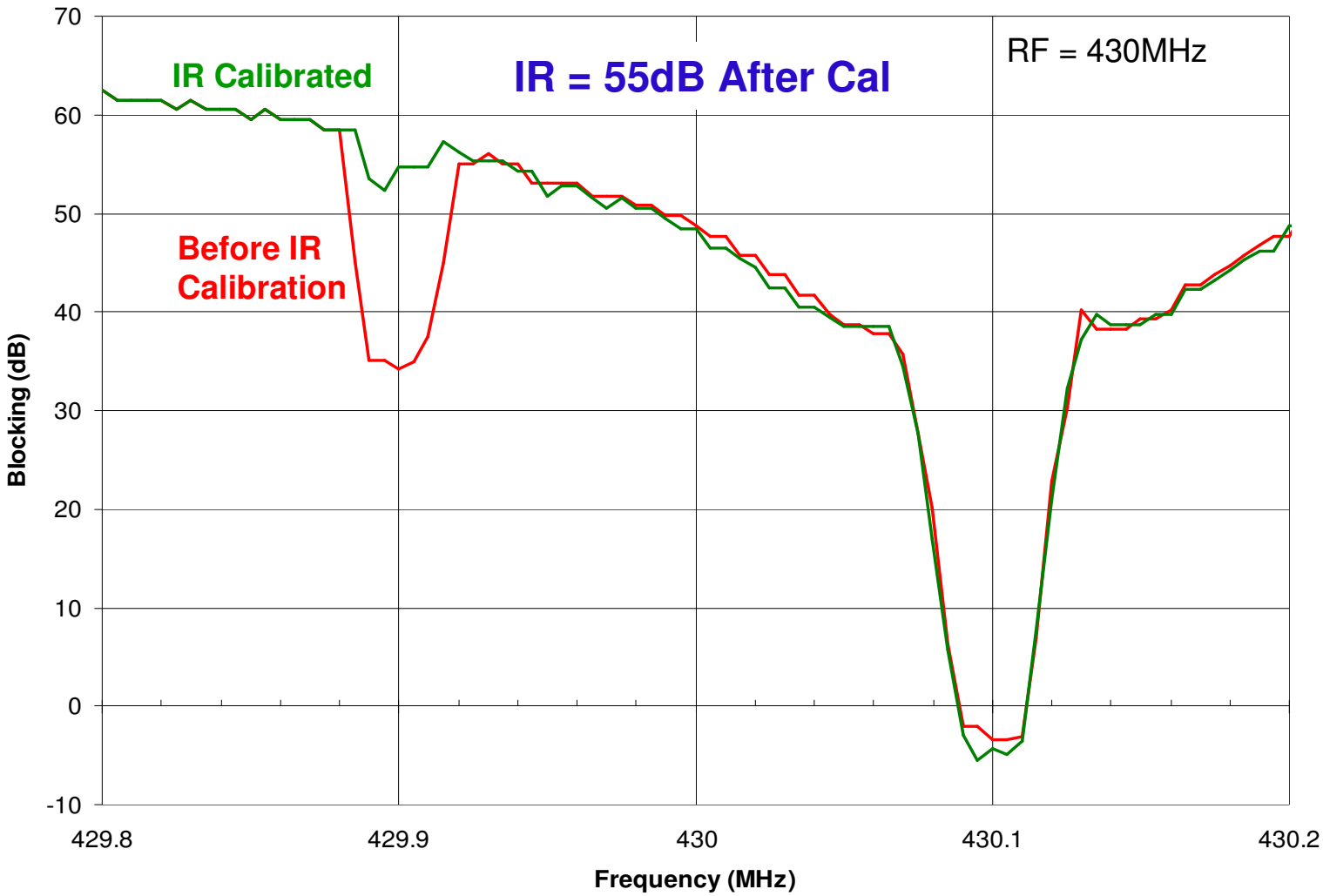
Performance – Pre and Post IR Cal



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- Background
- Overview of Wireless Transceiver Technology in CMOS
- Use of Digital Calibration to improve Receiver IR Performance
- Use of Digital Pre-emphasis to extend Transmitter Bandwidth

Hyman Shanan et al, ISSCC Feb 2009

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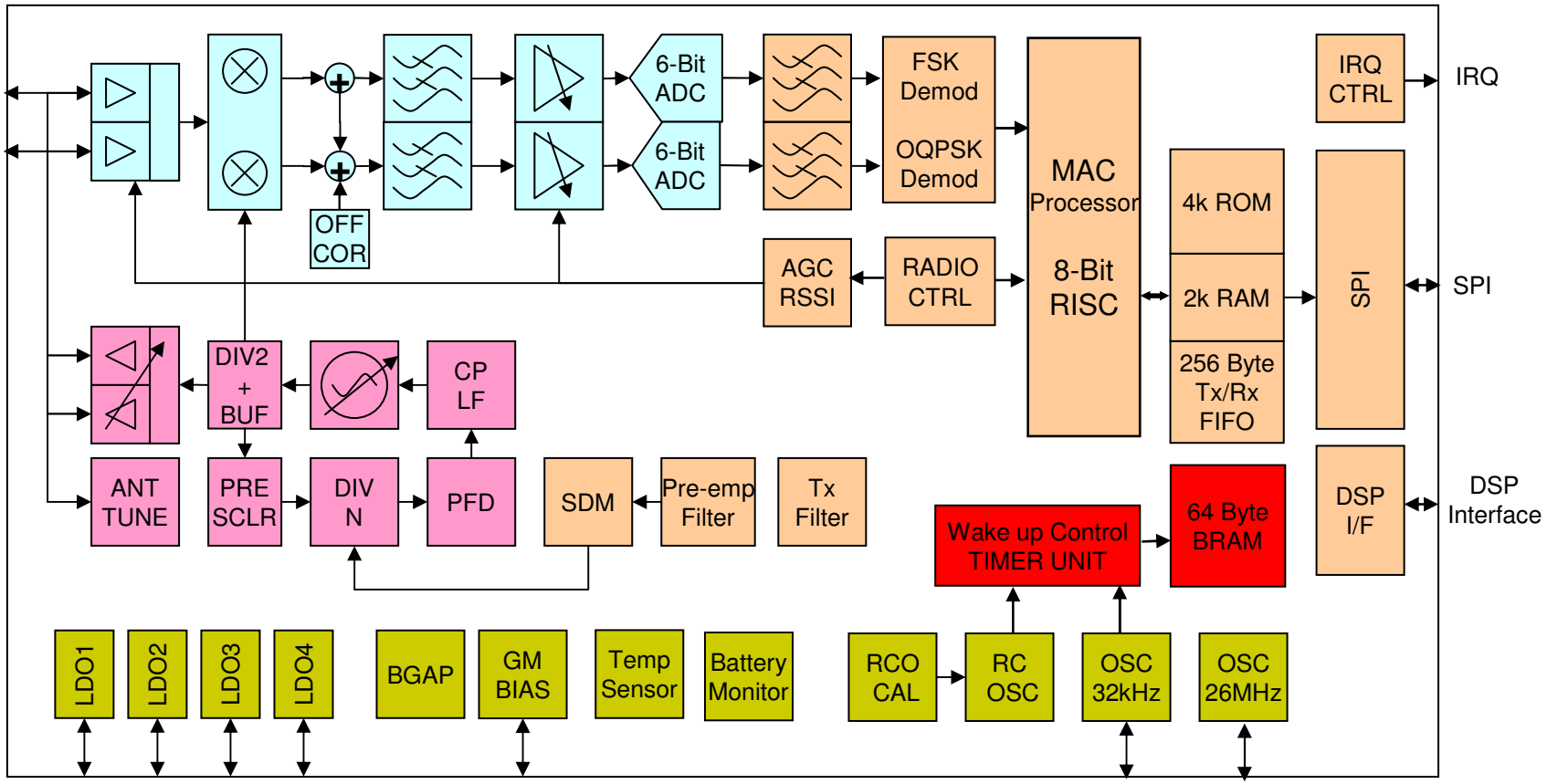
0.18um CMOS: 2.4GHz Wireless Transceiver



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ANALOG DEVICES

Product Highlights

- **Product Highlights**
  - **0.18u CMOS, 32 Pin LFCSP**
  - **Dual Modulation: IEEE 802.15.4 DSSS and 2GFSK**
    - **(a) MSK/GFSK with freq hopping**
      - **Data Rate: 65kbps to 2Mbps**
    - **(b) IEEE 802.15.4 Compliant Phy:**
      - **250kbps DSSS 2Mcps using OQPSK**
  - **Dual PA/LNA – Switched Antenna Diversity**
  - **5dBm Tx Output Power**
  - **On Chip Packet handler & 128 Byte Tx/Rx FIFO - for Packet based Telemetry**
  - **On Chip 32kHz wake-up timer – Packet sniffing**
  - **On chip battery backup RAM**
  - **Low Power 18mA Rx**

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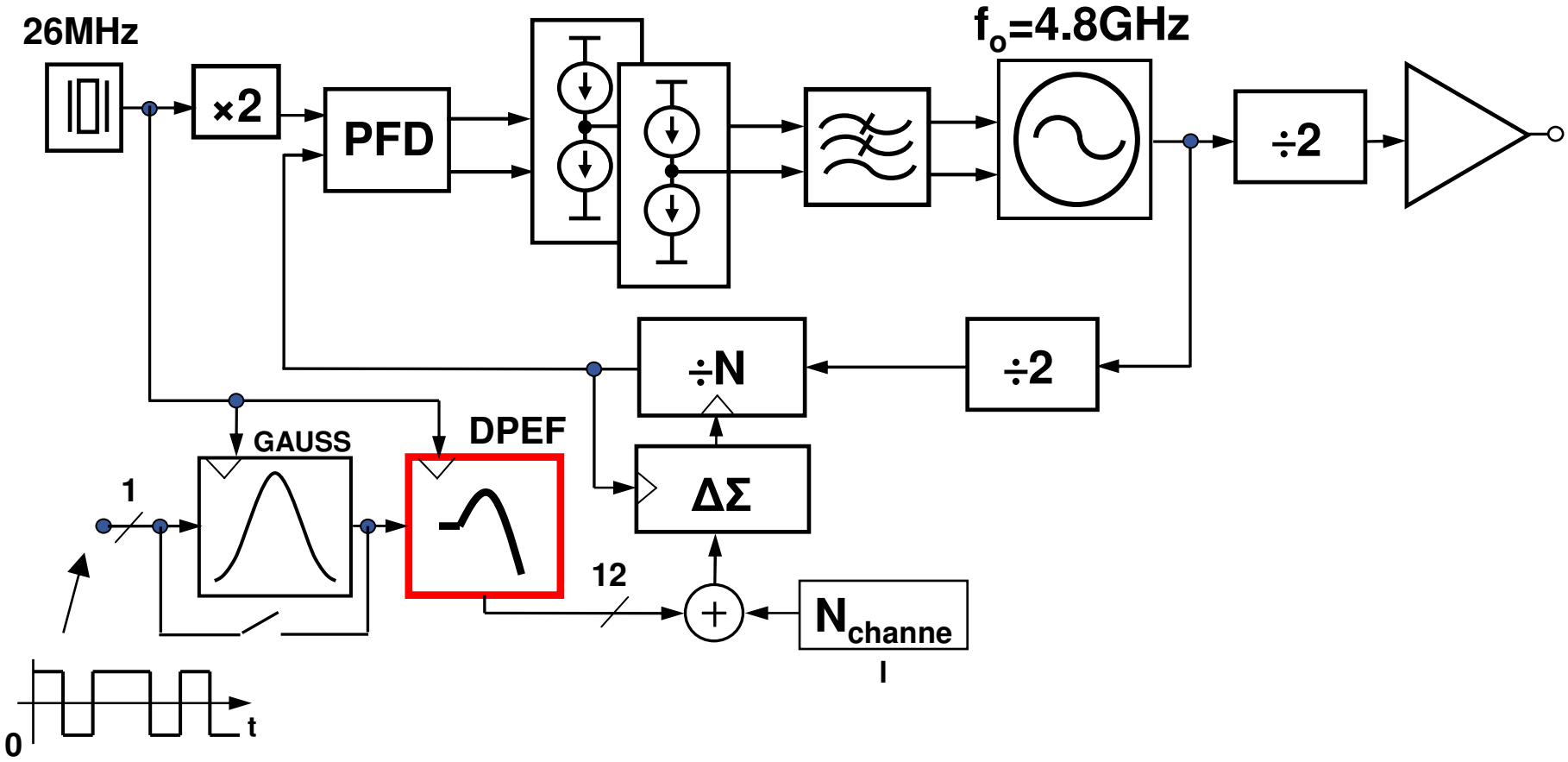
RF Transmitter Architecture



- PLL CLBW of 520kHz
  - Widest possible bandwidth meeting the spectral mask
  - Lower order digital pre-emphasis filter

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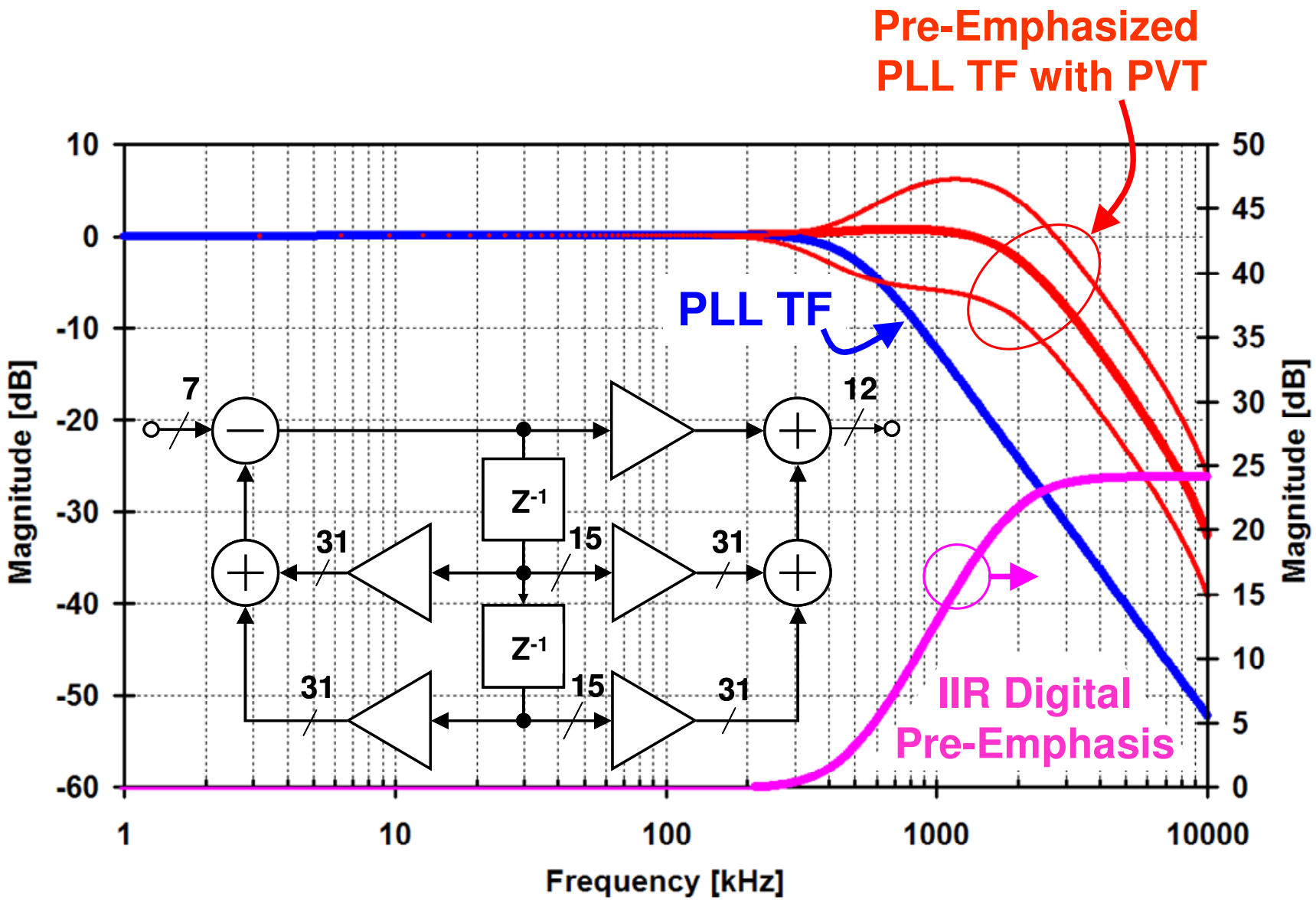
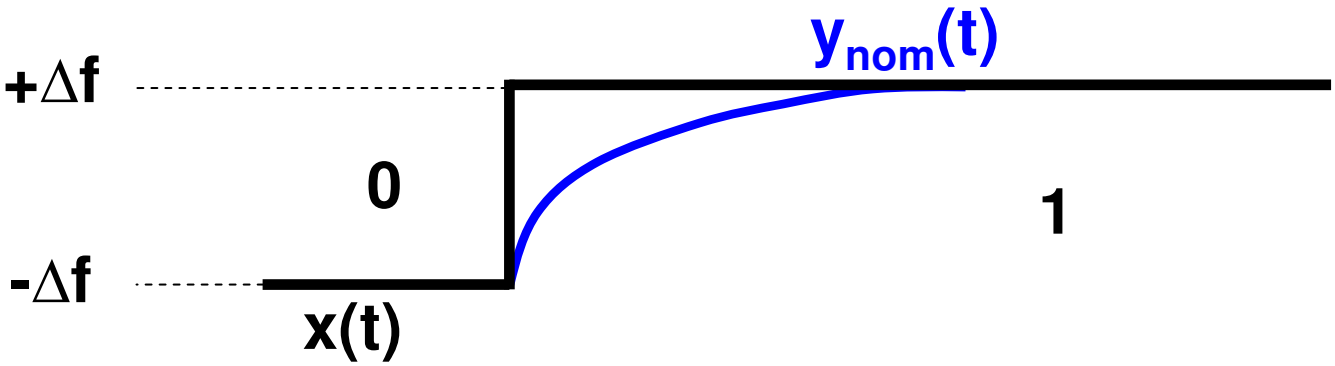
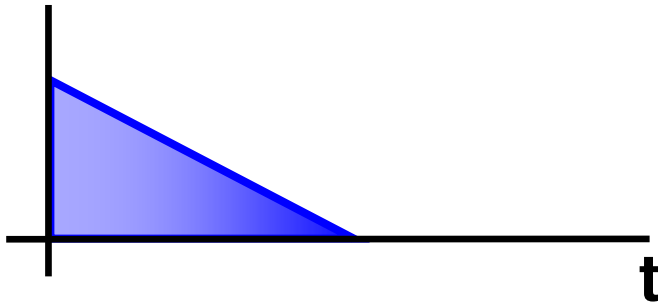
Digital Pre-Emphasis Filter

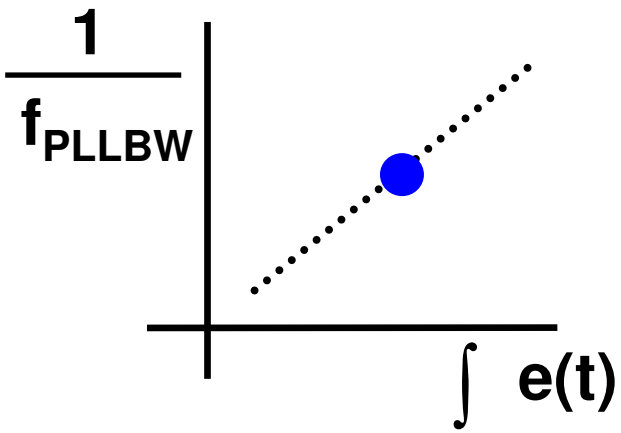


Calibration Scheme Concept



$$e(t) = X(t) - y(t)$$





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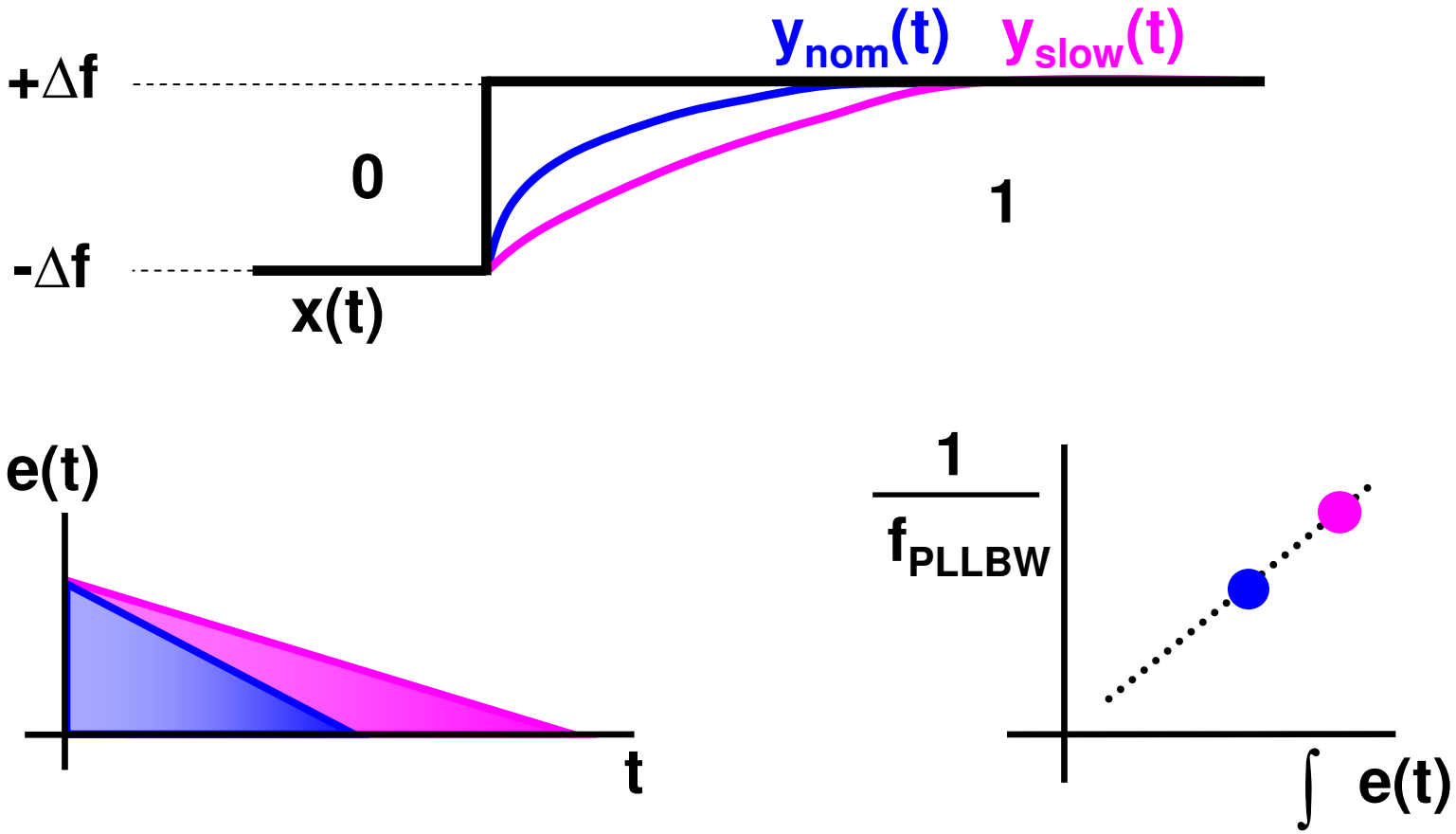
Calibration Scheme Concept



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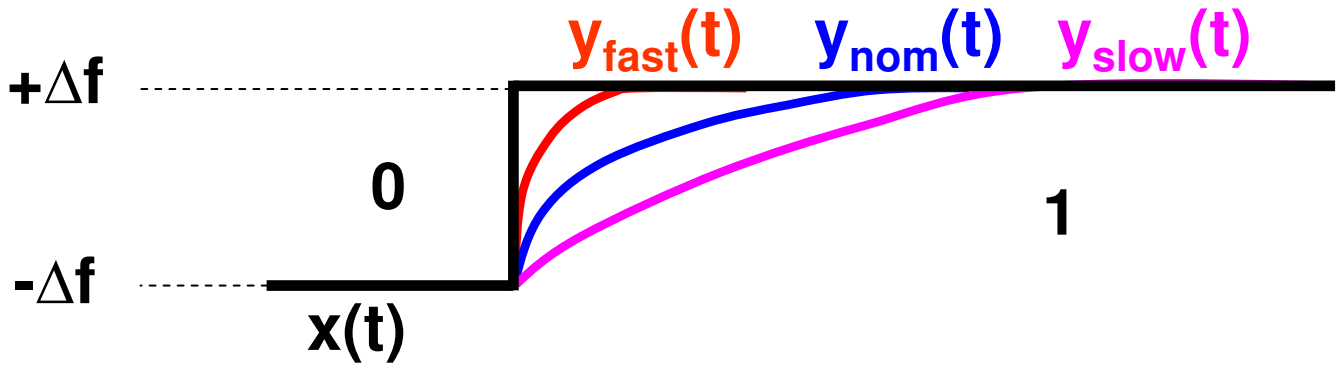
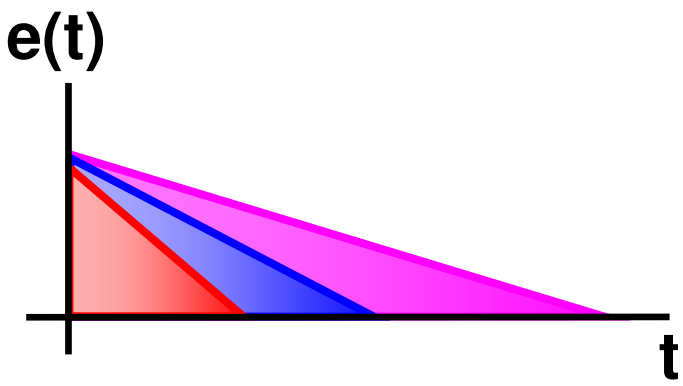
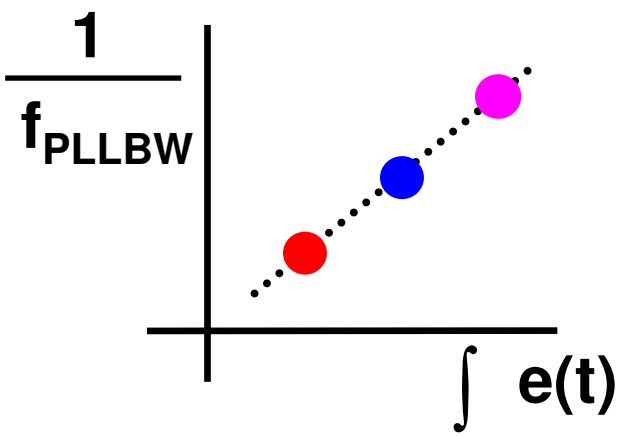
Calibration Scheme Concept







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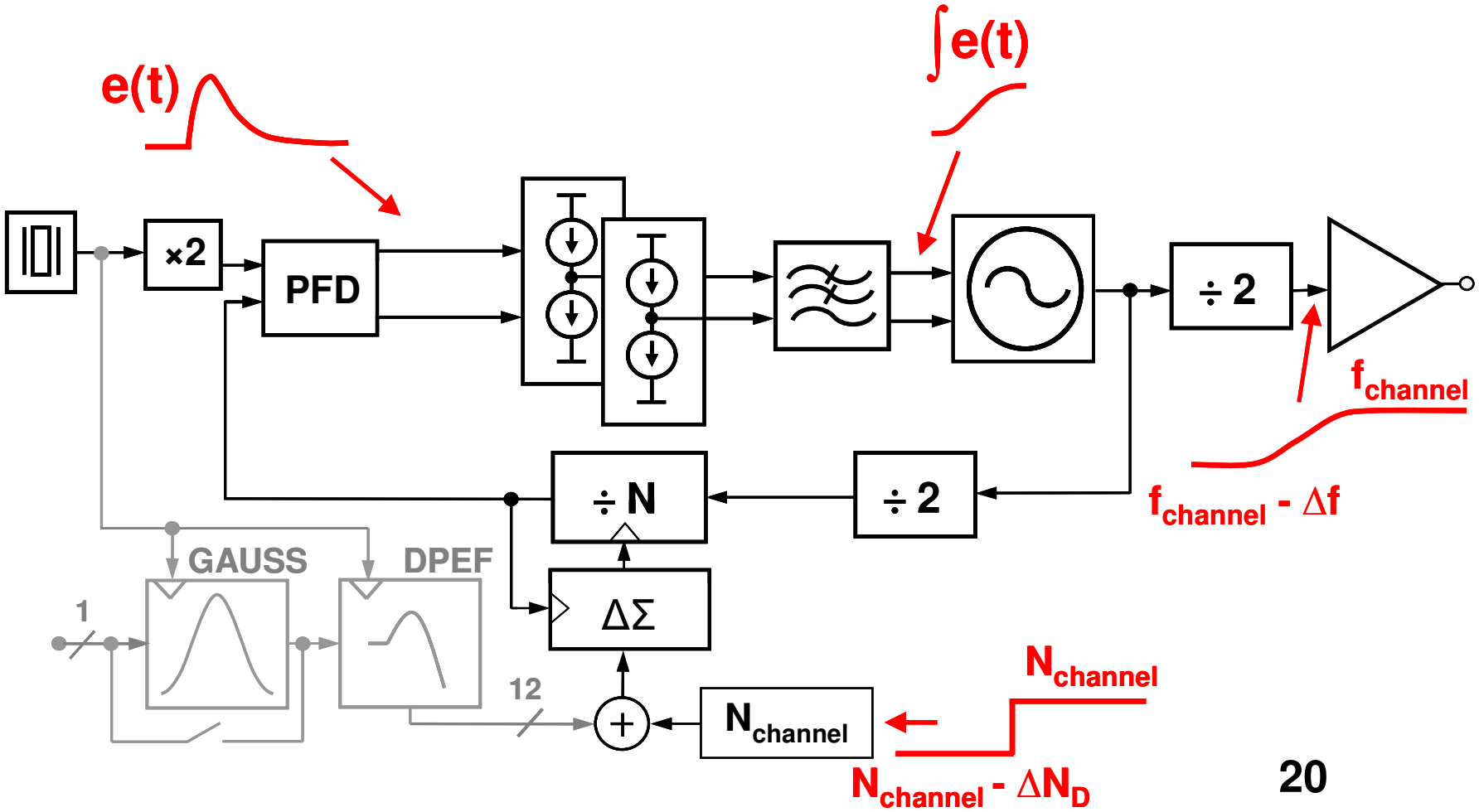
Calibration Scheme Implementation



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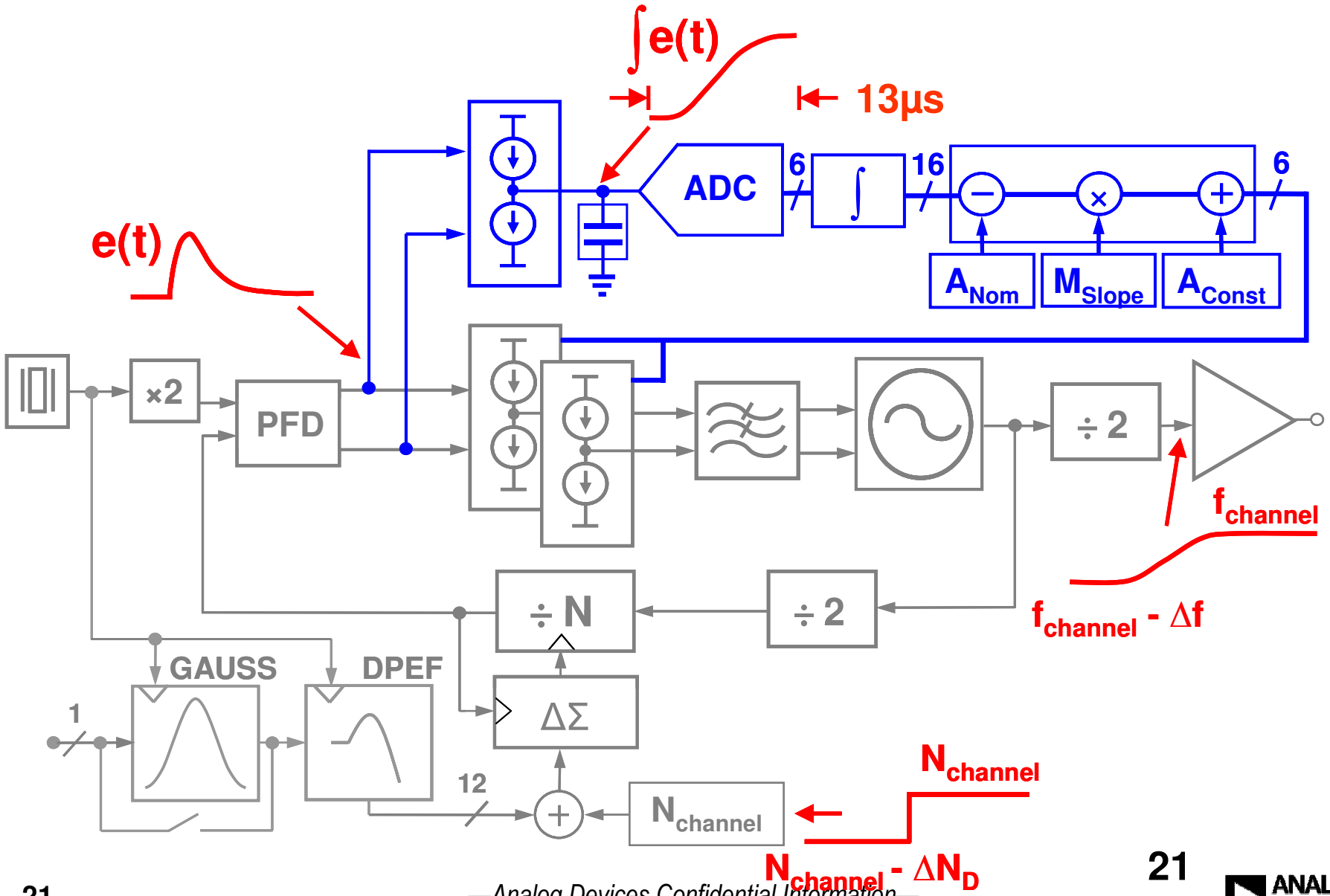
Calibration Scheme Implementation



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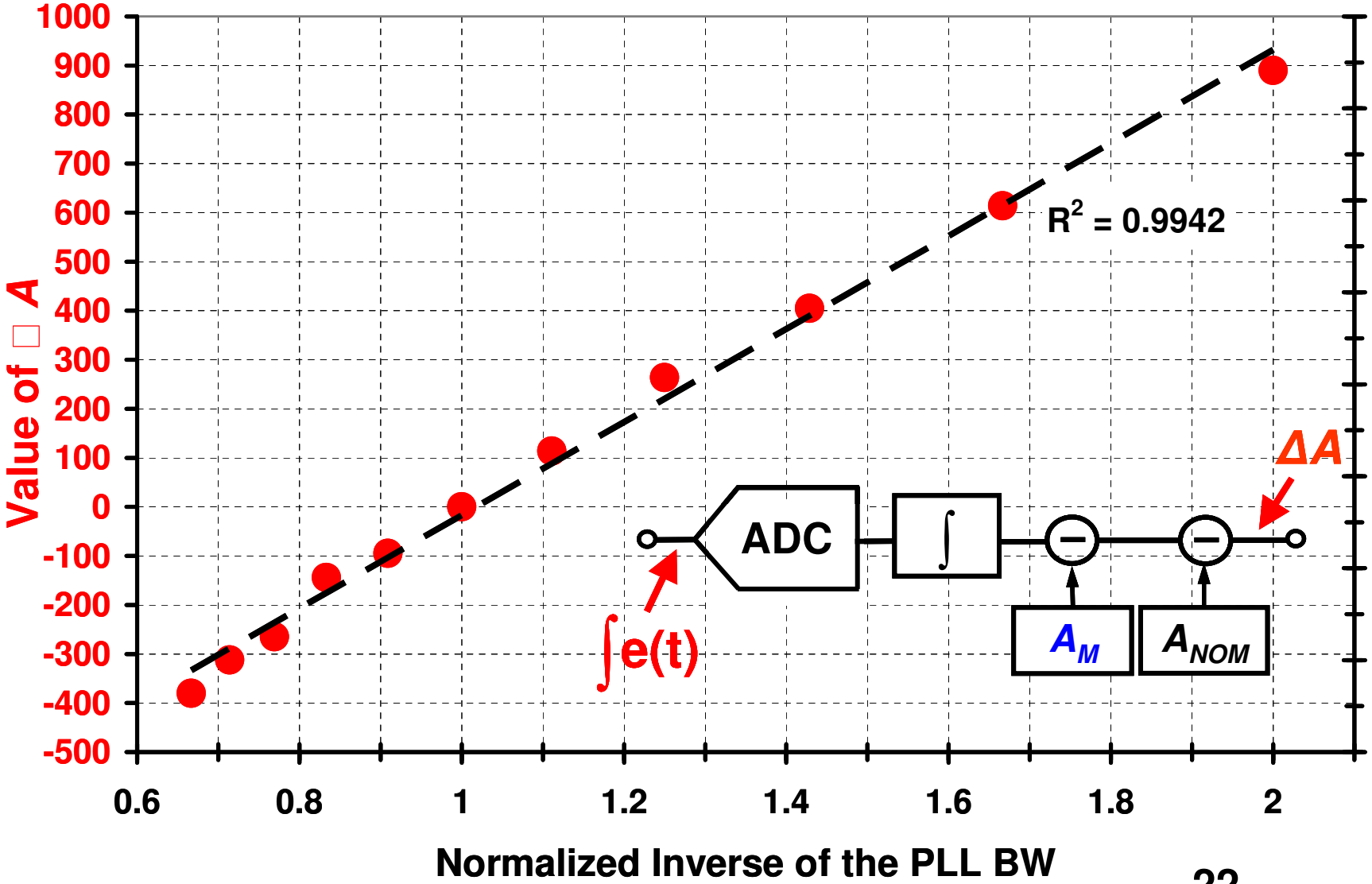
Linearity of the Calibration Signal



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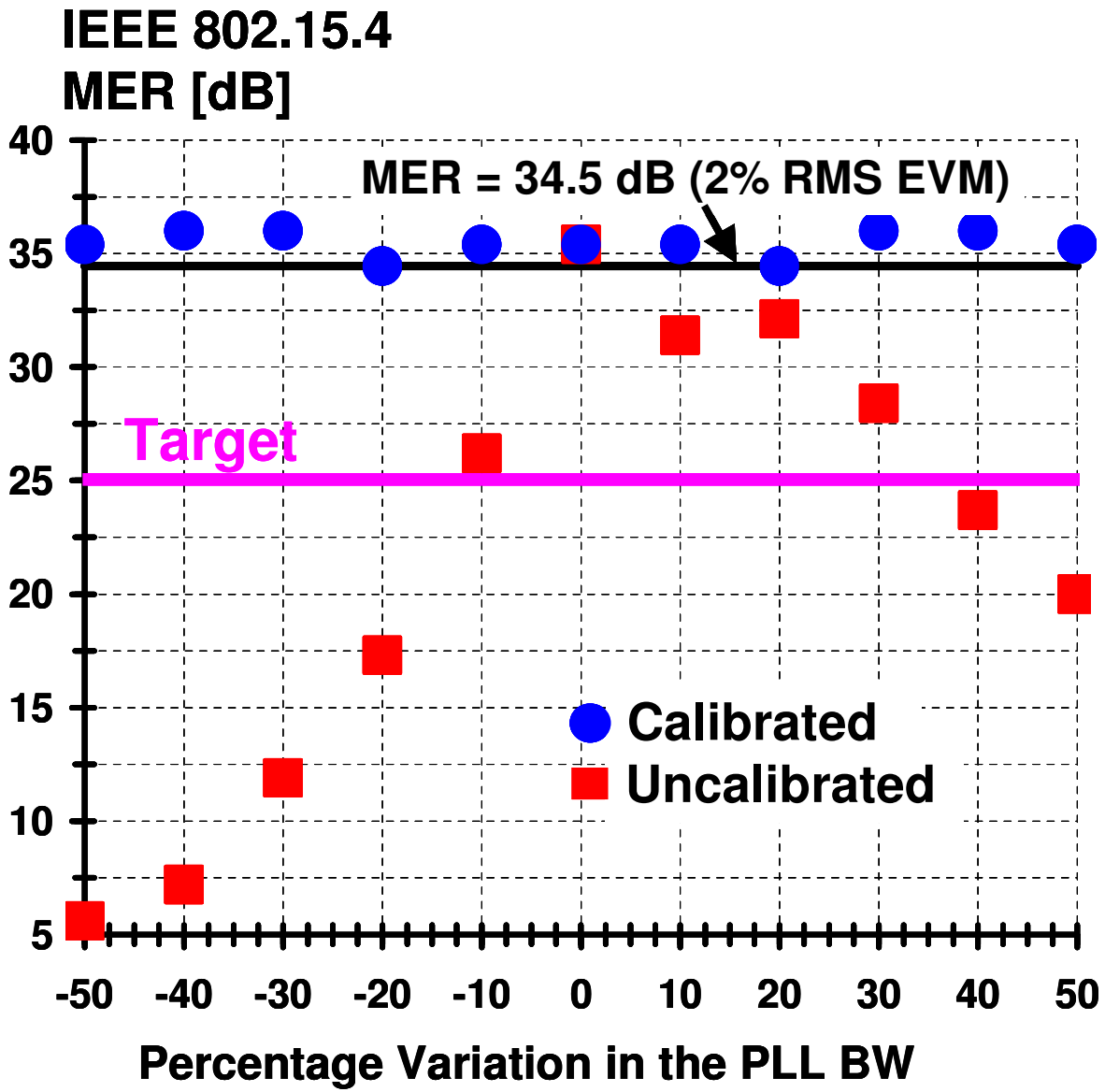
RF Transmitter Calibrated Performance



- Pout = 3dBm, 2.48GHz
- GMSK Filter BT = 0.5

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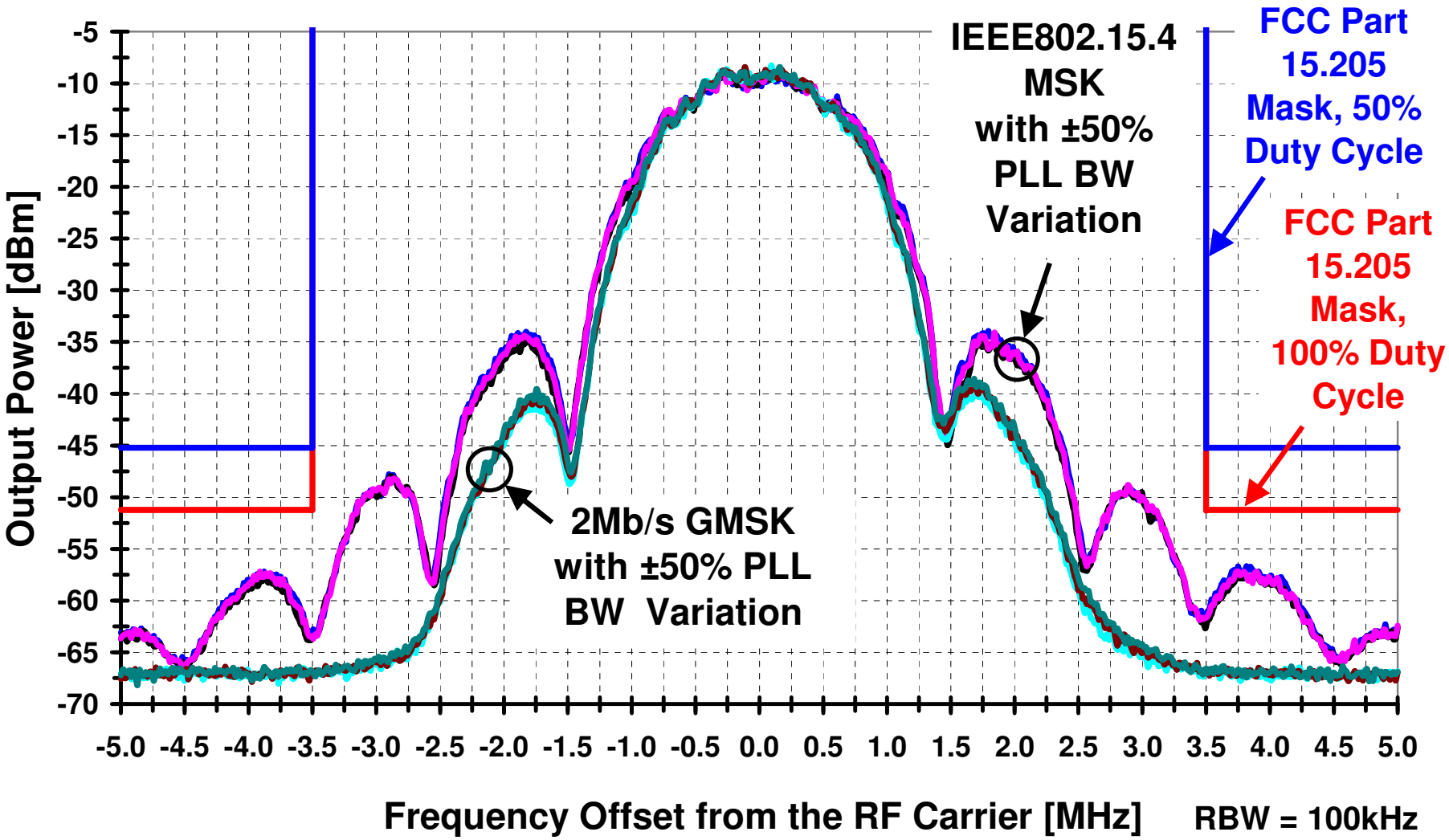
RF Transmitter Calibrated Spectrum



- Spurious components < 50dBc
- P_{out} = 3dBm, 2.48GHz

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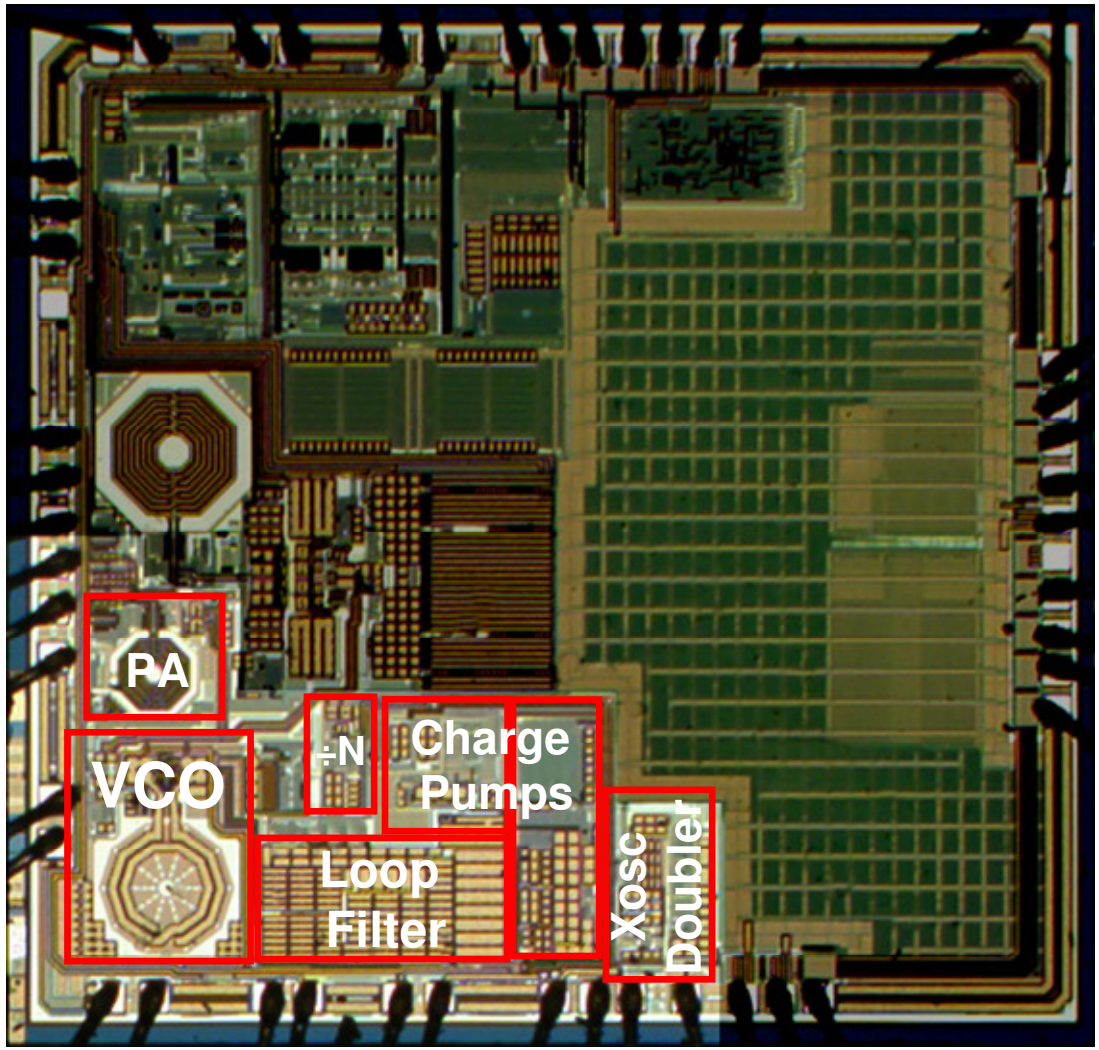
Chip Micrograph



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Summary

Summary:

Presented two topics using digitally enhanced RF:

- Use of Digital Calibration to improve Receiver Image Rejection
- Use of Digital Pre-emphasis to Extend Transmitter Bandwidth

End

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