technische universiteit eindhoven

# Calibration of Current Steering D/A Converters

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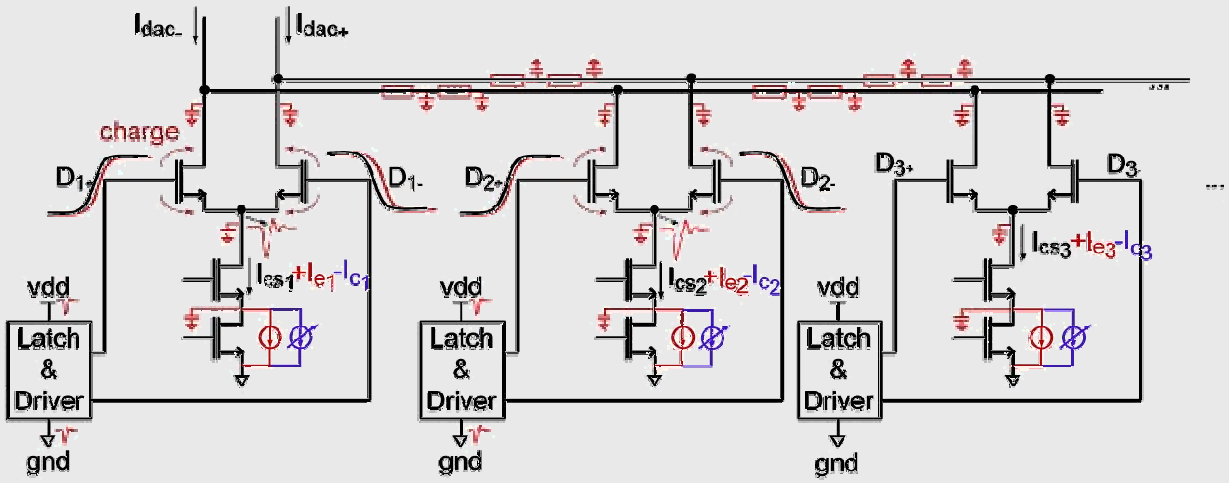
# Current-steering D/A converters




Applications demand performance;

**Errors** limit performance;

Small errors demand huge resources.

***Correction methods:***

***Improve*** *performance and*

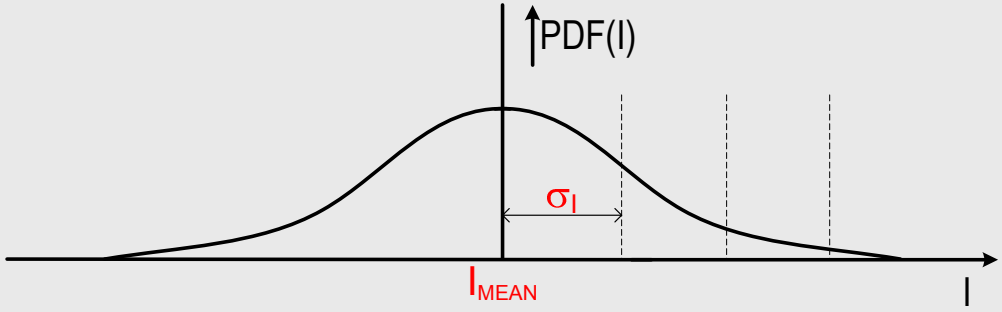
***Relax*** *design requirements*

# Overview

- Mismatch problem;
- Current calibration method;
- MSB unary currents calibration in a 12b 250nm DAC
- All (MSB unary and LSB binary) currents calibration in a quad-core 12b 180nm DAC;
- All currents calibration in a 12b-16b flexible 40nm DAC
- Conclusions

# Mismatch problem

- Elements' real values deviate
- Deviation depends on:
  - Area
  - Tech. and Circuit parameters
- High resolution D/A require
  - Many and accurate elements
  - Large silicon areas
- Large silicon areas cause
  - Systematic errors
  - Drop of performance




$$\left(\frac{\sigma_I}{I}\right)^2 \approx \frac{K}{(W \times L)_I}$$

$$INL_{\max} \approx n \cdot \left(\frac{\sigma_I}{I}\right)$$

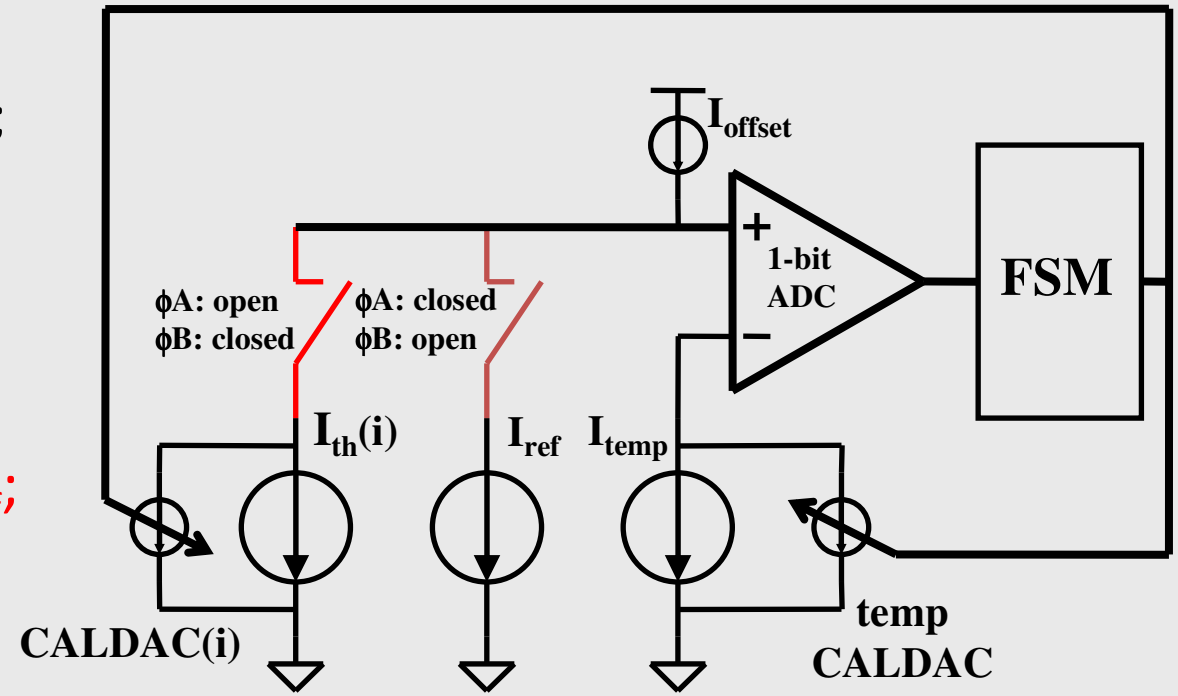
# Start-up calibration scheme

- Mismatch correction;
- Input offset cancellation;
- Two phases: ϕA, ϕB;

  ϕA: $I_{temp}=I_{ref} - I_{offset}$;

  ϕB: $I_{th}(i)=I_{temp} + I_{offset}=I_{ref}$;

  with $I_{ref}=\Sigma I_{bin} + I_{LSB}$;
- Simple logic: 8-state FSM.

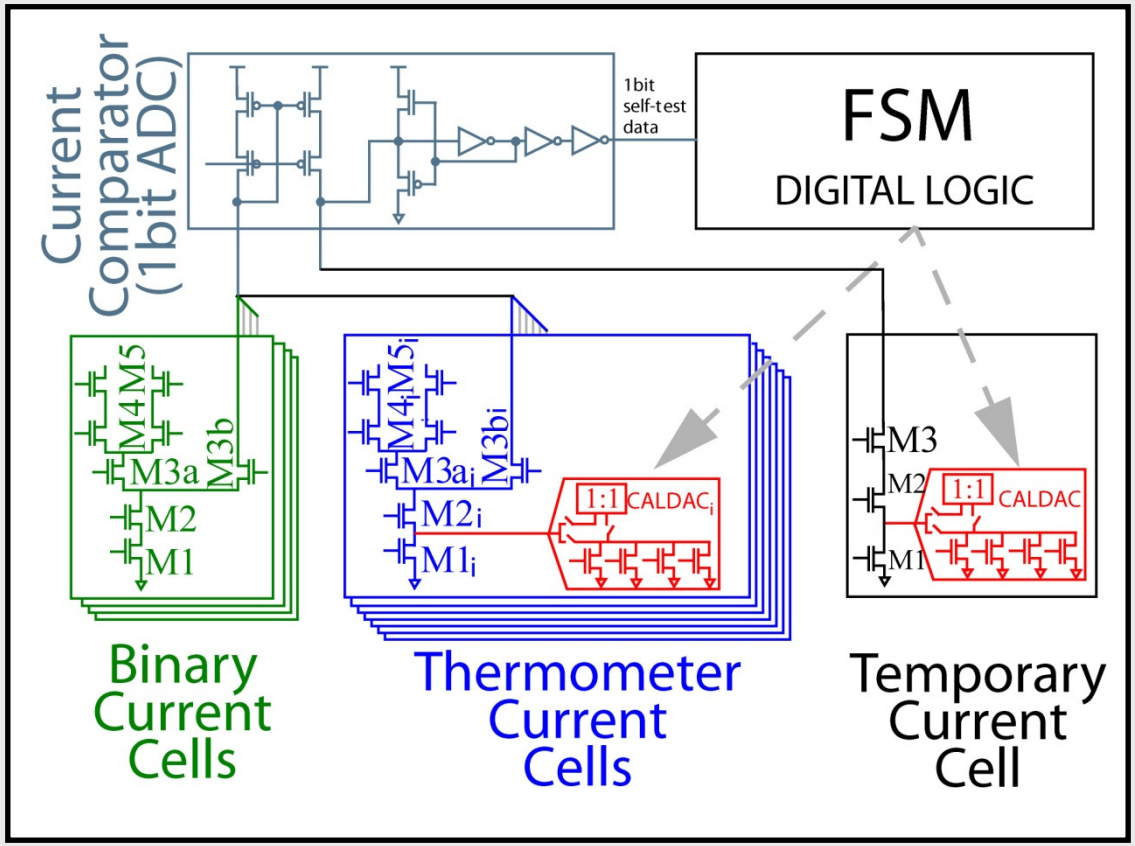


# 12bit self-calibrating DAC in 250nm CMOS,

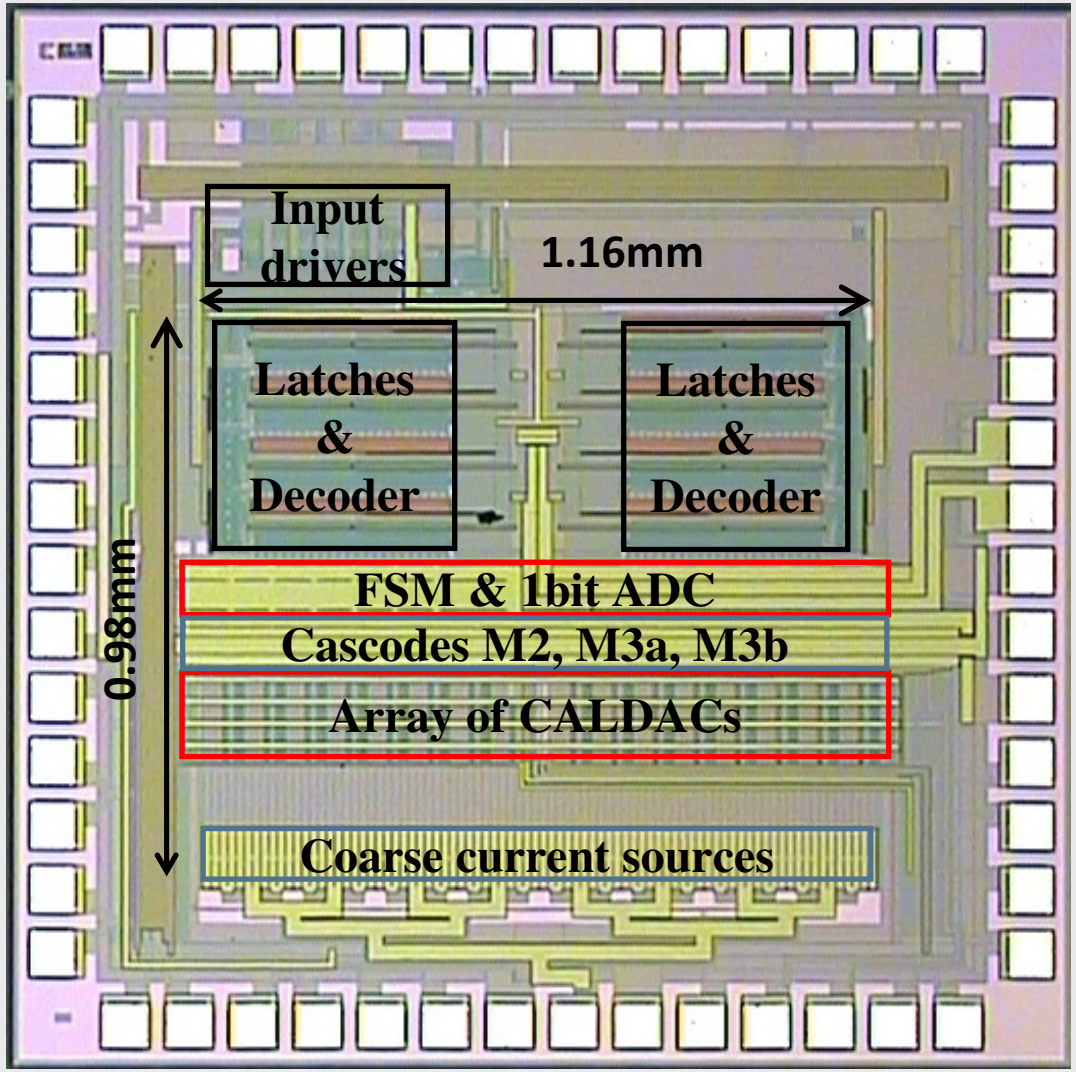
see ESSCIRC’05

# 12bit DAC implementation

- 12b current-steering DAC;
- Segmentation: 6LSB/6MSB;
- 63 thermo bits calibrated;
- 6 binary not calibrated;
- Reference: binary bits;
- 5bit signed CALDACs;
- CMOS 0.25µm; Vdd 2.5V.

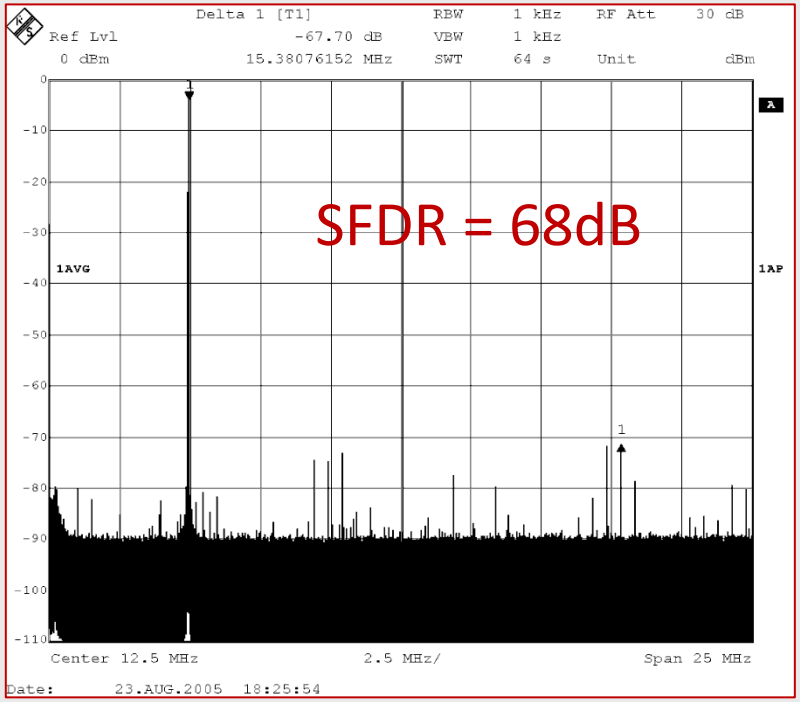


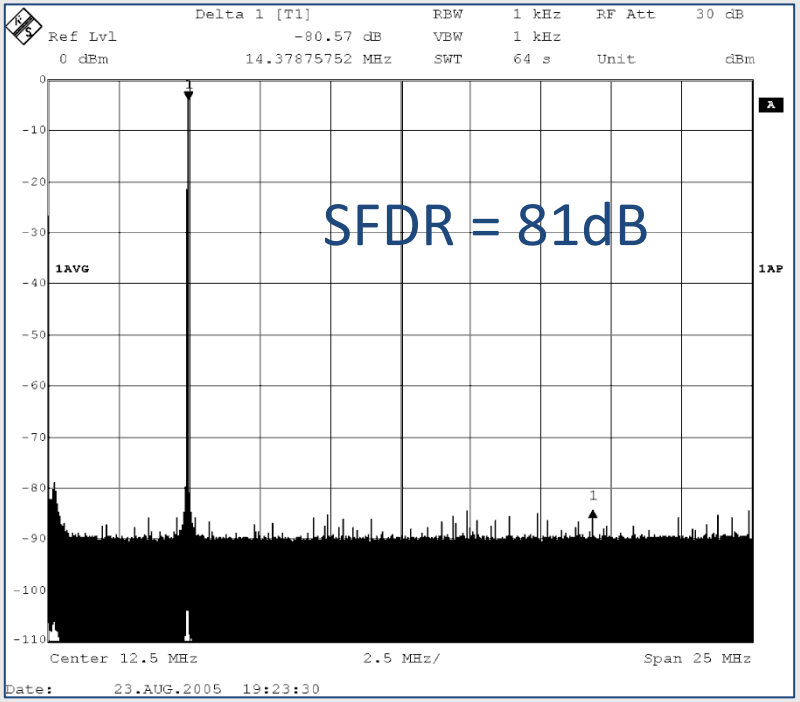
# Chip micrograph




- CMOS 0.25µm, 1P5M;
- Coarse (main) current sources designed for 10b accuracy in 0.1mm$^2$;
- Fully integrated self-calibration in 0.3mm$^2$;
- 5 extra pads for calibration: 4 in & 1 out;

# Self-calibration of MSB unary currents measurements

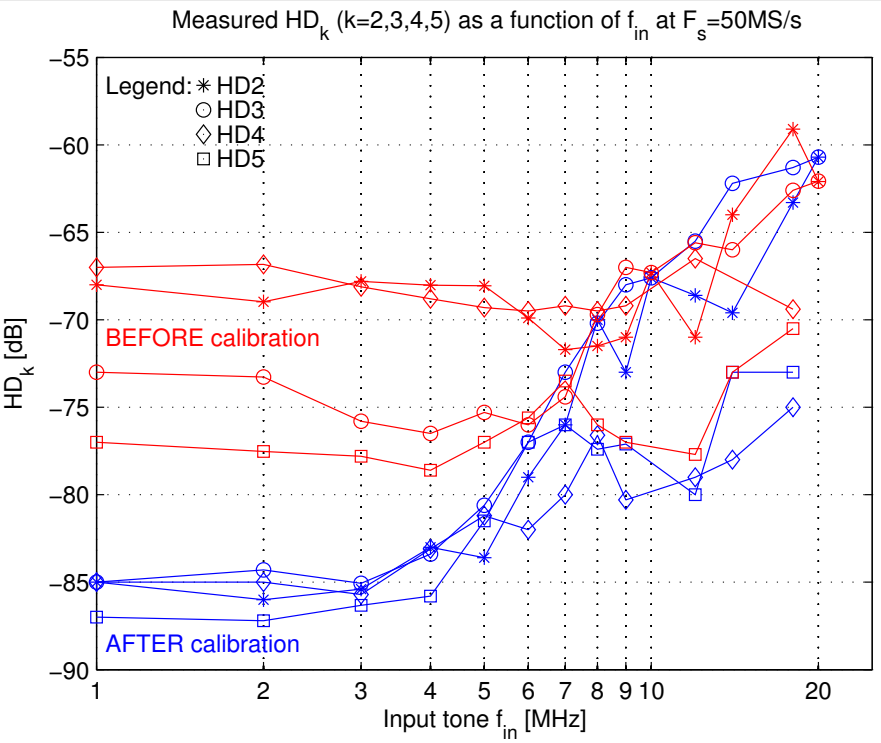


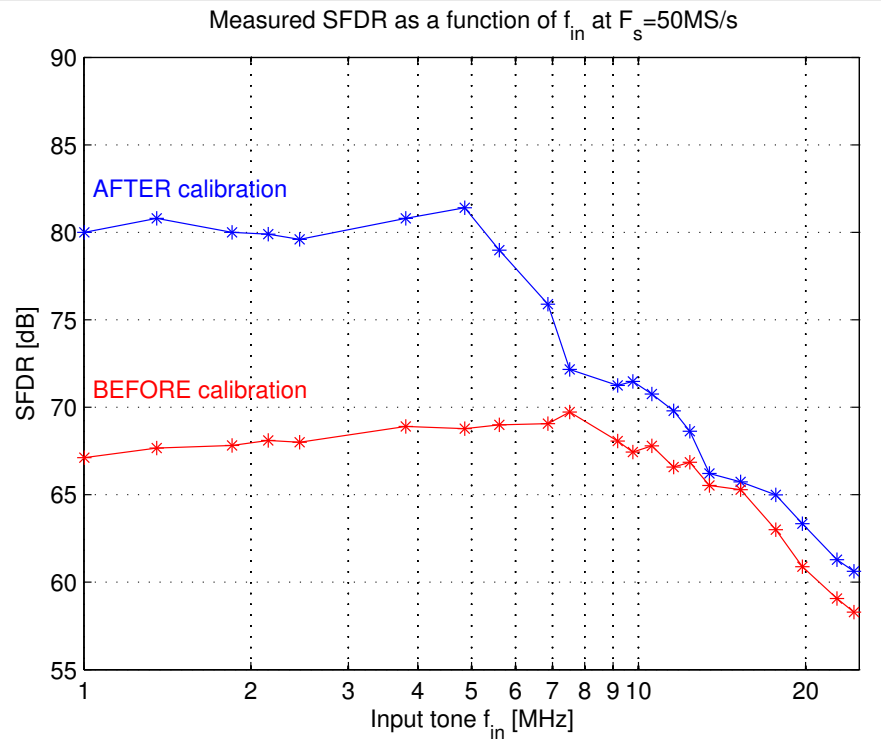

Before calibration $\xrightarrow{+13\text{dB}}$ After calibration

# Self-calibration of MSB unary currents measurements

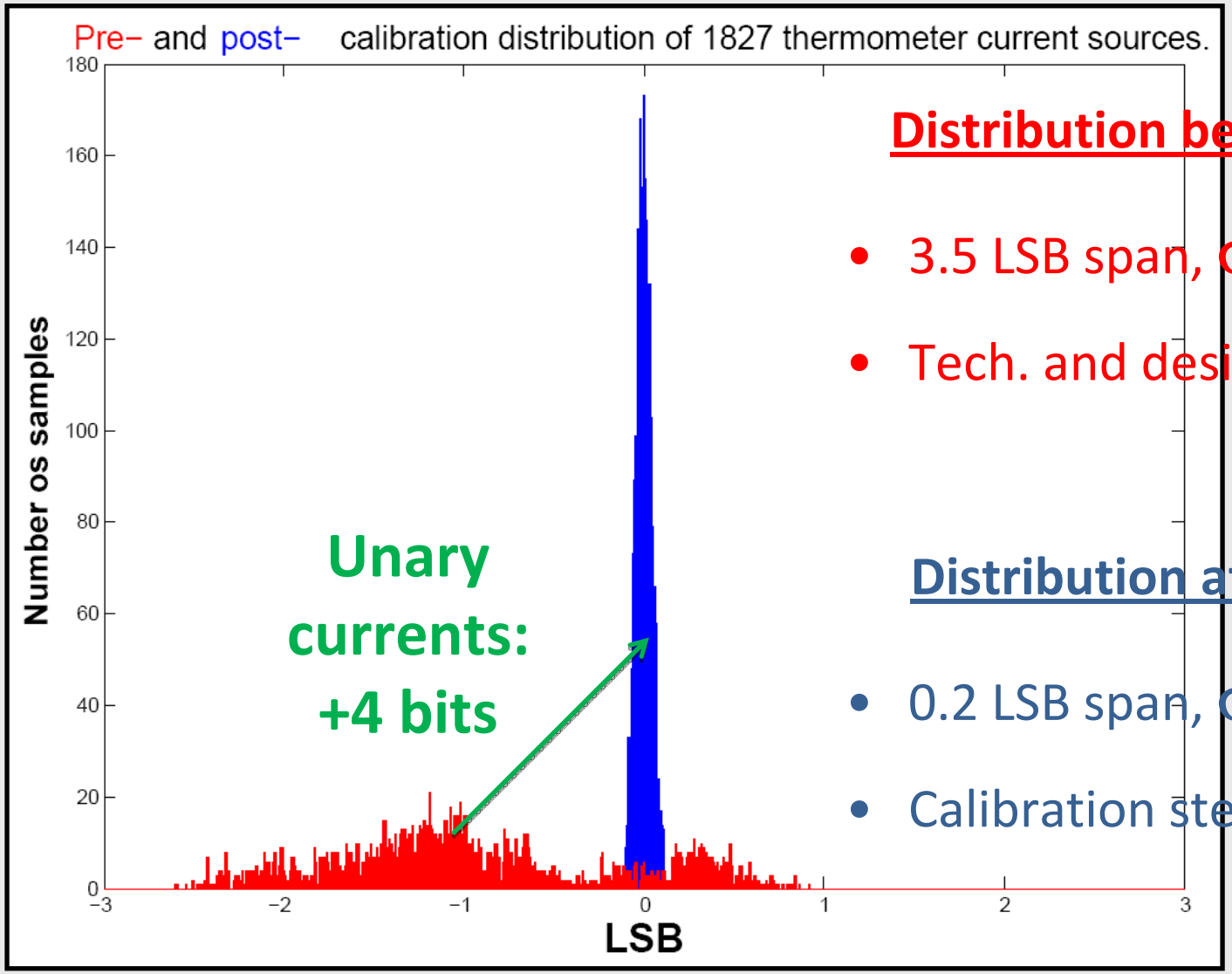
## HD (2,3,4,5) (max) improvement +18dB




## SFDR improvement +13dB



# Calibration potential



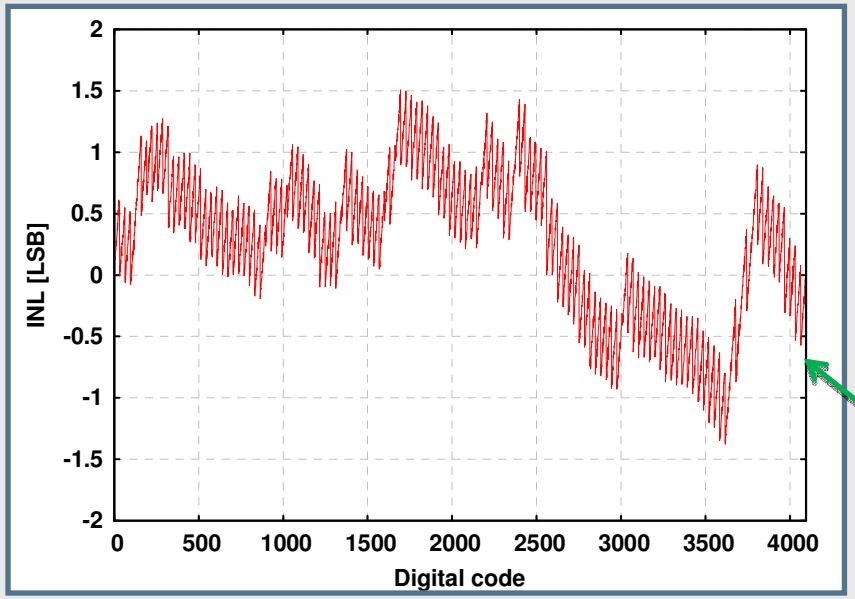

**Distribution before calibration**

- 3.5 LSB span, σ=1.06LSB;
- Tech. and design tolerances;

**Distribution after calibration**

- 0.2 LSB span, σ=0.03LSB;
- Calibration step sets the span;

# Static performance




Before

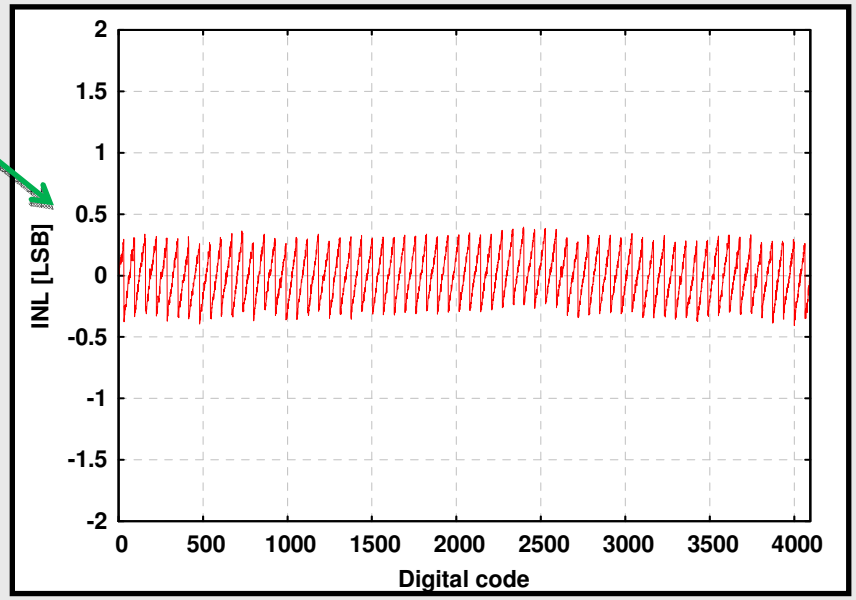
10b

- MSB unary part dominate;
- $INL_{max}$ = 1.5LSB;

**INL: +2b**

After

12b




- LSB non-calibrated binary part dominate;
- $INL_{max}$ = 0.4LSB

# Calibration of binary currents

Binary → no redundancy

New sub-DAC segmentation (M binary sets) → redundancy

$$1: I_{bin}(B)(1) + \underbrace{\sum_{i=1}^{B-1} I_{bin}(i)(1) + 1LSB}_{I_{ref_bn}} := I_{ref_u}^{su}$$

$$2: I_{bin}(B)(2) + \underbrace{\sum_{i=1}^{B-1} I_{bin}(i)(1) + 1LSB}_{I_{ref_bn}} := I_{ref_u}^{su}$$

$$3: I_{bin}(B)(1) + I_{bin}(B)(2) := I_{ref_u}^{su}$$

equal

1/2

# 12b-14b self-calibrating flexible DAC in 180nm CMOS,

see APCCAS'08

# Parallel sub-DAC units architecture

**Current-steering DACs:**

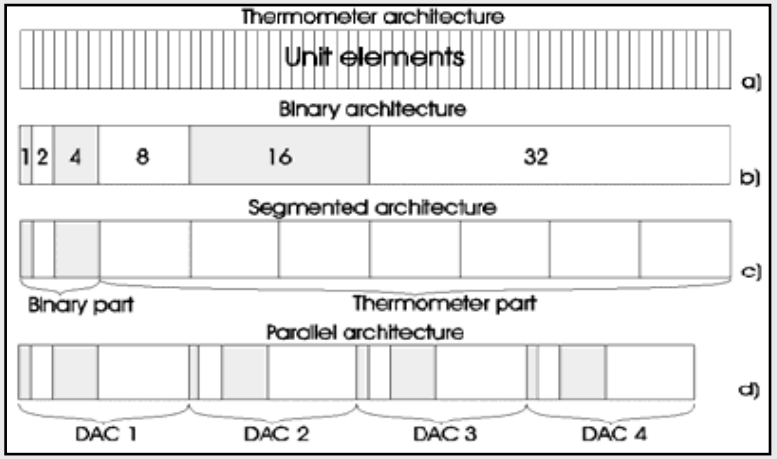
Parallel current sources (switch current cells), which are switched in groups to create the analog output;

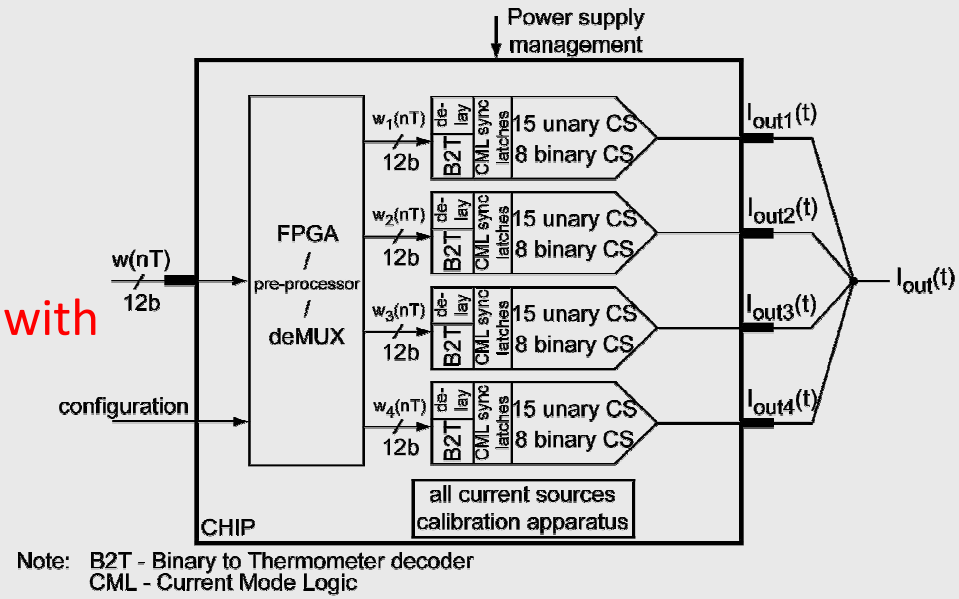
a) Unary (Thermometer) grouping;

b) Binary grouping;

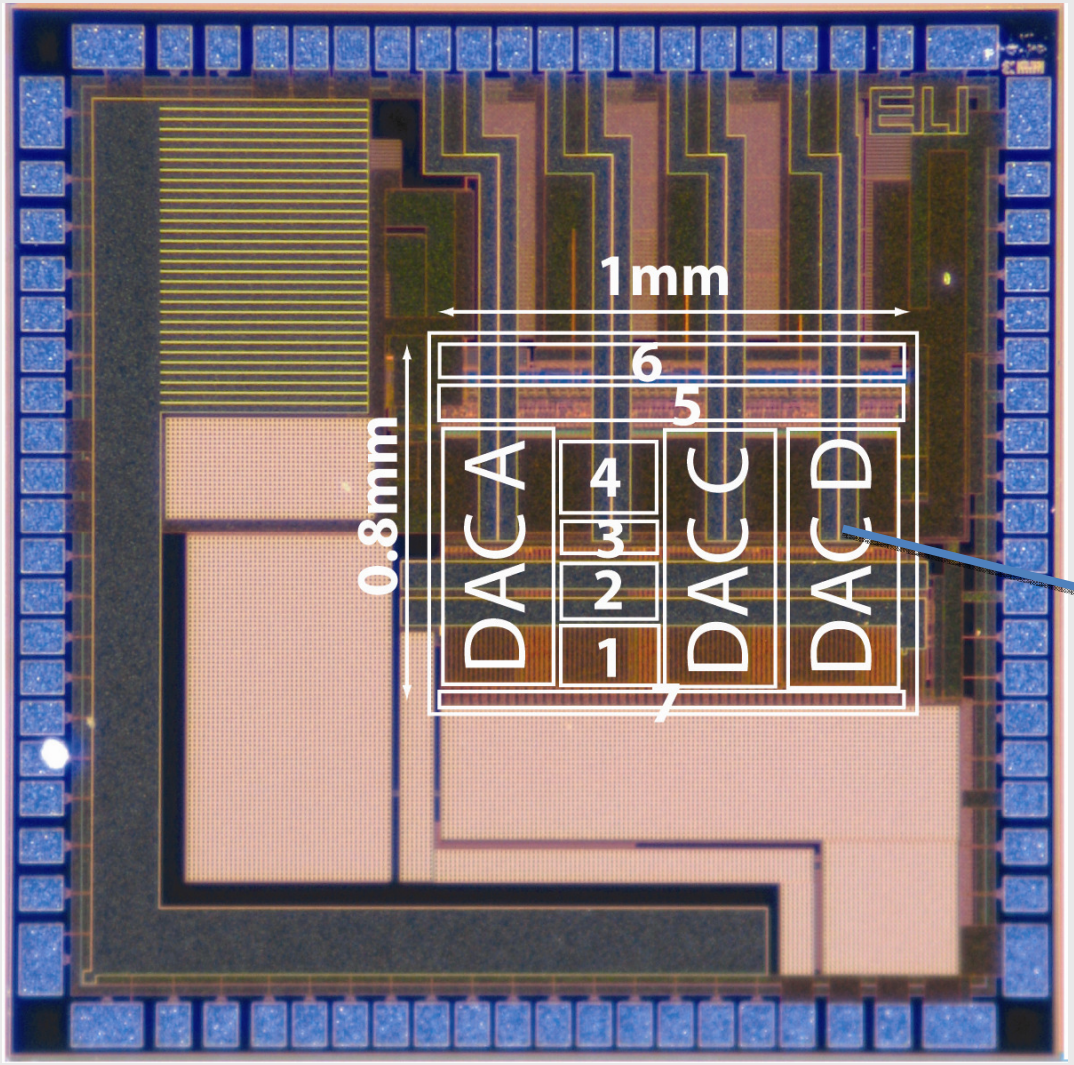
c) Segmented grouping;

d) Our NEW grouping: parallel sub-DACs (with an exemplary implementation).

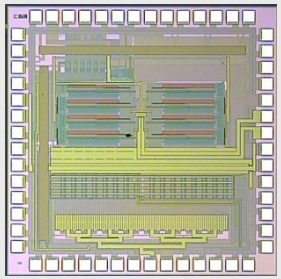


# A 12-bit self-calibrated quad-core current-steering DAC




recall:



**1mm² for the presented 12b DAC (250nm CMOS)**

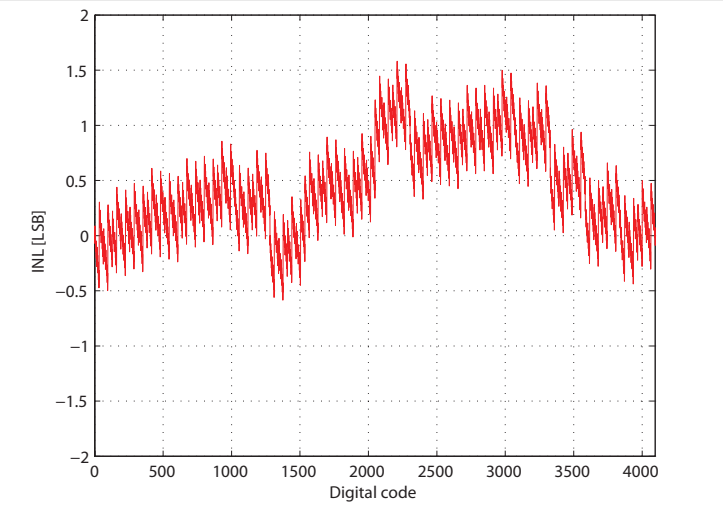
**0,2mm²**

**per 12b DAC (180nm CMOS)**

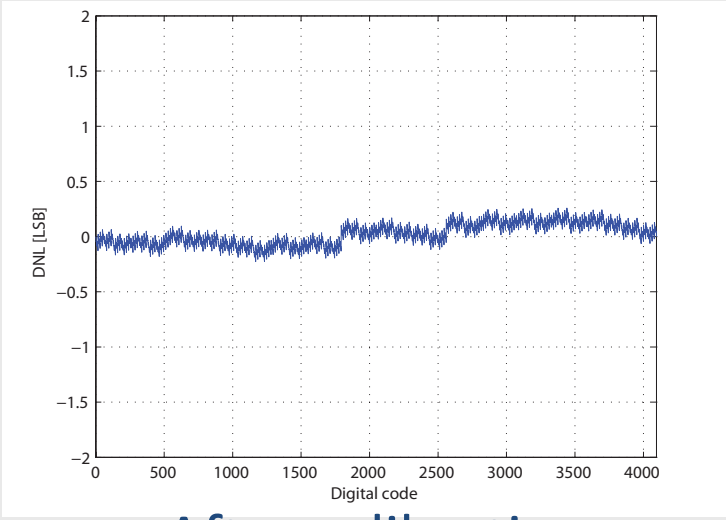
**-Large LSB binary part;**

**-Full calibration.**

# Calibration of unary and binary currents, measurements

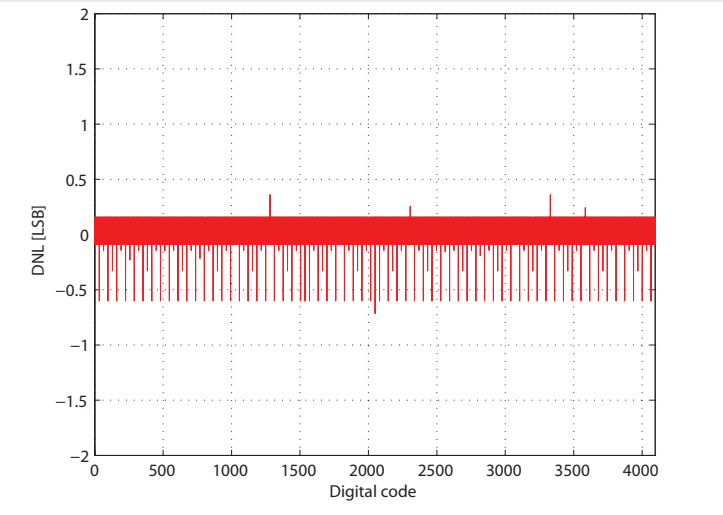



INL

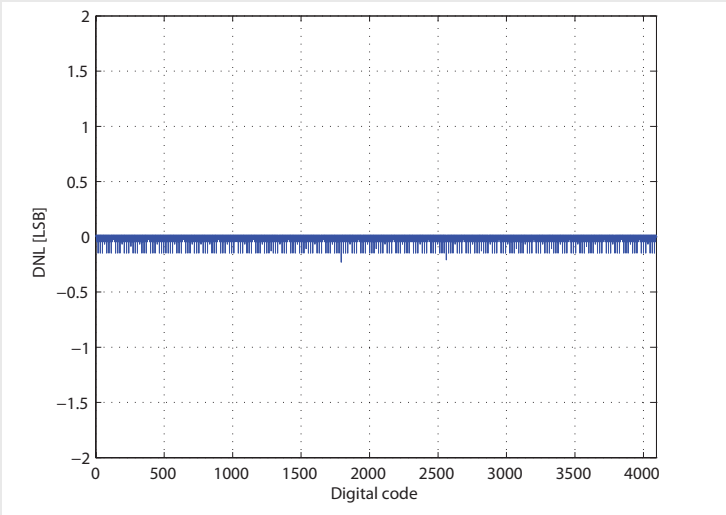



Before calibration

After calibration

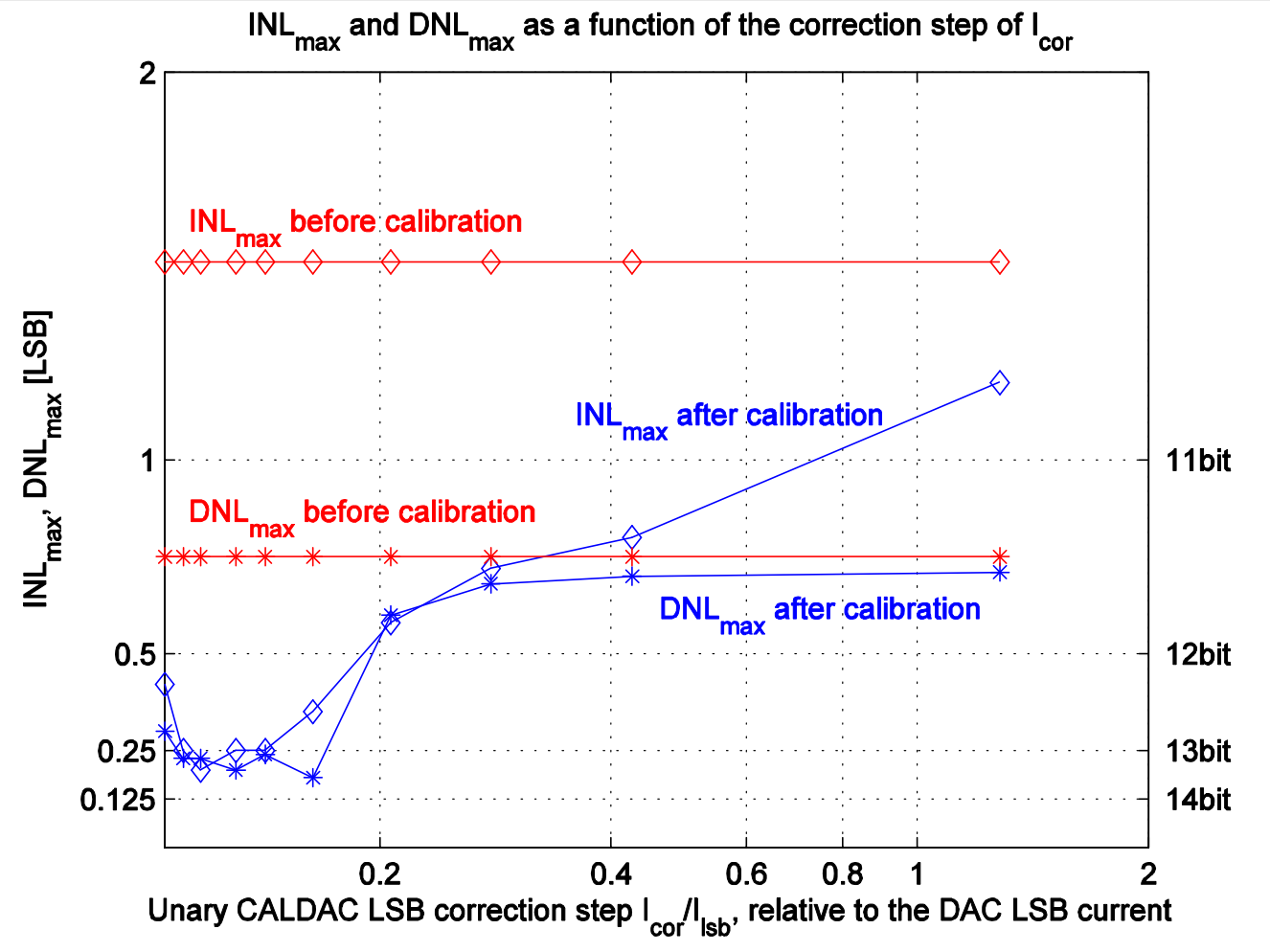



DNL

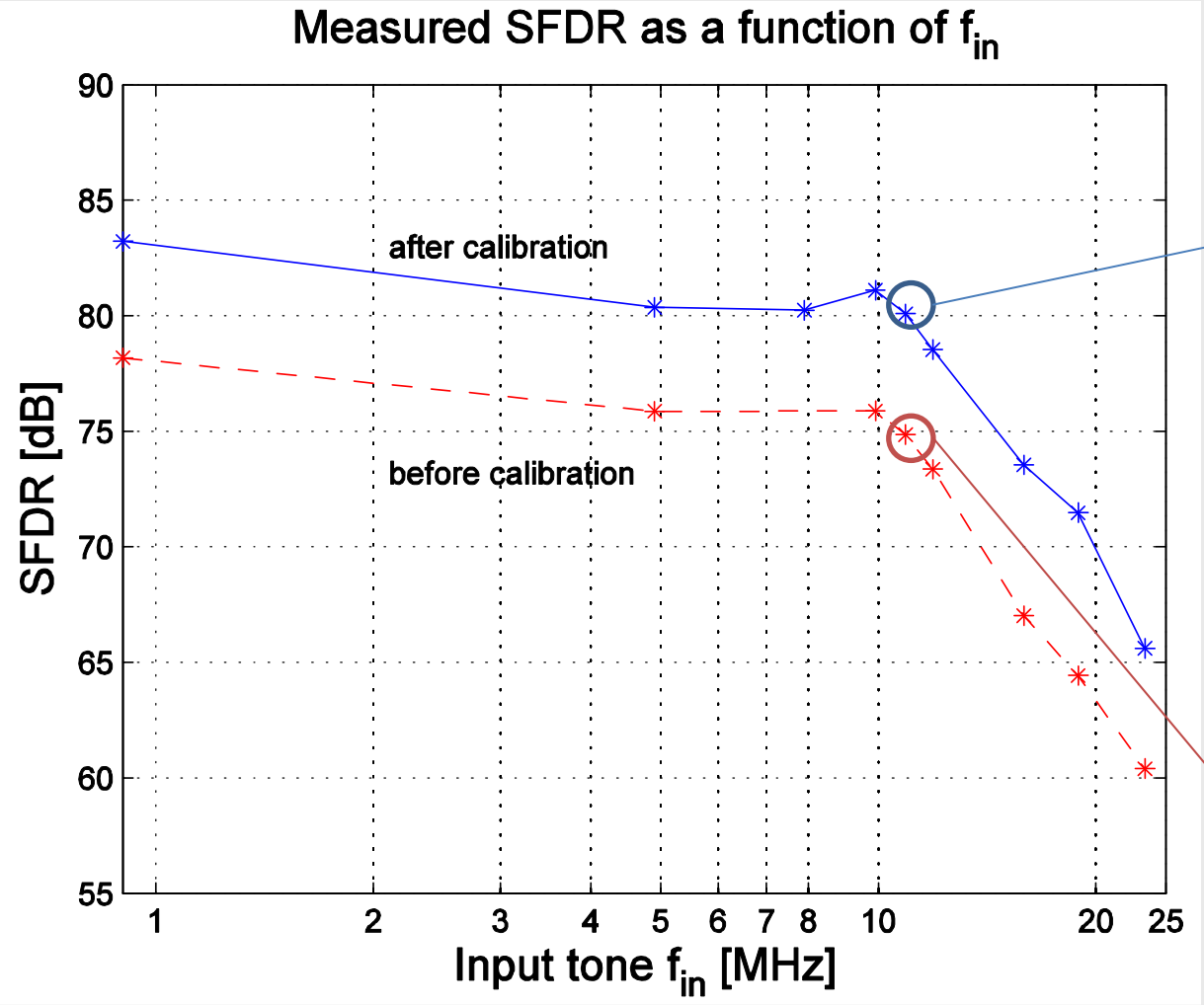


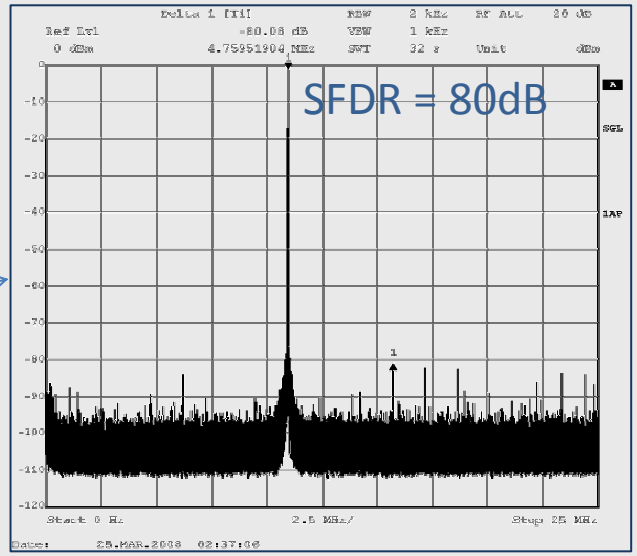
# Calibration of all DAC currents, measurements

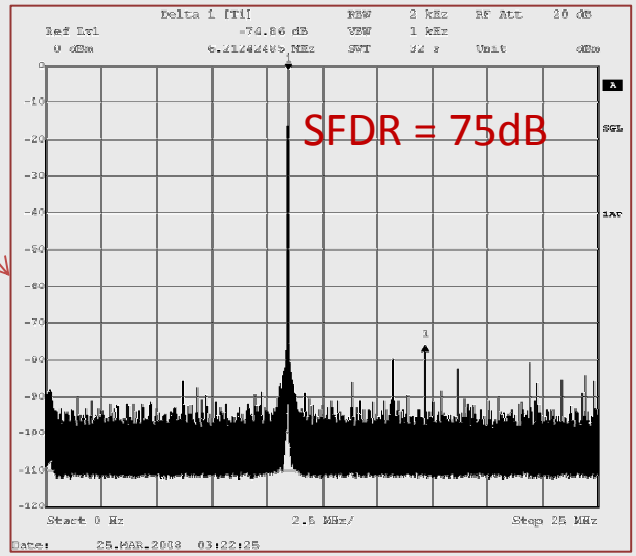
## DAC accuracy depends only on a design parameter



# Calibration of all DAC currents, dynamic measurements



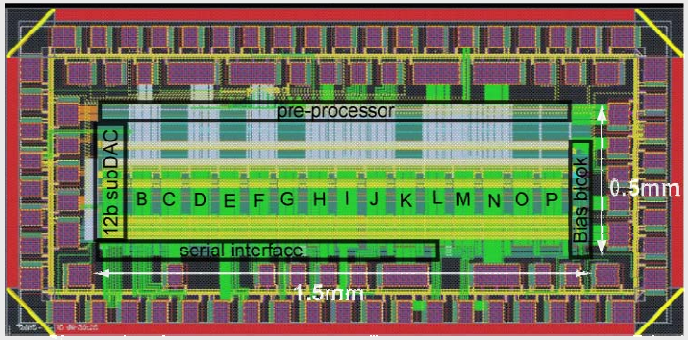



# 12b-16b self-calibrating flexible DAC in 40nm CMOS,

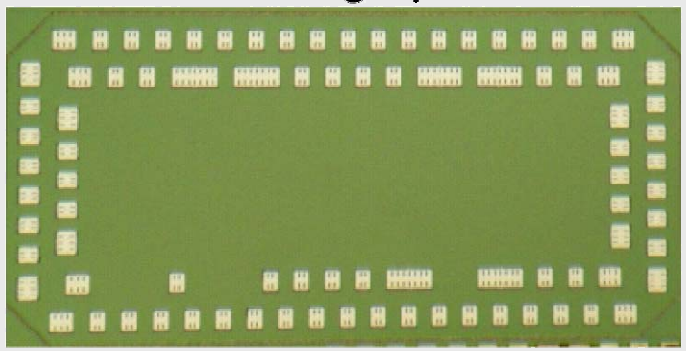
unpublished yet

# A 12b-16b self-calibrated flexible DAC in 40nm CMOS

Layout

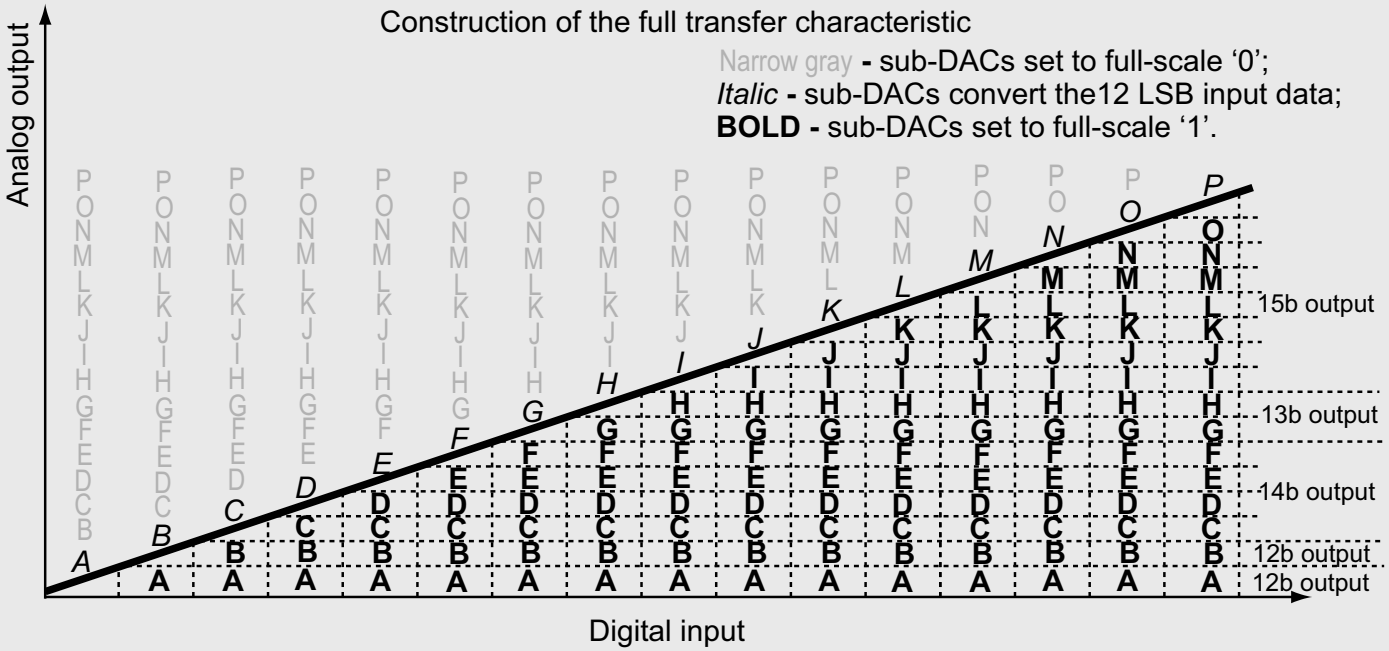



Micrograph



Construction of the full transfer characteristic

Narrow gray - sub-DACs set to full-scale '0';
*Italic* - sub-DACs convert the12 LSB input data;
**BOLD** - sub-DACs set to full-scale '1'.

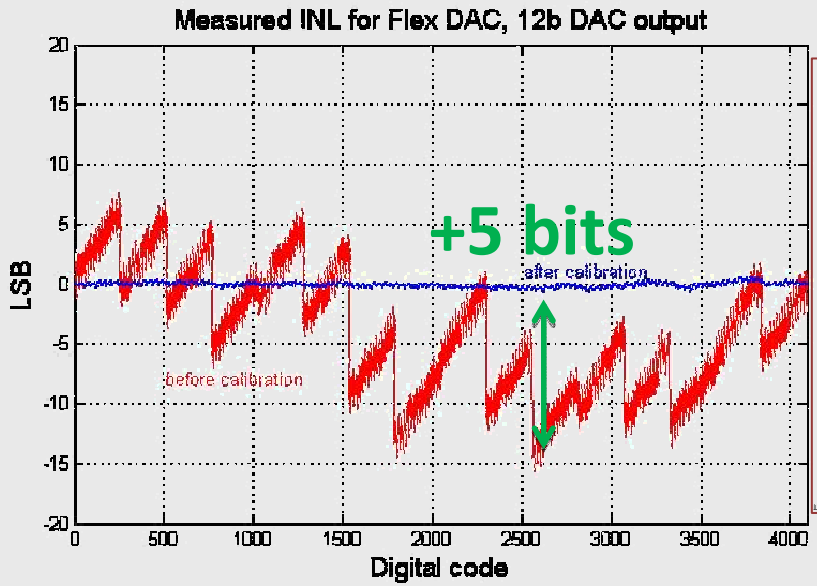


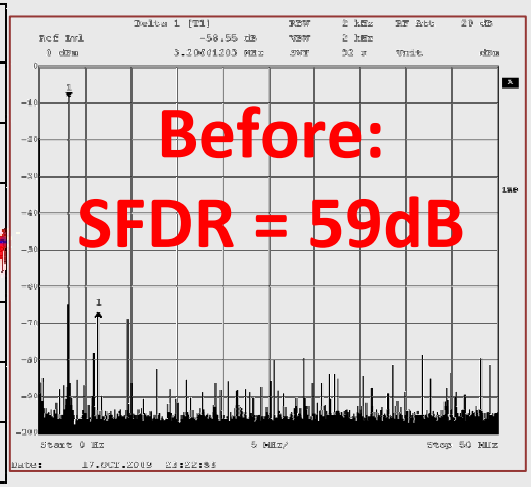

**Off-chip calibration engine;**

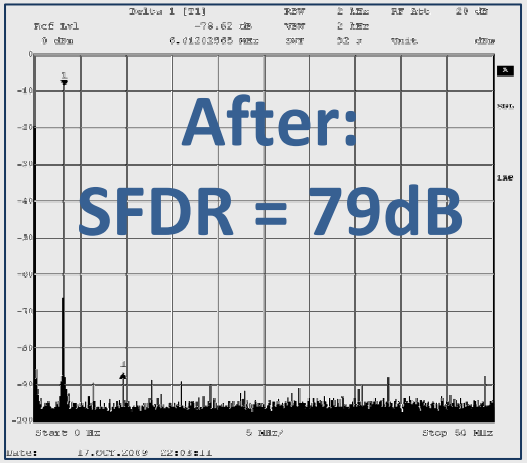
**Flexibility;**

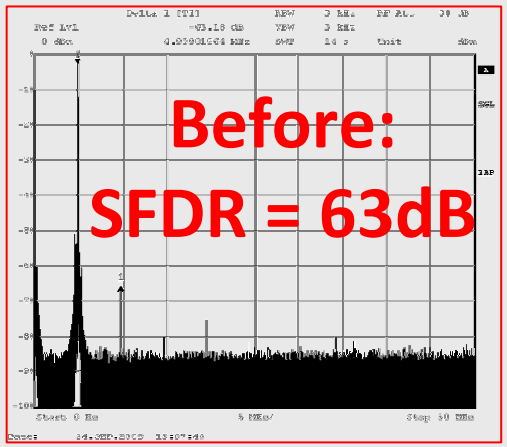
**0.047mm² per 12b sub-DAC (recall: 1mm² for 250nm; 0.2mm² for 180nm)**

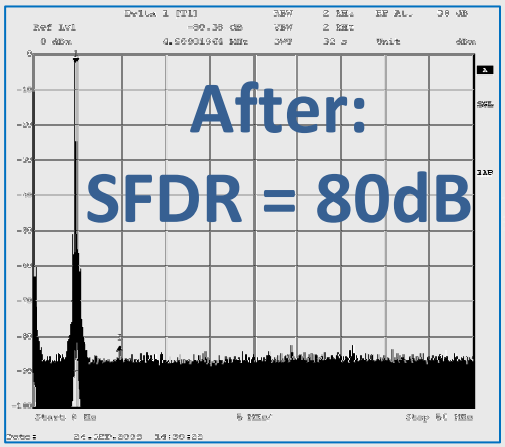
# Calibration of all DAC currents, INL & slow signals measurements

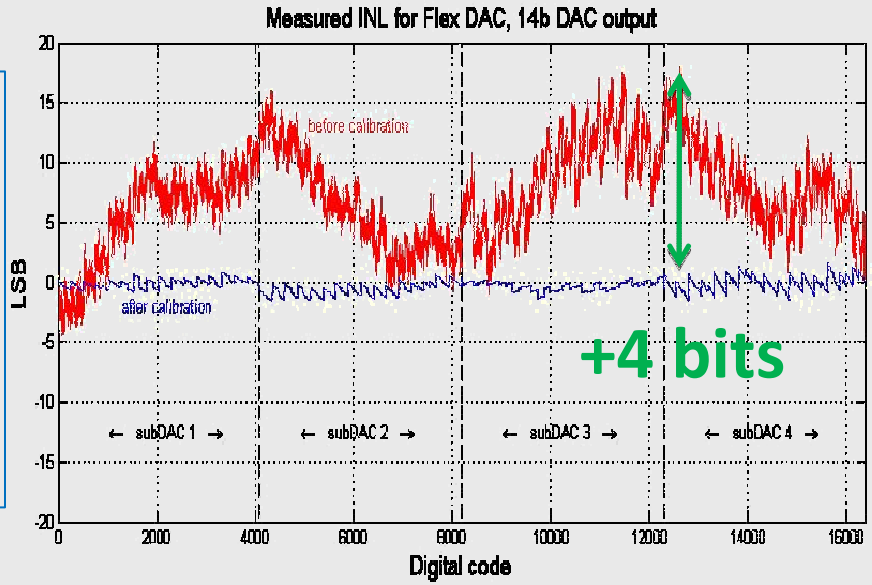


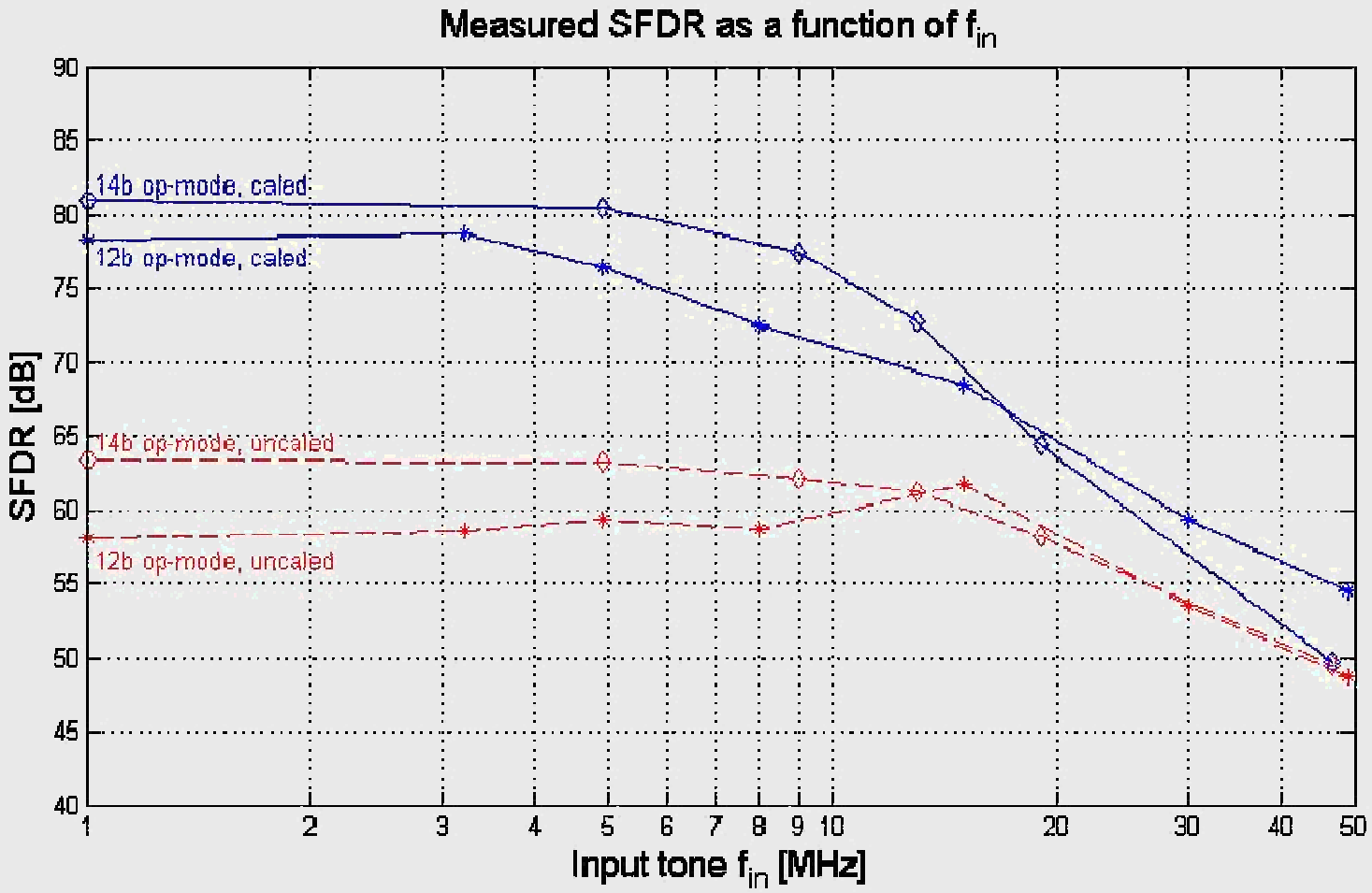



# Calibration of all DAC currents, dynamic measurements



# Conclusions

- **Calibration:**
  - improves performance;
  - relaxes design requirements;
  - reduces product risks;

- 3 **test-chip demonstrated:**
  - aggressive analog area reduction;
  - high current accuracy;
  - analog performance supported by digital.

## Acknowledgements

**Xilinx** Ireland, Mixed-Signal Design Group

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# Thanks for attention!

# Discussion