National
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Embedded Systems Network

Multi-Core/Multi-Processor Systems

Thursday 25th June 2009, Bourne End

National Microelectronics Institute

Building and Uniting a Strong Microelectronics Community

NMI Embedded Network Sponsors

LAUTERBACH
DEVELOPMENT TOOLS

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Thursday 25th June 2009, Bourne End

09:00 Registration
Refreshments, Networking & Sponsor Table-Tops

09:45 ***Welcome & Introduction***
Robin Kennedy, NMI
Jeremy Bennett, Embecosm (Chair)

Housekeeping

- In case of…
- Who to speak to…

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About the NMI

- A Not-for-Profit Organisation Funded Primarily from Membership
- Strong & Representative Board of Directors (left to right)
  - *David Burrows*, Chairman of NMI, Director, Aptina Imaging UK
  - *Derek Boyd*, CEO, National Microelectronics Institute
  - *Steve Neill*, Vice President, Bristol Design Centre and Technical Director, Infineon Technologies (UK) Ltd
  - *Hossein Yassaie*, CEO, Imagination Technologies
  - *Ivor Evans*, VP Product Engineering, CSR plc
  - Patrick McNamee, VP Supply Chain, Powervation
  - *Gerry Edwards*, Vice President & Managing Director, National Semiconductor (UK) Ltd
  - *Ron Dickinson*, Operations Director, Freescale Semiconductor
  - *Stuart Langdon*, European Facilities Director, International Rectifier
  - *Professor Anthony O'Neill*, Newcastle University
  - Advisor to the Board, Vince Osgood, EPSRC *(not pictured)*

Background

- Embedded
  - a vital part of microelectronics
- Multi-Core
  - embedded-europe.com; 24th June
  - **Parallel software plays catch-up with multicore**
    Microprocessors are marching into a multicore future to keep delivering performance gains without frying in their own heat. But mainstream software has yet to find its path to using the new parallelism.
  - **A real-time HPC approach for optimizing Intel multi-core architectures (Part 1 of 3)**
    In this three part series, the authors present findings that demonstrate how a novel approach with Intel hardware and software technology is allowing for real-time high-performance computing (HPC) in order to solve engineering problems with multi-core processors that were not possible only five years ago.
  - **Enea Optima upgrade eases analysis and debugging**
    Enea Optima 2.1 is an Eclipse-based integrated development environment providing enhanced system level debugging functionality for multicore and multi processor applications.

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Innovation Networks

- Innovation = Technical + Business
  - Listen and Contribute
- Network
  - TALK TO EACH OTHER
- Statistics
  - 70 registered attendees
  - 49 organisations represented (30 are NMI members)

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NMI Update

- NMI News at a Glance
  - register via www.nmi.org.uk
- Government Call to Action
  - Meeting with Minister at Department for Business, Innovation and Skills
- NMInet www.nminet.org
  - An open global forum
  - Complement our physical meetings

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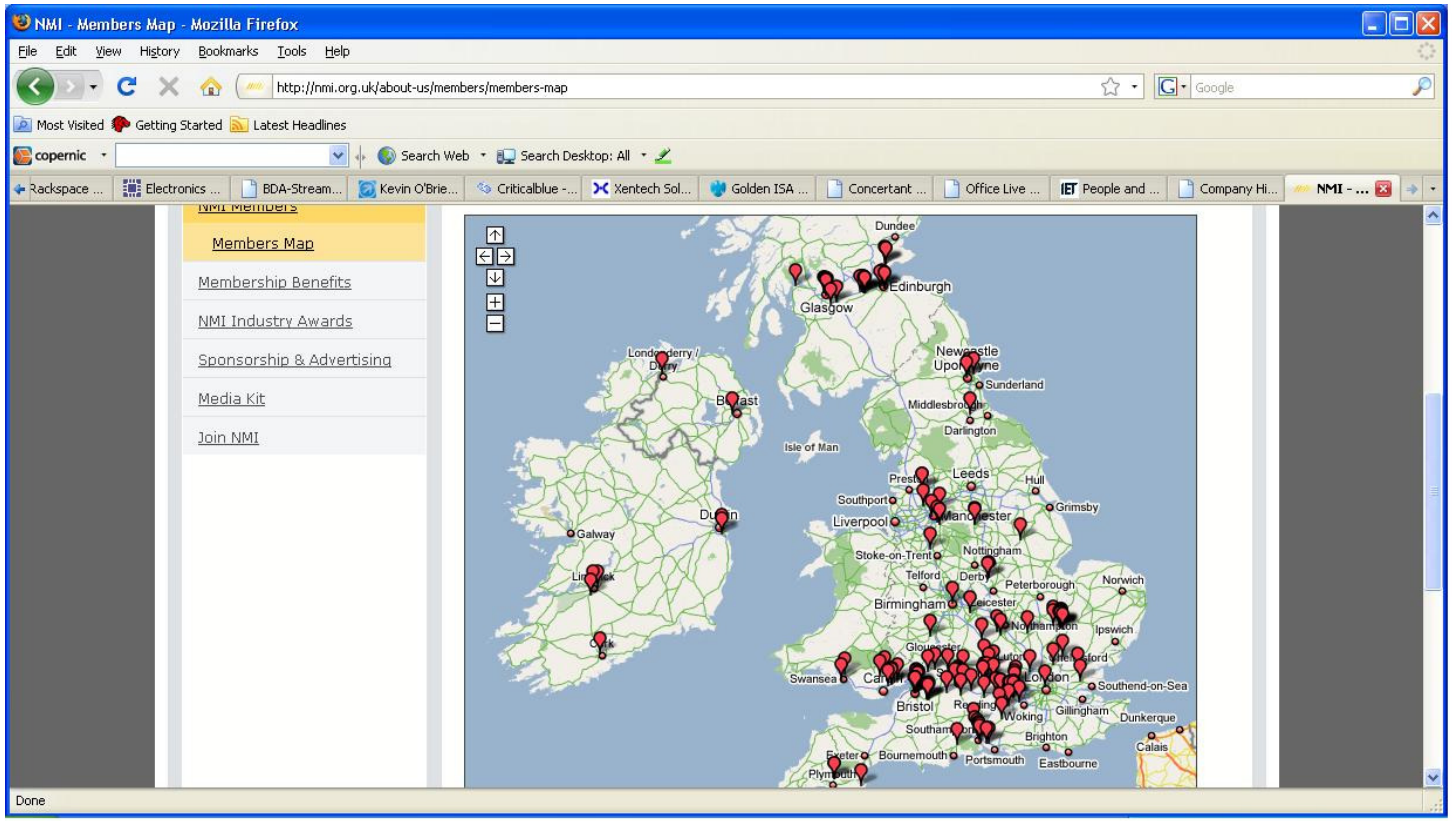
NMI Update

New Website

- members map
- events calendar
- members' area



NMI Update

- International Semiconductor Conference (ICCV 2009)
  - proceedings available

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ICCV 2009

Conference Agenda Day 1
12th May 2009

Theme: Designing for Variability (DfV) - Minimizing the impact of Variability in the Foundry

8:30am: Registration and Refreshments

Welcome & Introduction

tbc, Conference Opening Address

Paul Jarvie, National Microelectronics Institute, "Welcome to ICCV2009"

SESSION 1: The IDM & Fabless perspective

Key Note: Dr Kelin Kuhn ,Intel, "Variation in 45nm and implications for 32nm and beyond"

Krisztian Flautner, ARM , "Life on the Treadmill"

Professor Asen Asenov, University of Glasgow ,"Statistical variability and reliability in the next generation CMOS technologies and the ITRS response"

12:30pm: Buffet Lunch & Networking

SESSION 2: Embracing DfV in the Foundry

Key Note: Dr Sani Nassif, IBM, "Variability beyond 45nm countermeasures"

Davide Pandini , ST Microelectronics, "Statistical Static Timing Approach to Deal with Increased Process Variability in Advanced Technologies"

PANEL: Are we ready for DfV at sub 32nm ?

Chair : **Professor Asen Asenov**

17:00 Conference Close (DAY 1)

19:00~22:00 Conference Dinner : Savoy Place, London, UK ,

Conference Sponsors

Mentor Graphics

csr

cadence

SYNOPSYS

Key Note: **Dr Kelin Kuhn ,Intel,** "Variation in 45nm and implications for 32nm and beyond"

Conference Agenda Day 2
13th May 2009

Theme: Designing the chips of tomorrow with "Variability aware" Tools and flows

8:30am Registration and Refreshments

SESSION 1: Are EDA Tools ready for the era of Variability?

Key Note: Jean-Marie Brunet, Mentor Graphics, " Managing Variability in next generation design methodologies and tools "

Andrew Appleby, NXP Semiconductors, "Realising a 45nm System on Chip for digital TV in the age of variability"

Dr. Ahsan Bootehsaz , Synopsys, "tbc"

12:30pm Buffet Lunch & Networking

SESSION 2: Delivering Product Performance in the face of Variability

tbc , *PDF Solutions, "tbc"*

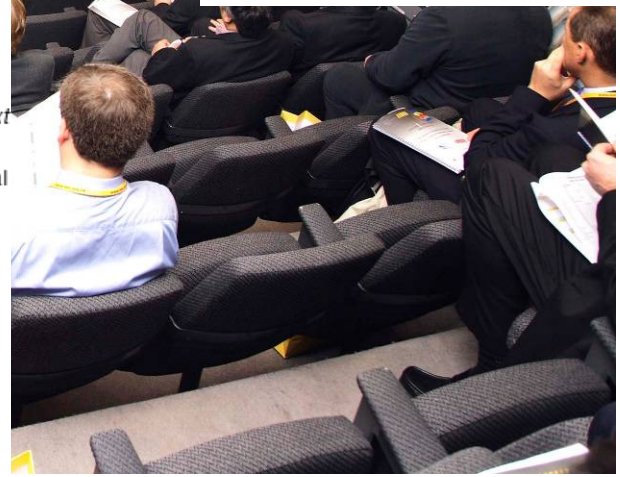
Jeff Watt, Altera, "Variability-Aware Product Development in a Fabless Environment"

Patric Drenan, SOLIDO, "Design for Variability in Analog / Mixed-Signal Circuits"

PANEL: "Are design tools variability aware ? "

Chair : Ian Phillips , ARM

16:00 Conference Close & Wrap up



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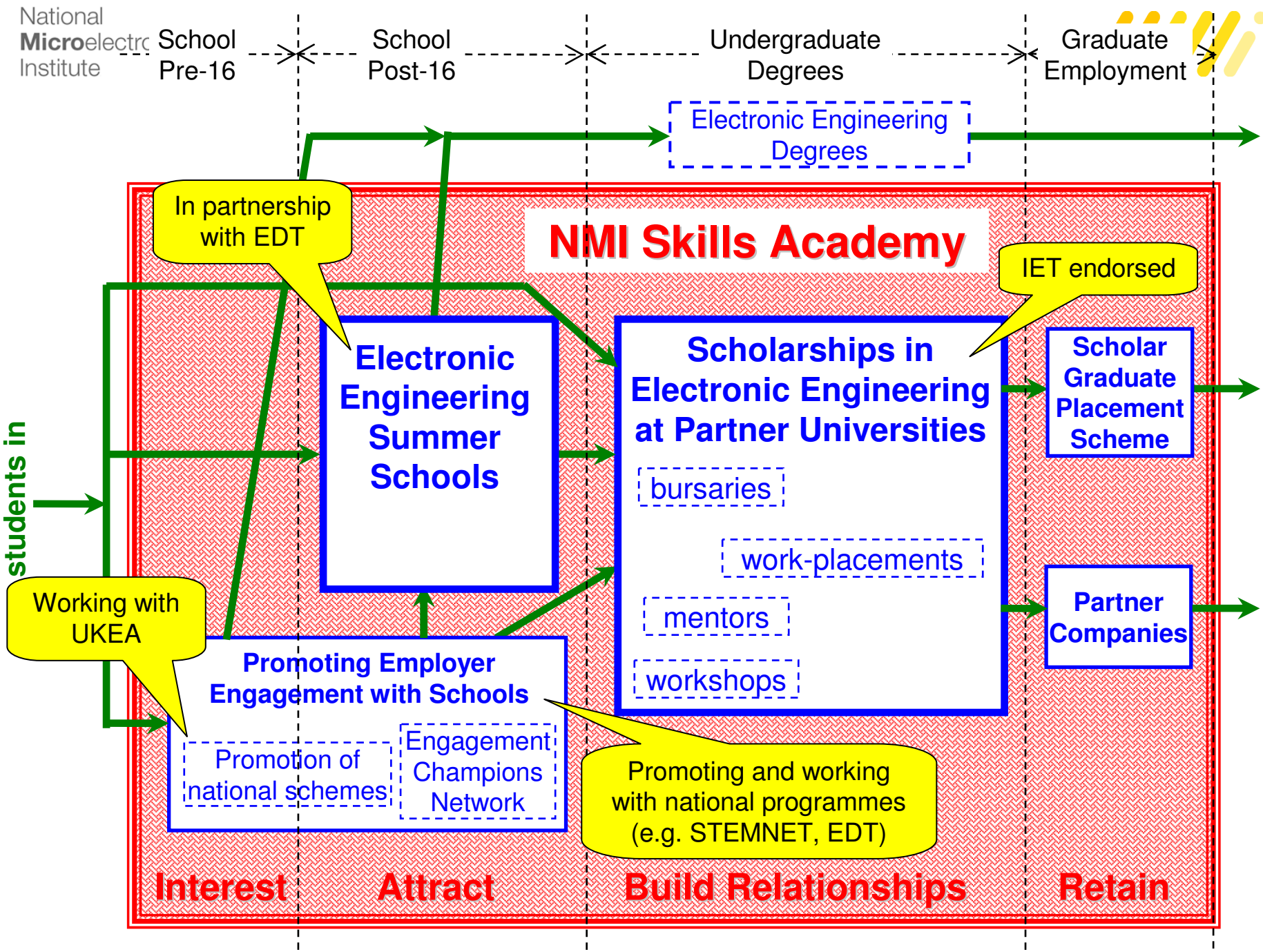
NMI Update

- Innovation Networks
  - Build on Technical Networks
  - Application Themes
  - Innovation Network Advisory Groups
- Network Events
  - Power “Low-Carbon” 8th September
  - System-Level Design 24th September
  - Analogue-Mixed Signal 22nd October
  - Design for Manufacture 12th November
- Annual **Awards** Dinner – 5th November, London
  - Award submissions
  - Sponsorship opportunities
- Skills Academy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School Pre-16
School Post-16
Undergraduate Degrees
Graduate Employment
Electronic Engineering Degrees
NMI Skills Academy
In partnership with EDT
IET endorsed
Electronic Engineering Summer Schools
Scholarships in Electronic Engineering at Partner Universities
bursaries
work-placements
mentors
workshops
Scholar Graduate Placement Scheme
Partner Companies
students in
Working with UKEA
Promoting Employer Engagement with Schools
Promotion of national schemes
Engagement Champions Network
Promoting and working with national programmes (e.g. STEMNET, EDT)
Interest
Attract
Build Relationships
Retain

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Academy Development

- Steering Group
  - 5 leading UK universities in Electronics Engineering
  - Companies in Microelectronics sector with a UK presence

University of BRISTOL
Imperial College London
University of Southampton
UNIVERSITY OF SURREY
ARM
from software to silicon EDA SOLUTIONS
FUJITSU
Imagination TECHNOLOGIES

- Consultation with Public Sector Groups
  - ESSG, SEMTA and BERR
- Attract support from more companies once programme agreed and funding model established
- Extend to other leading universities once viability and impact of Academy demonstrated

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Embedded Update

- Elsevier
  - content needed
- Perforce podcast
  - invite members of the NMI to record a panel discussion on current themes in embedded software development.
- ESC, Farnborough 6-8 October
  - panel session
- See me if you want to know more or take part

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Thank you to our Network Sponsor

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And our hosts

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09:00 Registration
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09:45 ***Welcome & Introduction***
Robin Kennedy, NMI

"Fifteen Years in Multi-Core Systems"
Andy Lunness, STMicroelectronics

"Surviving a Multicore Development Project"
Barry Lock, Lauterbach

11:00 -11:30 Break

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"Multi-Core, Multi-threaded, Multi-standard: Using architecture to maximise IP product scalability"
Tony King-Smith, Imagination Technologies

"Multicore System Architecture - from the Software Perspective"
Paul Tingey, Wind River

12:30 – 14:00 Lunch & Networking

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"What Do Embedded Software Developers Really Think About Multicore Architectures?"
David Stewart, Critical Blue

"Systems Knowledge at a Premium"
Joe Brennan, Renesas

"Evolution of Protocol Aware Exercisers using multi-threaded techniques"
Matthew Dunn, LeCroy

16:00 Close Refreshments & Continued Networking

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Thank you for attending

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