Evolution of Protocol Aware Tools using multi-threaded techniques

Matthew Dunn
LeCroy PSG
EMEA technical Manager

Confidential

Agenda

- Introduction
- Background on bus testing tools
- The move to serial bus
- Evolution of tools to assist serial bus development
- Complexities of serial bus
- Advantages offered using multiple threads and multiple cores in T&M toolsets

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Introduction

- LeCroy is a leading provider of Oscilloscopes, Protocol analysers and related test and measurement
- founded in 1964
- T&M tools to improve productivity by resolving design issues faster and more effectively.
- Specialised in analysing serial data streams
- Headquartered in Chestnut Ridge, New York, LeCroy
  - sales, service and development subsidiaries in the US and throughout Europe and Asia

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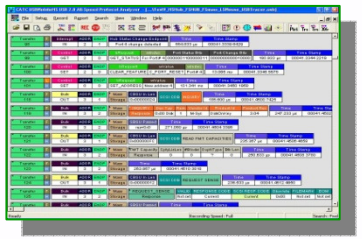
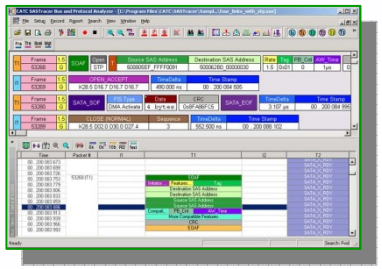
Tools for Bus testing

- Any Electrical Bus
  - Scope used to verify electrical signal shape
    - Typical issues: noise, cross talk, reflections, driver problems
- Parallel bus
  - Used Logic Analyzer to examine bus skew and state of sideband (control) signals
    - Typical issues: skew, line shorts, line open
  - Use Protocol Analyser at application level
    - Typical issues: flow control, timeouts, memory control, protocol over a transport
- Serial bus
  - Use protocol Analyser
    - Typical issues: arbitration, scrambling, coding, flow control, timeouts, messaging





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Where digital test tools started

- Scopes
  - Analogue, sampling, real time...
  - 1-4 channels
  - Great for wave shape, parametric
    - Peak to peak voltage, rise time, arrival time etc.
  - not so easy to understand digital content
    - Can often be done with a good toolbox to some degree on more powerful systems
  - Real time Pattern Filtering isn't really practical
  - Triggering usually limited to edge or base patterns only

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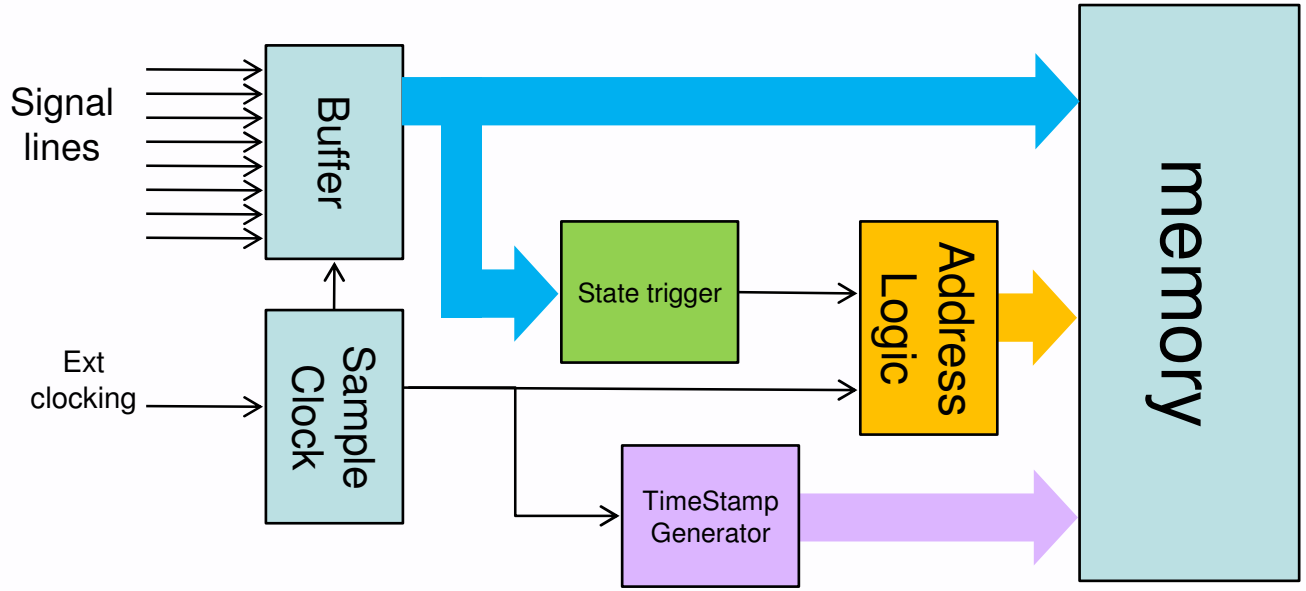
Where digital test tools started

- Logic Analyser approach
  - Developed from the need to see more signals than a scope could show
  - simplified logical view of signal (analogue scope era)
  - Basically an n-wide buffer clocked into memory at regular intervals



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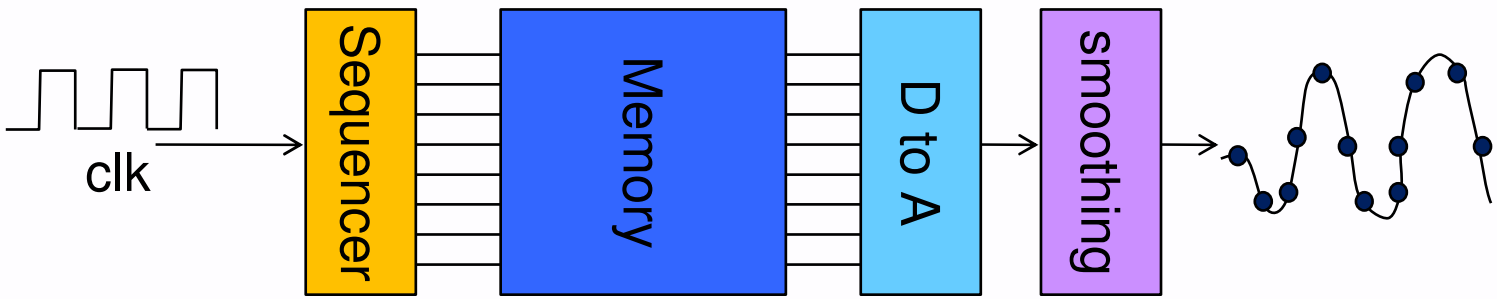
Exercising the bus

- Arbitrary Waveform Generators (AWG)
  - Basically some memory linked to a D/A convertor
  - flexible
  - Hard to program
    - Requires knowledge of the waveform
      - Voltage level, rise/fall times
  - No intelligence
  - Comparatively short exercise time



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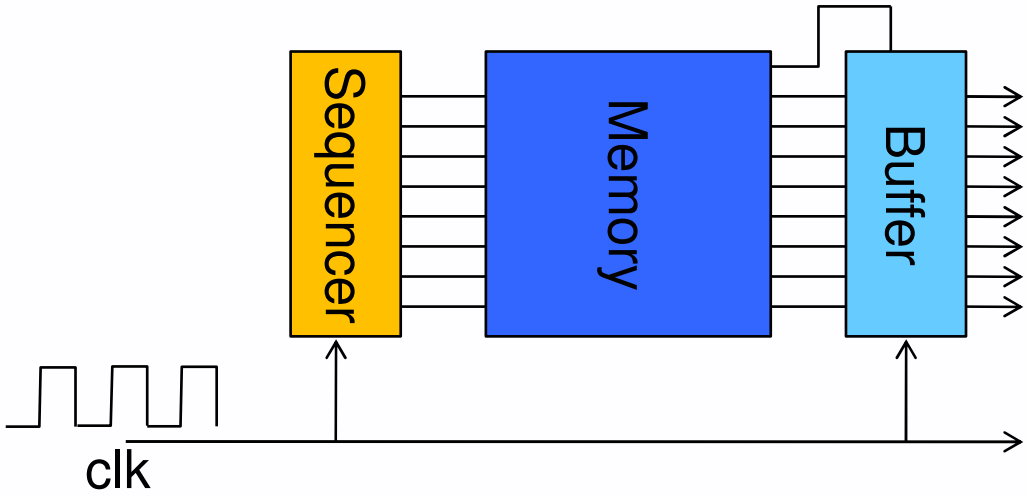
Exercising the bus

- Bit Blaster
  - Basically some memory linked to a Buffer
  - Easier to program than an AWG
  - No intelligence
  - Every bit time must be programmed



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The Parallel Bus Speed Limit

- Parallel busses are not good over ‘long’ distances.
  - Wire to wire signal skew and transmission line effects sample window
  - Data must be stable when clock/strobe arrives
- Busses are often multiplexed to reduce wires
- Error detection minimal or none
- Most embedded busses have a physical limit of 300-500MHz data rate
  - PCI-X 533MHZ, SCSI-320MHz, Printer Port 12MHZ, Memory 200-400(800)MHz
- Its isn't always possible to go ‘more parallel’ to work with a slower clock and gain bandwidth

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Parallel Buses Moving to Serial

- Parallel Port
  - 25pin 10MB/s
- Parallel ATA
  - 100-133MB/s
  - 40-80wire cable
- Parallel SCSI
  - U320 – 320MB/s –
  - 68wire cable
- Parallel PCI / PCI-X
  - 133MB/s-1GB/s
  - 92conductors

- USB2.0 Port
  - 4pin 40MB/s
- Serial ATA (7Pins)
  - 150MB/s -> 300MB/s
  - 7 wire cable
- Serial Attached SCSI
  - 300MB/s
  - 7 wire cable
- PCI-Express
  - 250MB/s-4GB/s
  - 4-64conductors

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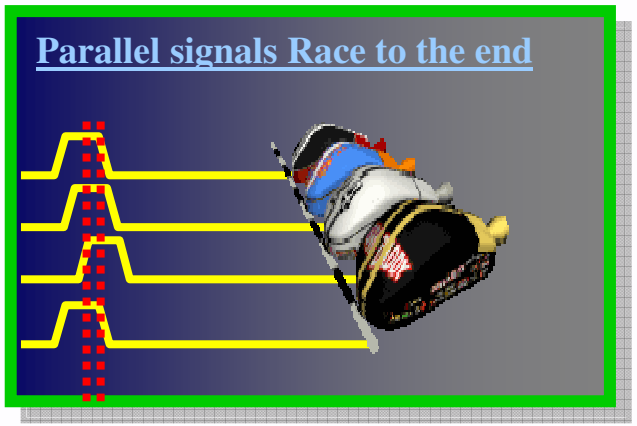
Why go Serial?

Advantages:

- A serial connection takes up less space.
  - Fewer wires means less pins needed ,Saves I/O Pads, Easier to layout
- Easier to isolate from its surroundings.
  - Not having multiple conductors in close proximity switching at the same time, means less crosstalk at higher frequencies.
- Speed
  - Higher bus speeds easier to achieve with fewer wires
  - skew between the different channels is not an issue.
  - No Parallel signals Race
    - Therefore can go faster
- Distance
  - Asynchronous serial transmission can be reliably sent great distances
- Power
  - Fewer wires to 'drive' means less power

Dis-advantages:

- Conversion required
  - Parallel – serial / serial - parallel



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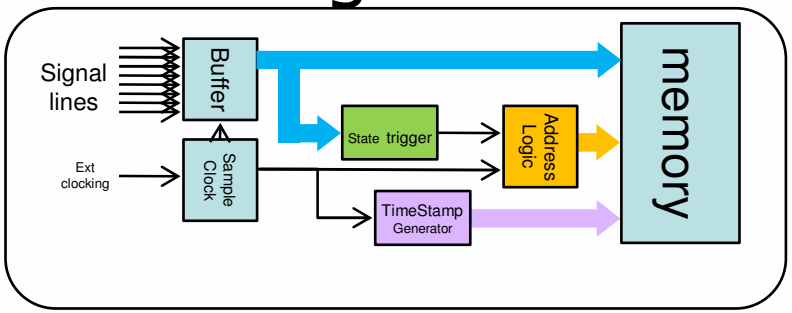
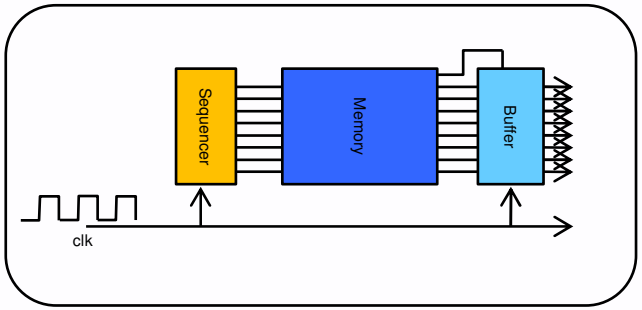
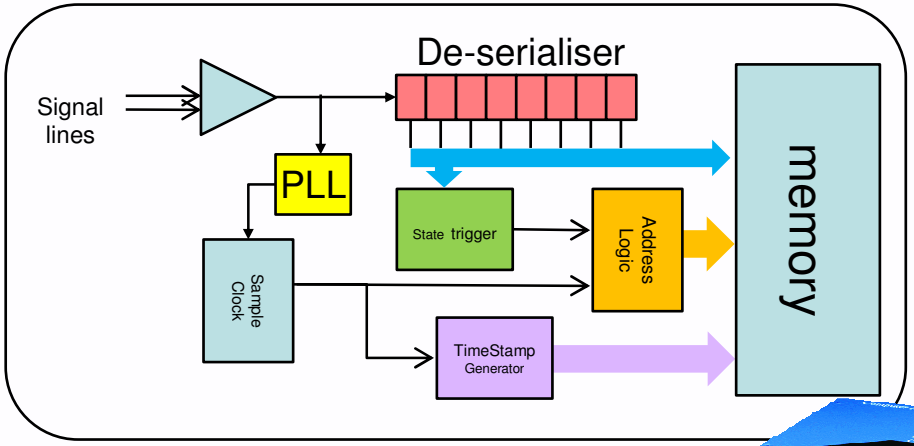
Toolset Change #1

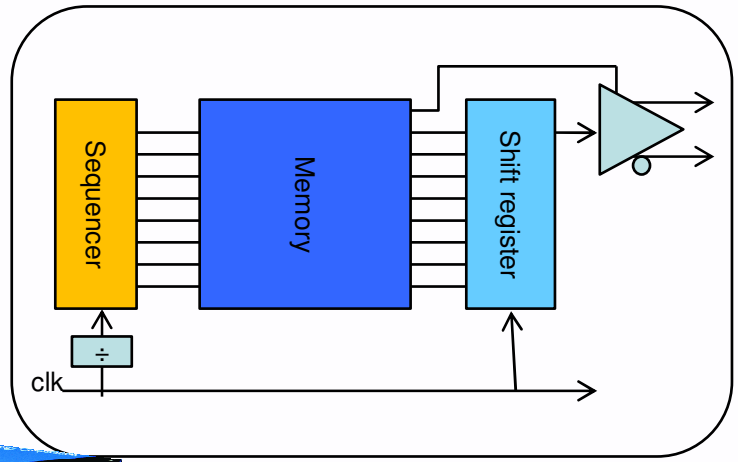
- 128 single ended channels?





- 1 differential channel





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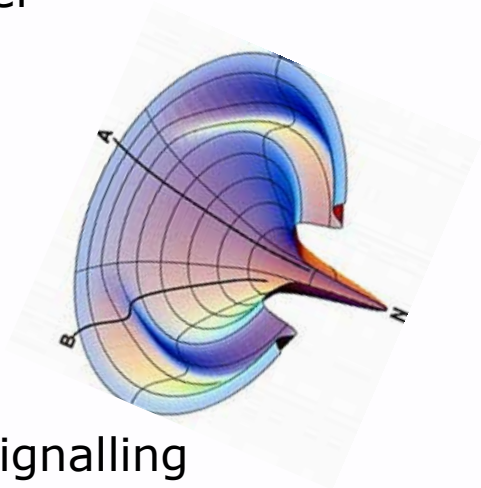
Serial bus Complexities

- Flow control
  - no side band/HW flow control, requires messages
- Routing/Addressing
  - In-band
- Error protection
  - Usually multi-bit error detection at physical level
  - Additional protection for routed data
- Interrupts
  - No wires, use messaging
- Clocks
  - Embedded in data, recovered by receiver
  - Multi-segment paths require buffer elasticity
- EMI avoidance
  - Continuous signalling, scrambling, differential signalling
- Event queuing/posting
  - Increase efficiency of available bandwidth



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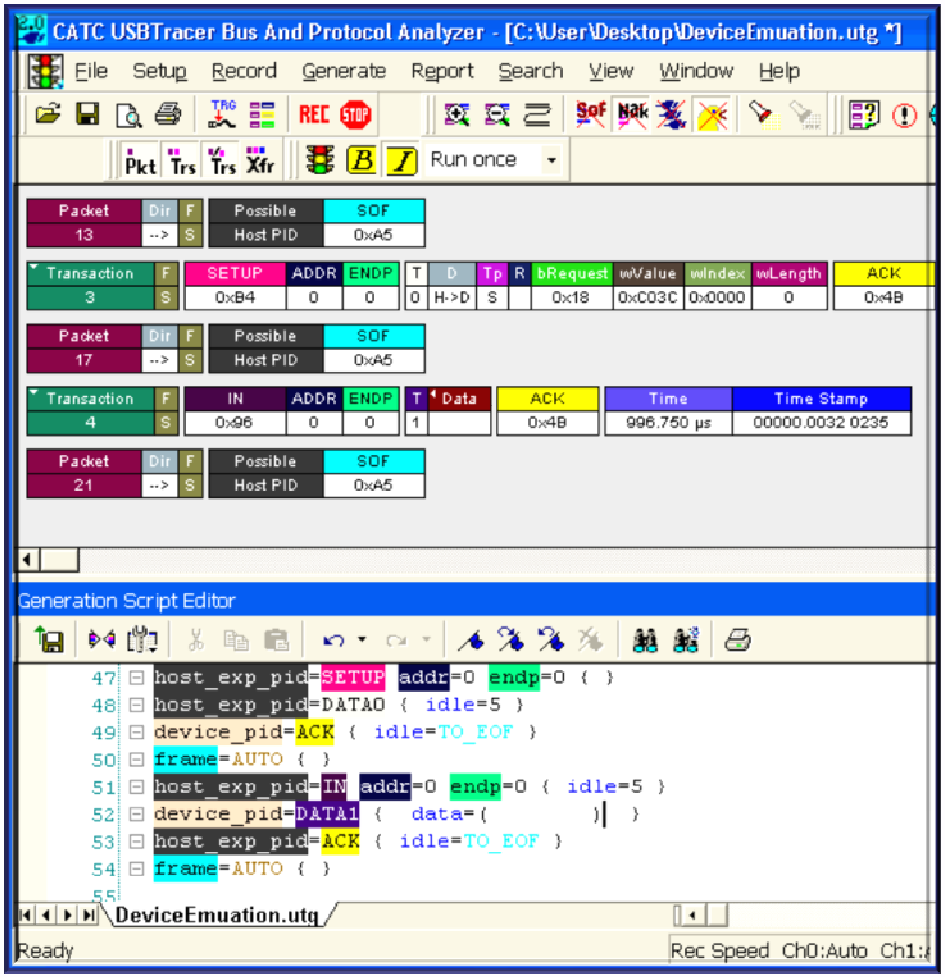
Toolset Changes #2

- To allow for 'variable' flow control and routing a more intelligent model may be needed.
  - state flow over timing reproduction
- In a multi-device bus an exerciser needs to know where it has been allocated
  - Address/WWN/Bus number



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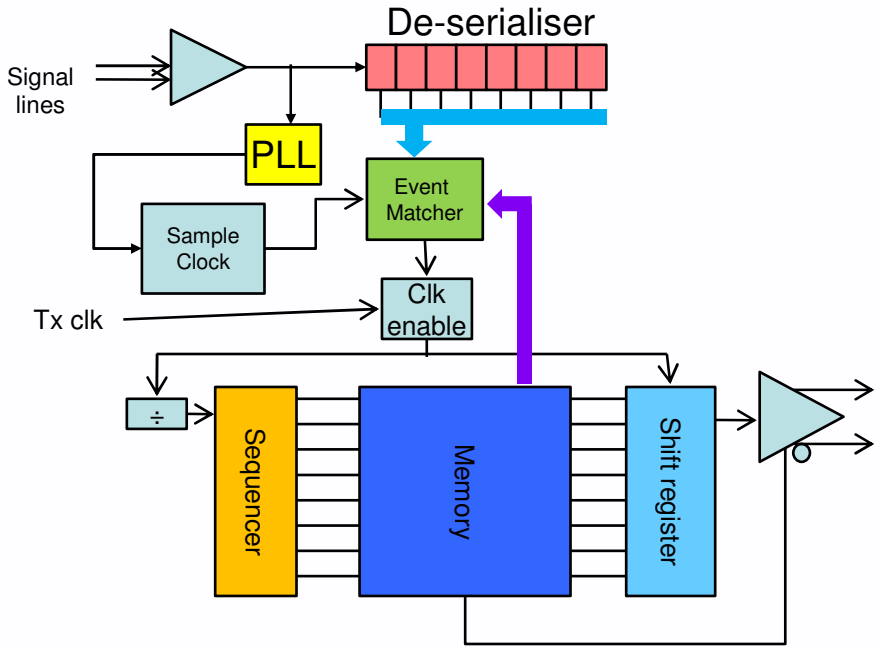
Toolset evolution #2

- Bit Blaster evolves in to protocol 'event' aware exerciser
  - Trade-off fine control of timing to support flow control and longer programs



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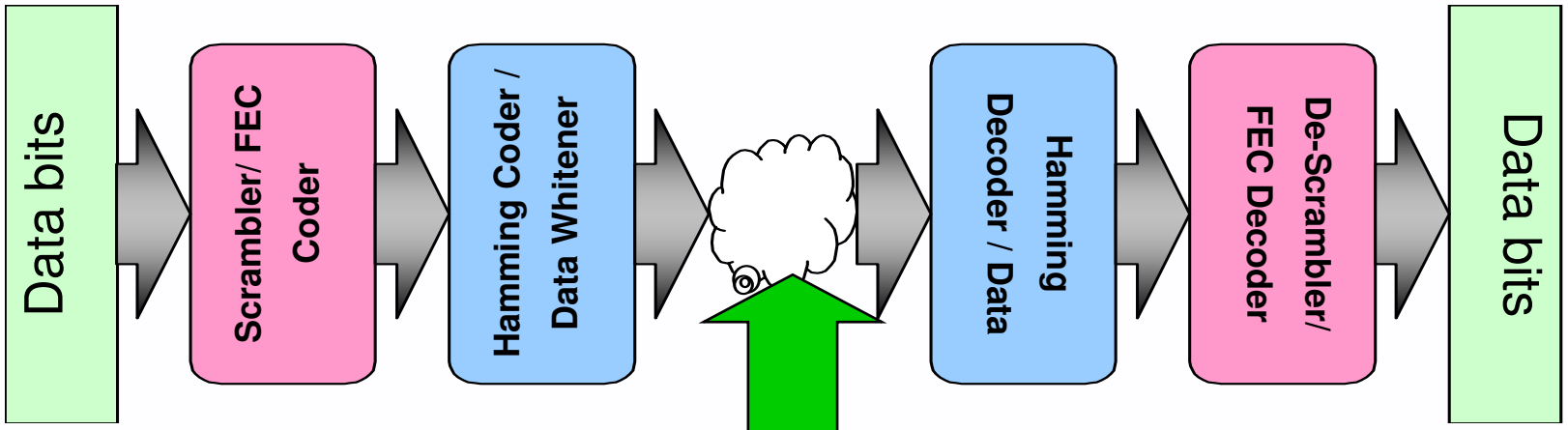
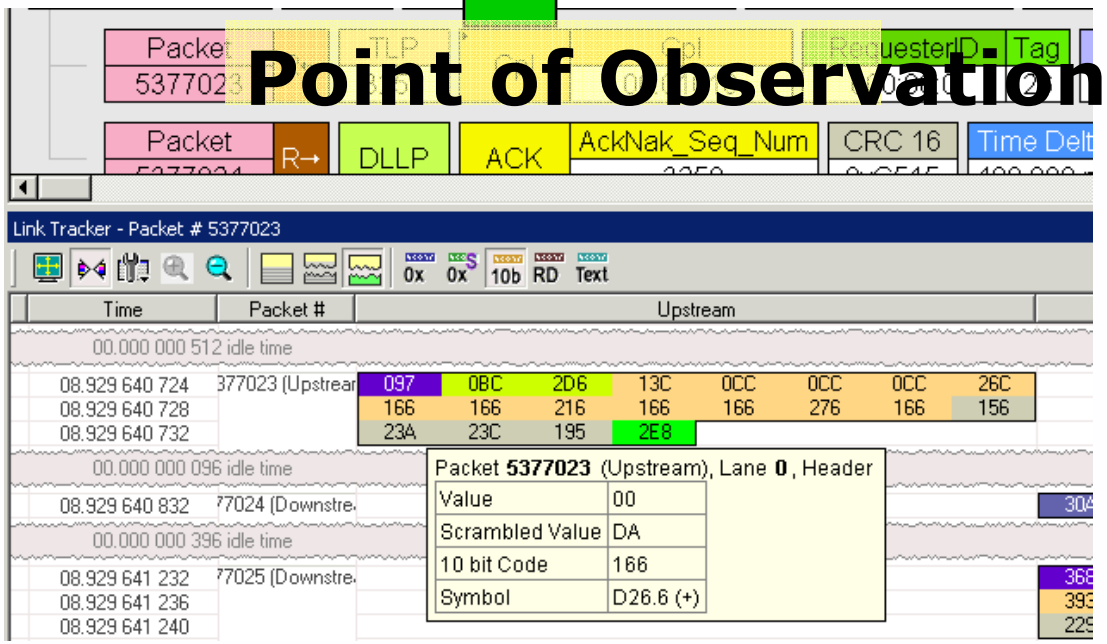
Typical effect of combined complexity





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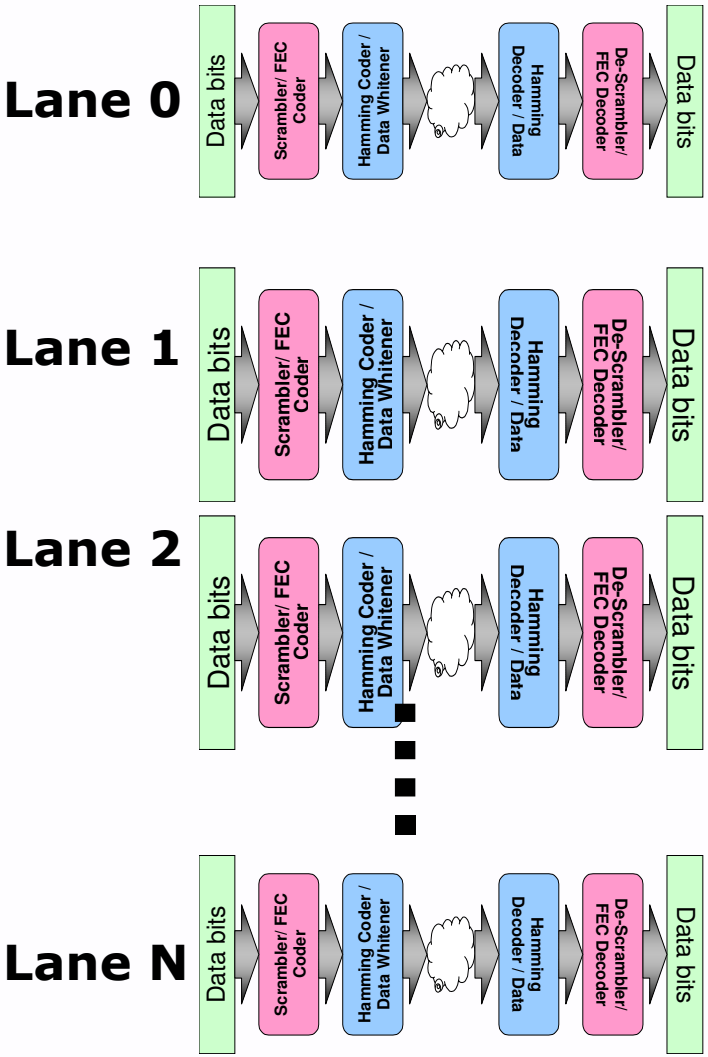
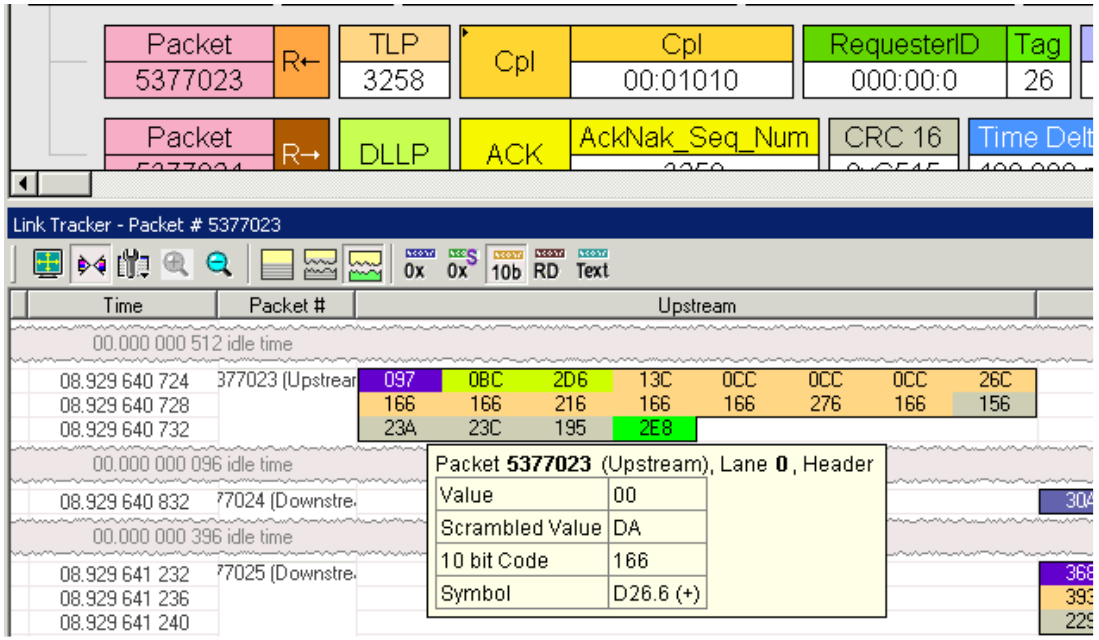
More Lanes…



- Bandwidth
  - increased by multiple asynchronous serial streams in parallel
- Scrambled, encoded and then:
  - Striped (PCI-E)
  - Independent (SAS)



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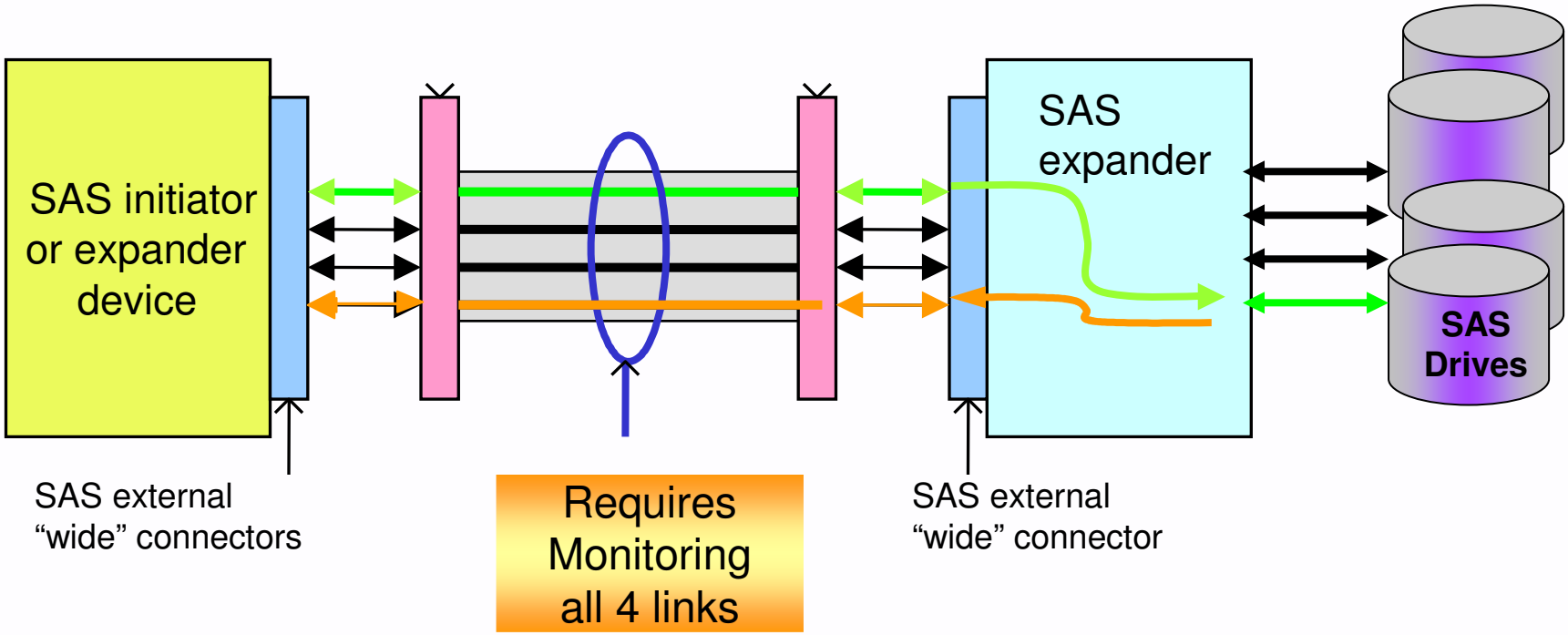
Supporting SAS "wide" Environment

SAS "wide" links with Expanders can dynamically use multiple "pathways" to complete a single operation



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Example Wide Port Transfer

I4	SCSI Operation 729	1.5 G	Initiator SAS Address 50006280_00000024	Target SAS Address 50001075_40000001	Tag 0x0054	SCSI LUN 0000 0000 0000 0000	SCSI CDB READ(10)				
I4	Transaction 17969	1.5 G	SSP	COMMAND	Tag 0x0054	IU	SCSI LUN 0000 0000 0000 0000	SCSI CDB READ(10)	Result ACK	TimeDelta 159.982 ms	
T2	Transaction 19340	1.5 G	SSP	DATA	Tag 0x0054	Data 1024 bytes	Result ACK	TimeDelta 7.760 µs	Time Stamp 02.100 279 212		
T2	Transaction 19342	1.5 G	SSP	DATA	Tag 0x0054	Data 1024 bytes	Result ACK	TimeDelta 8.238 µs	Time Stamp 02.100 286 972		
T2	Transaction 19344	1.5 G	SSP	DATA	Tag 0x0054	Data 1024 bytes	Result ACK	TimeDelta 14.113 µs	Time Stamp 02.100 295 210		
T2	Transaction 19346	1.5 G	SSP	DATA	Tag 0x0054	Data 1024 bytes	Result ACK	TimeDelta 15.703 µs	Time Stamp 02.100 309 322		
T2	Transaction 19348	1.5 G	SSP	DATA	Tag 0x0054	Data 1024 bytes	Result ACK	TimeDelta 13.498 µs	Time Stamp 02.100 325 025		
T2	Transaction 19350	1.5				Data	Result ACK	TimeDelta 7.305 µs	Time Stamp 02.100 338 522		
T2							Result CK	TimeDelta 16.372 µs	Time Stamp 02.100 345 827		
T2	19354						Result ACK	TimeDelta -157.147 ms	Time Stamp 02.100 362 200		
I4	SCSI Operation 731	1.5 G	Initiator SAS Address 50006280_00000024	Target SAS Address 50001075_40000001	Tag 0x0039	SCSI LUN 0000 0000 0000 0000	SCSI CDB READ(10)				

Command sent down one link; may return data on another

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Link training

- Most links support multiple speeds and power states
  - Speed negotiation can be by 'trying' different speeds at specific times after an event (eg SAS)
  - Speed negotiation can be based on an initial default speed which is then switched to a higher speed if mutually agreed (eg PCI Express)
- Low power modes
  - Normal operating, reduced power, sleep
    - State tracking
    - Wake up time

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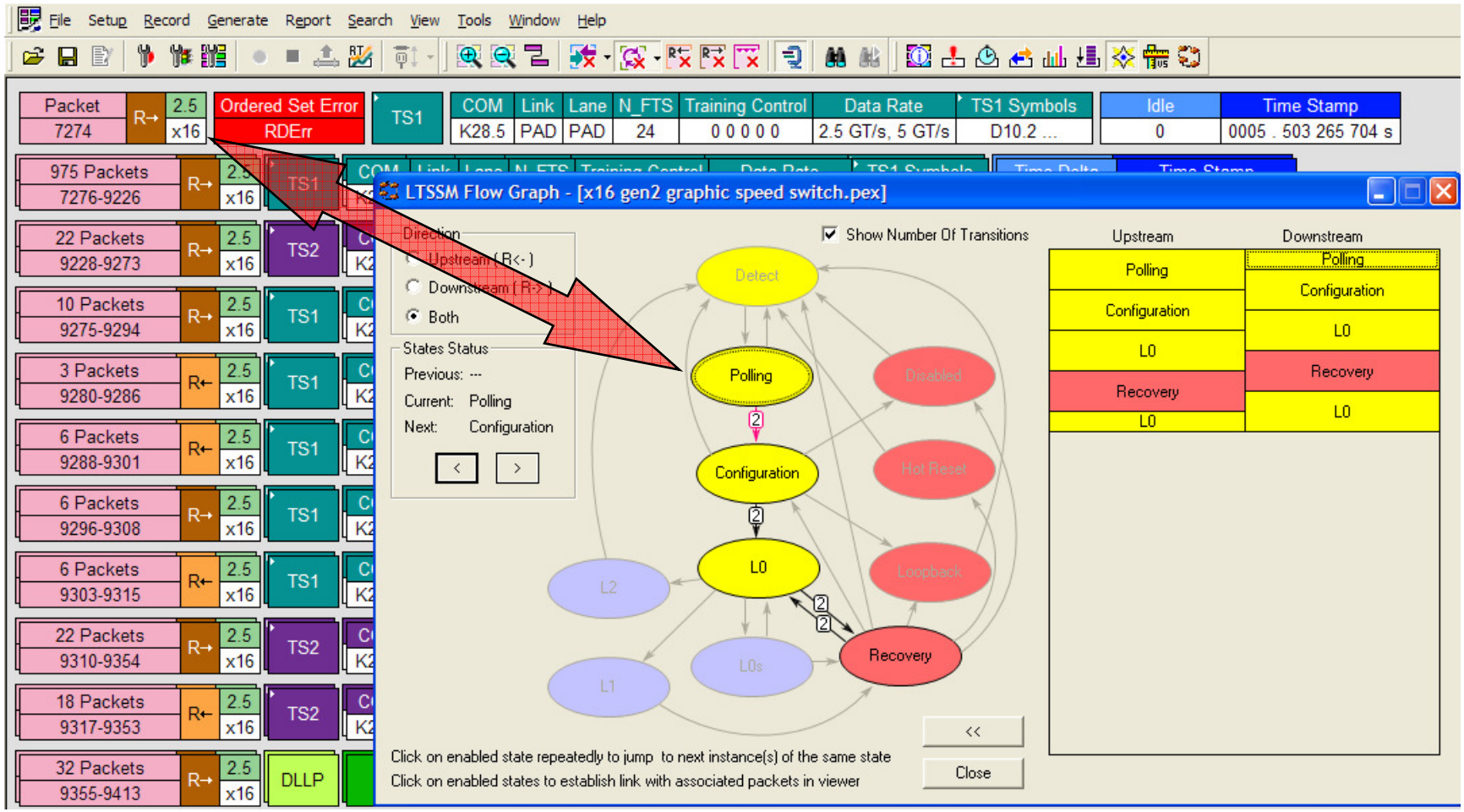
Low Power and State Flow



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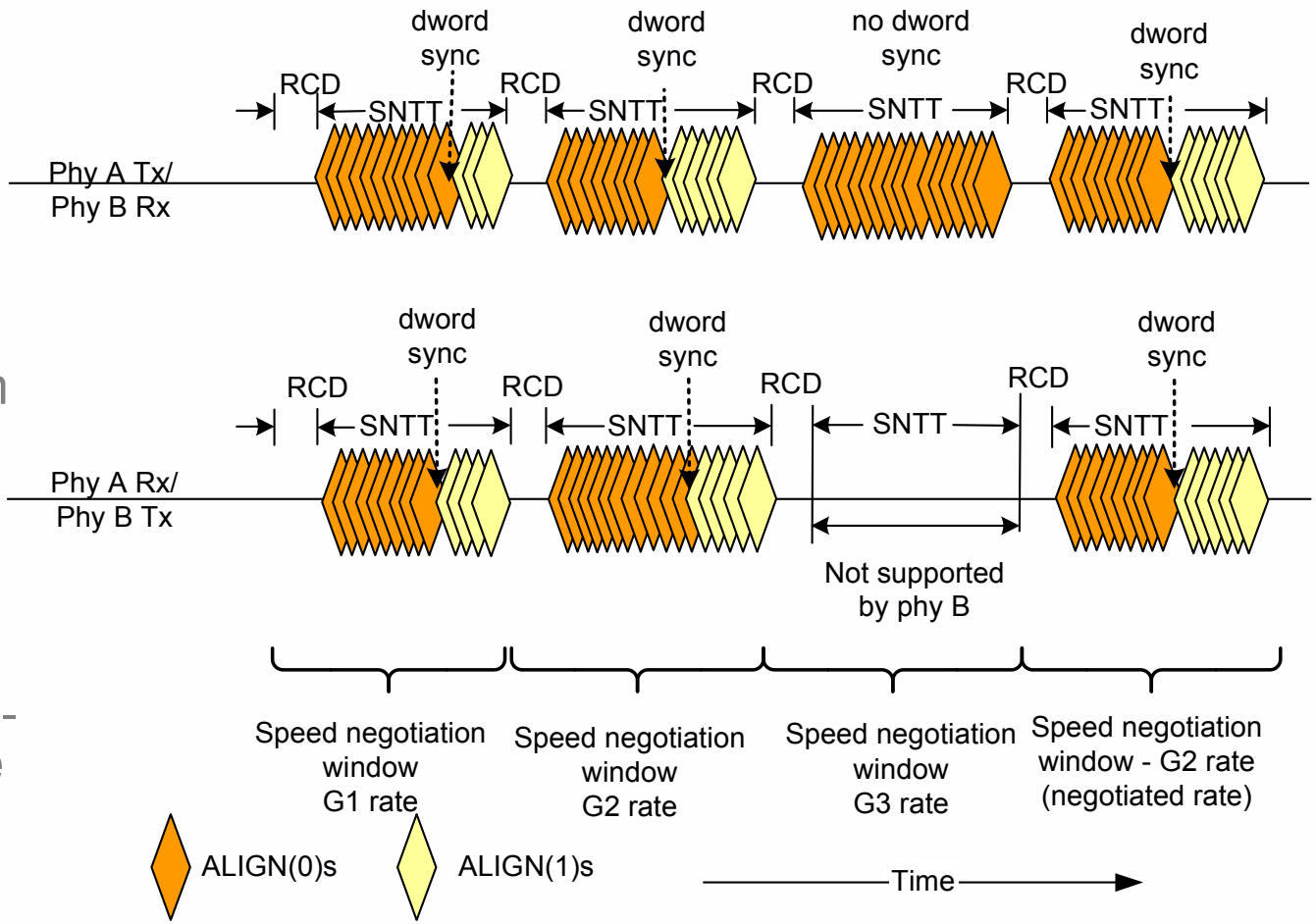
SAS speed negotiation

- Slow-to-fast
- Both phys run same set of speed negotiation windows
- 1.5, then 3.0, then 6.0 (if needed), etc. until they find:
  - a supported rate; then
  - a (faster) non-supported rate
- Last window returns to the highest supported rate detected



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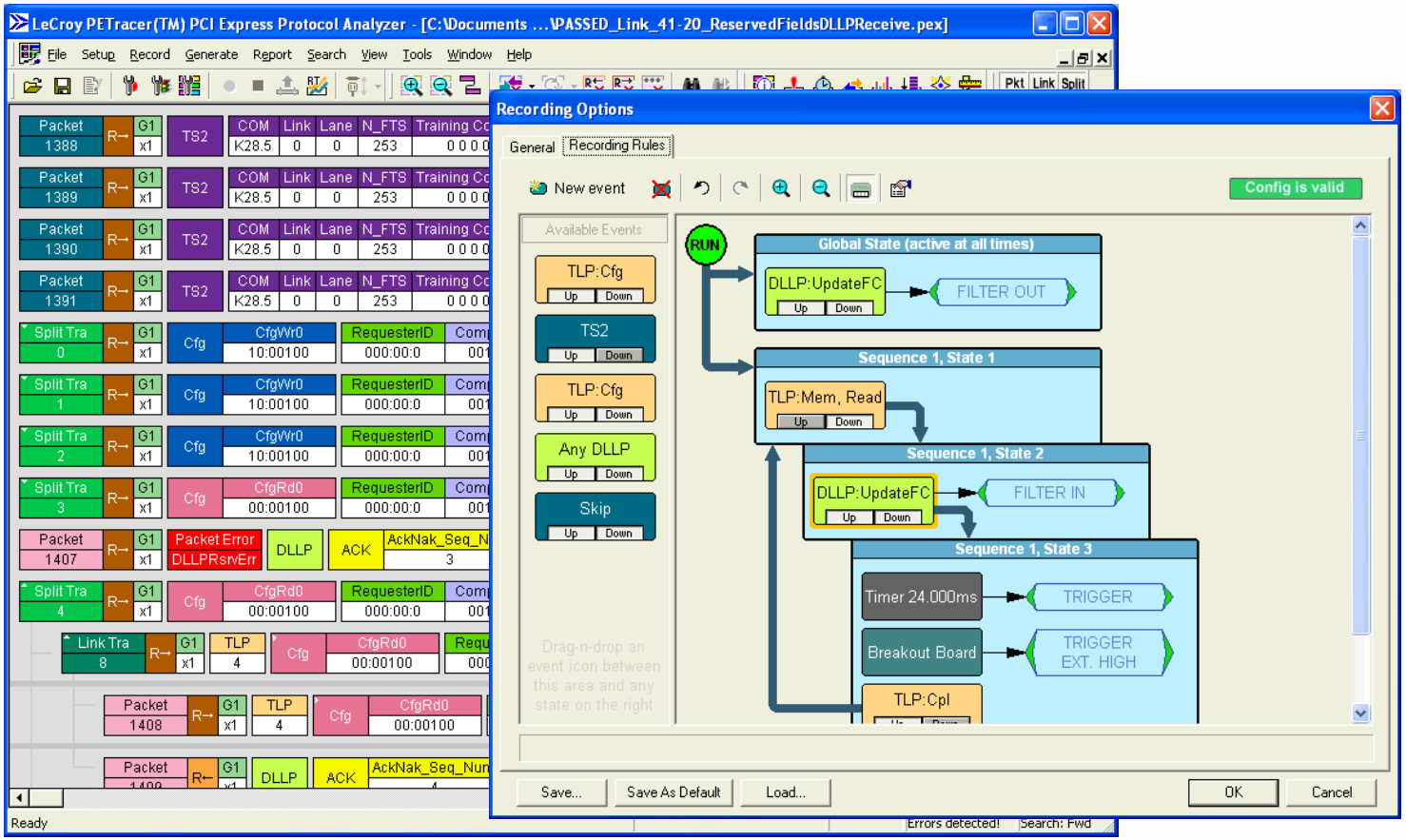
Trigger and filter threads

User interface hides thread to thread communication



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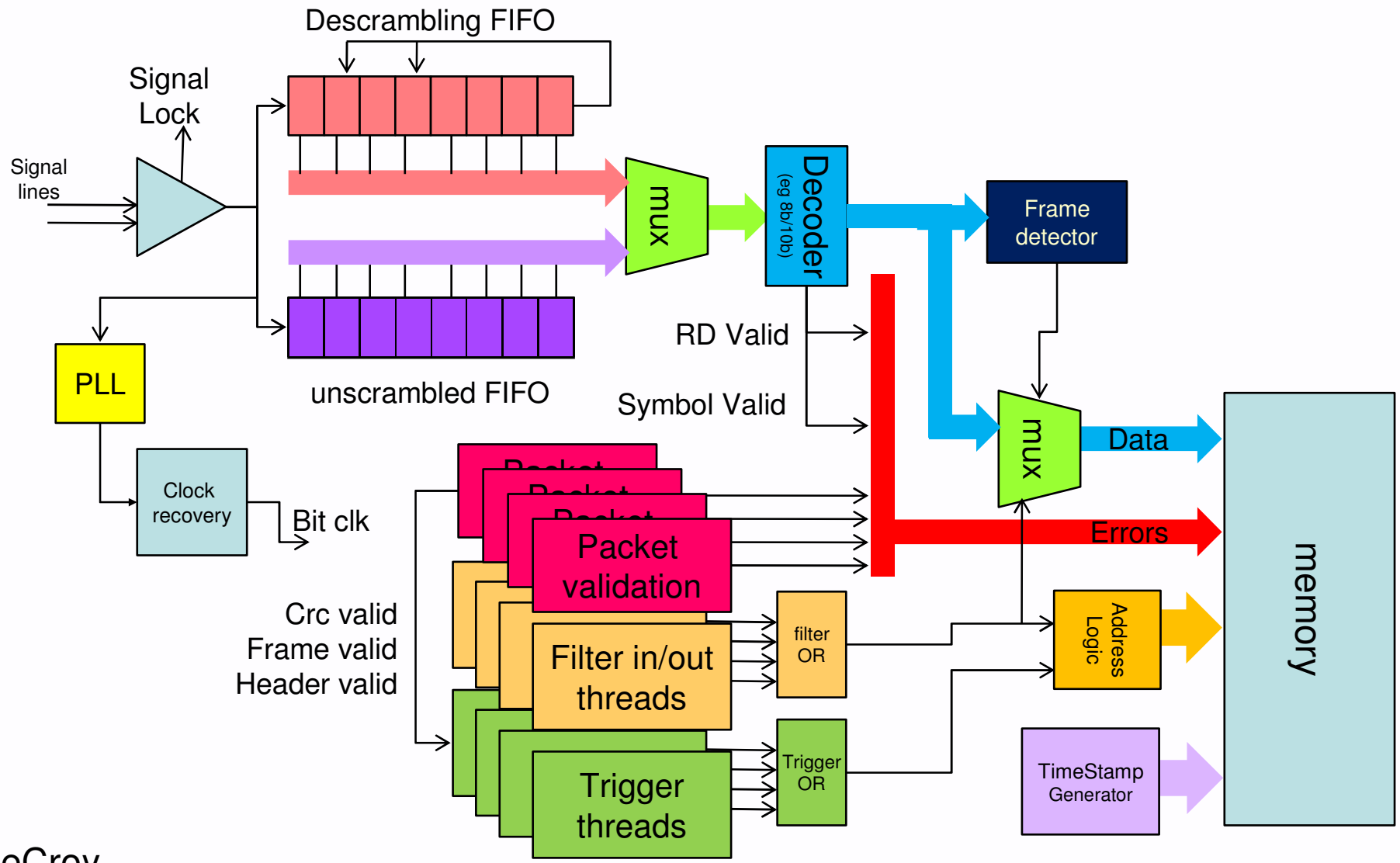
Advanced protocol model 1PHY



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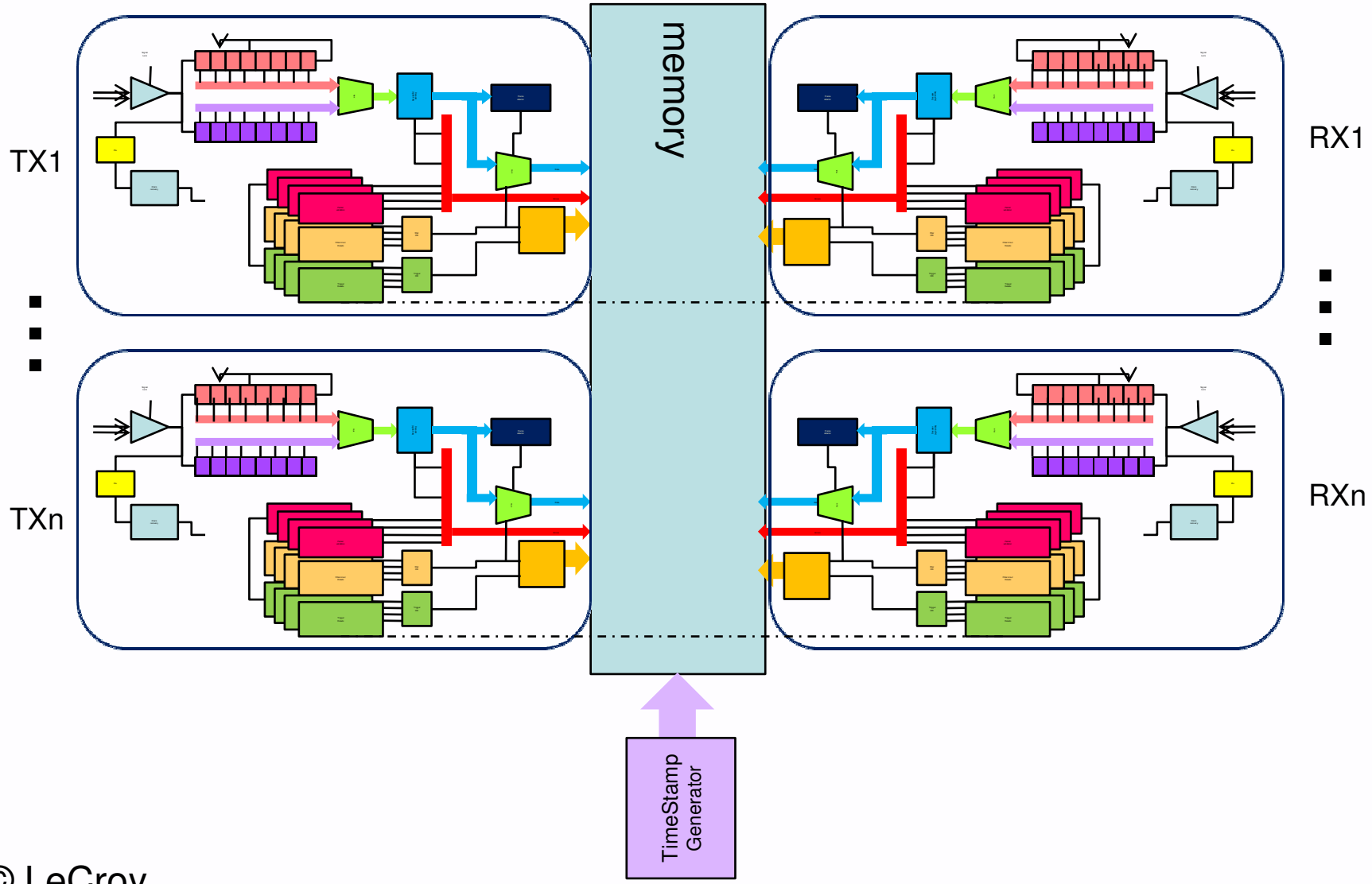
General multi core multi channel solution



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Other applications of method

- Jamming
  - Need to watch traffic in both directions
  - Keep track of multiple state machines
  - Make modification before leaving the box
    - Modification direction has a latency
      - Special handling of handshakes
  - Typically one core per PHY pair
  - Cores synchronised via messaging loop

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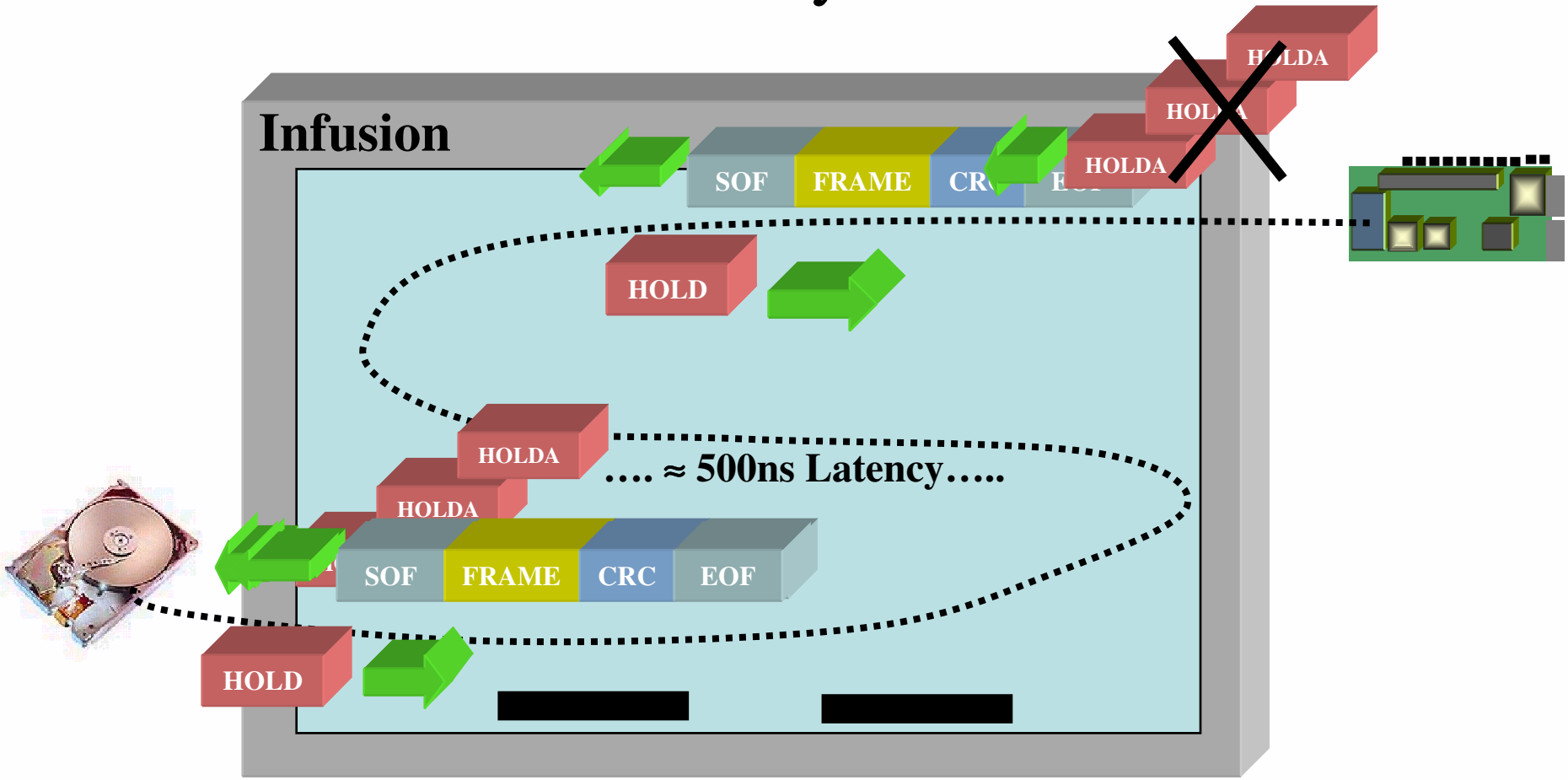
Hold handling threads

SATA HOLD/HOLDA – sync to main thread



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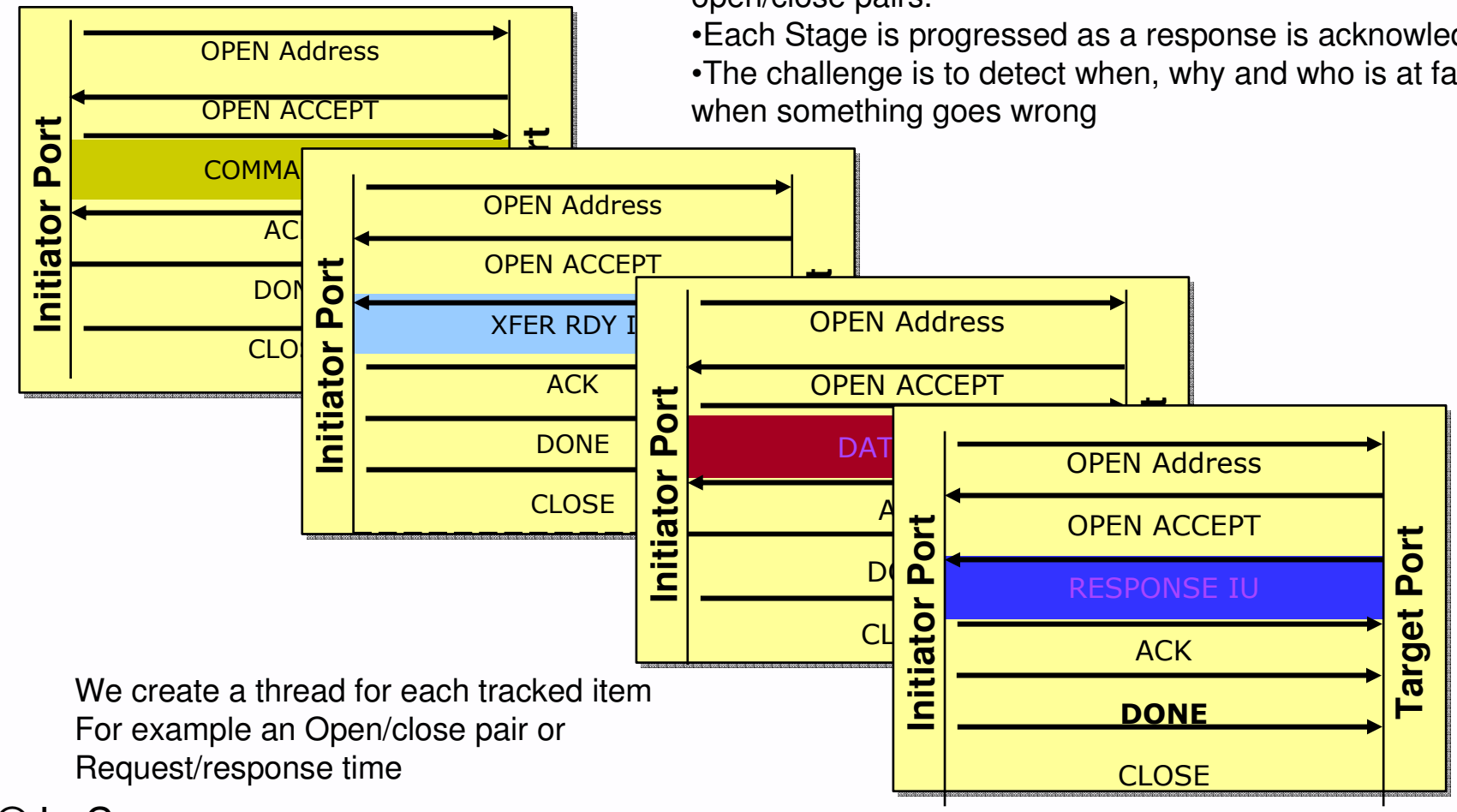
Long term command tracking

- SAS provides a transport for SCSI,
- Each SCSI operation is encapsulated between Address open/close pairs.
- Each Stage is progressed as a response is acknowledged
- The challenge is to detect when, why and who is at fault when something goes wrong



We create a thread for each tracked item
For example an Open/close pair or
Request/response time

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Tracker Log Interface

LeCroy SASSuite Application Software - [C:\Program Files\CATC\SASTracer\Sam...\tracker_3HBAx8Drives.strk]

File Setup Record Generate Tracker Report Search View Tools Window Help

Ch	Command	Sp	Compl Time	Δ	COMMAND	Prot	Target SAS Address	Tag			Level	AD
I1	21.405 018 887	3	317.353 µs	Δ	0x0000A7A	SSP	50010B90_00005421	0x00E1	IU	SCSI LUN	1	
I1	21.405 430 405	3	298.295 µs	Δ	0x0000A7B	SSP	[illegible]	[illegible]	[illegible]	[illegible]	1	
I1	21.405 822 977	3	520.495 µs	Δ	0x0000A7C	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
I1	21.406 436 962	3	252.473 µs	Δ	0x0000A7D	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	
I1	21.406 782 887	3	252.510 µs	Δ	0x0000A7E	SSP	[illegible]	[illegible]	[illegible]	[illegible]	1	
I1	21.407 129 352	3	260.090 µs	Δ	0x0000A7F	SSP	50010B90_00005421	0x00F1	IU	SCSI LUN	1	
I1	21.407 480 962	3	252.573 µs	Δ	0x0000A80	SSP	50010B90_00005421	0x00F7	IU	SCSI LUN	1	
I1	21.407 826 075	3	1.085 ms	Δ	0x00000D5	SSP	50010B90_00005421	0x00EB	IU	SCSI LUN	1	
I1	21.408 172 090	3	1.084 ms	Δ	0x00000D6	SSP	50010B90_00005421	0x00DA	IU	SCSI LUN	1	
I1	21.408 517 925	3	1.086 ms	Δ	0x00000D7	SSP	50010B90_00005421	0x00D3	IU	SCSI LUN	1	
I1	21.408 864 932	3	252.533 µs	Δ	0x0000A84	SSP	50010B90_00005421	0x00C8	IU	SCSI LUN	1	
I1	21.409 212 480	3	253.183 µs	Δ	0x0000A85	SSP	50010B90_00005421	0x00D2	IU	SCSI LUN	1	
I1	21.409 559 940	3	251.685 µs	Δ	0x0000A86	SSP	50010B90_00005421	0x00EE	IU	SCSI LUN	1	
I1	21.409 905 505	3	252.083 µs	Δ	0x0000A87	SSP	50010B90_00005421	0x00E2	IU	SCSI LUN	1	
I1	21.410 251 157	3	254.475 µs	Δ	0x0000A88	SSP	50010B90_00005421	0x00C5	IU	SCSI LUN	1	
I1	21.410 797 112	3	252.550 µs	Δ	0x0000A89	SSP	50010B90_00005421	0x00EA	IU	SCSI LUN	1	
I1	21.411 170 015	3	254.007 µs	Δ	0x0000A8A	SSP	50010B90_00005421	0x00F3	IU	SCSI LUN	1	
I1	21.411 517 022	3	252.963 µs	Δ	0x0000A8B	SSP	50010B90_00005421	0x00E3	IU	SCSI LUN	1	
I1	21.411 863 580	3	252.368 µs	Δ	0x0000A8C	SSP	50010B90_00005421	0x00F2	IU	SCSI LUN	1	
I1	21.412 209 505	3	252.405 µs	Δ	0x0000A8D	SSP	50010B90_00005421	0x013C	IU	SCSI LUN	1	
I1	21.412 556 150	3	251.723 µs	Δ	0x0000A8E	SSP	50010B90_00005421	0x00EF	IU	SCSI LUN	1	

Identify specific commands that take more than 1ms to complete

Ready Search: Fwd

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More Information

- http://www.lecroy.com
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